MOSFET - Power, Single P-Channel, µ8FL

-30 V, 7.5 mΩ, -88.6 A

NVTFS015P03P8Z

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
–30 V	7.5 mΩ @ –10 V	–88.6 A
	12 mΩ @ –4.5 V	

Features

- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- Advanced Package Technology in 3.3 x 3.3 mm for Space Saving and Excellent Thermal Conduction
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Load Switch
- Protection: Reverse Current, Over Voltage, and Reverse Negative Voltage
- Battery Management

S (1, 2, 3)

G (4)

P–Channel MOSFET

D (5, 6, 7, 8)

MARKING DIAGRAMS

WDFN8 (µ8FL) CASE 511AB

XXXXX
AYWW■

WDFNW8 (µ8FL WF) CASE 515AN

XXXX
AYWW■

XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
■ = Pb−Free Package

(Note: Microdot may be in either location)

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

| Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	–30	V
Gate−to−Source Voltage			V_{GS}	± 25	V
Continuous Drain Current $R_{θJC}$ (Notes 1, 2)	Steady State	T_C = 25°C	I_D	–88.6	A
		T_C = 100°C		–62.6	
Power Dissipation $R_{θJC}$ (Notes 1, 2)		T_C = 25°C	P_D	88.2	W
		T_C = 100°C		44.1	
Continuous Drain Current $R_{θJA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	–17	A
		T_A = 100°C		–12	
Power Dissipation $R_{θJA}$ (Notes 1, 2)		T_A = 25°C	P_D	3.2	W
		T_A = 100°C		1.6	
Pulsed Drain Current	T_A = 25°C, t_p = 10 µs		I_{DM}	–353	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	73.5	A
Single Pulse Drain to Source Avalanche Energy (I_L = 8.5 A)			E_{AS}	88	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Drain) (Note 2)	$R_{θJC}$	1.7	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{θJA}$	46.4	°C/W

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 1 in^2, 2 oz. Cu pad. Assuming a 76 mm x 76 mm x 1.6 mm board.
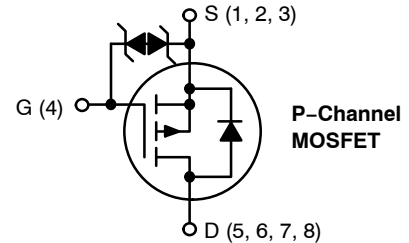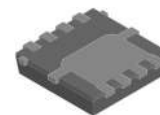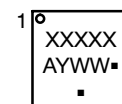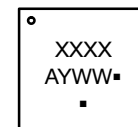
ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = −250 μA, ref to 25°C			−4.4		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −30 V	T_J = 25°C			−10	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 25 V				± 10	μA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−1.0		−3.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = −250 μA, ref to 25°C			5.6		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −10 V, I_D = −12 A			5.0	7.5	mΩ
		V_{GS} = −4.5 V, I_D = −10 A			8.0	12	
Froward Transconductance	g_{FS}	V_{DS} = −5 V, I_D = −10 A			77		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −15 V			2706		pF
Output Capacitance	C_{oss}				907		
Reverse Transfer Capacitance	C_{rss}				875		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −10 A			37		nC
Threshold Gate Charge	$Q_{G(TH)}$				5.1		
Gate−to−Source Charge	Q_{GS}				8.2		
Gate−to−Drain Charge	Q_{GD}				21.7		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −10 V, V_{DS} = −15 V, I_D = −10 A			62.3	105	
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 3)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −10 A, R_G = 6 Ω			25		ns
Rise Time	t_r				138		
Turn−Off Delay Time	$t_{d(off)}$				55		
Fall Time	t_f				98		
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −10 V, V_{DS} = −15 V, I_D = −10 A, R_G = 6 Ω			6		ns
Rise Time	t_r				17		
Turn−Off Delay Time	$t_{d(off)}$				52		
Fall Time	t_f				63		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −10 A	T_J = 25°C		−0.8	−1.3	V
			T_J = 125°C		−0.65		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = −10 A			40.7		ns
Charge Time	t_a				18.4		
Discharge Time	t_b				22.3		
Reverse Recovery Charge	Q_{RR}				29		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

NVTFS015P03P8Z

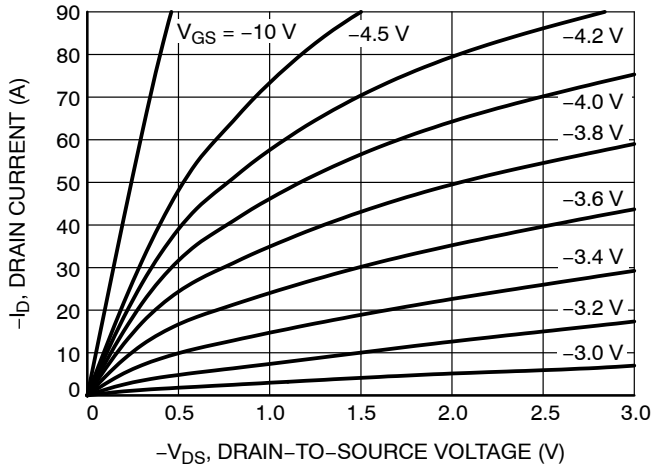## TYPICAL CHARACTERISTICS

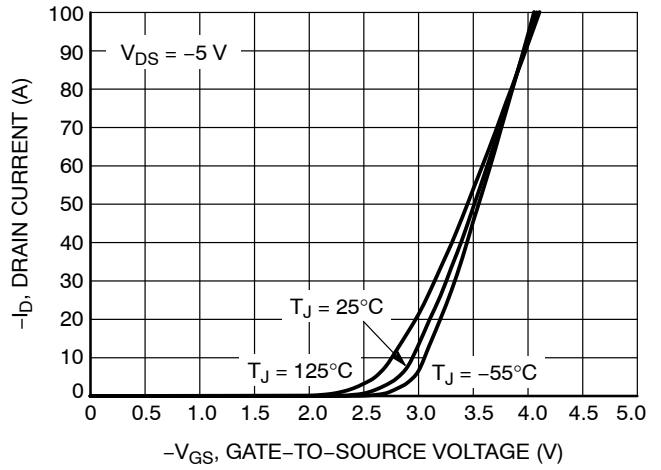Figure 1. On−Region Characteristics
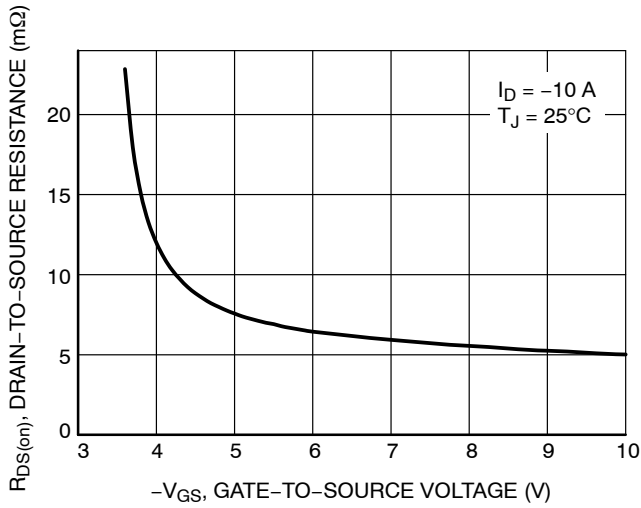

Figure 2. Transfer Characteristics

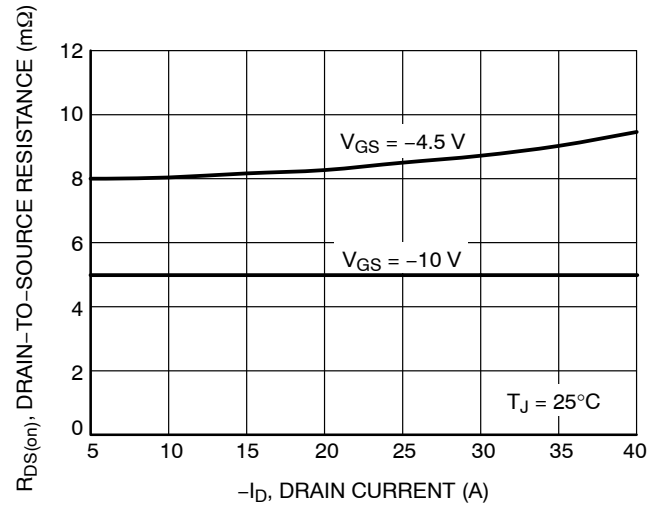Figure 3. On−Resistance vs. Gate−to−Source Voltage

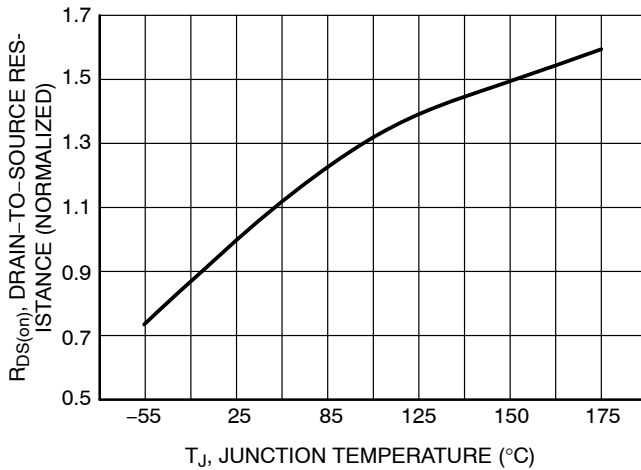Figure 4. On−Resistance vs. Drain Current and Gate Voltage
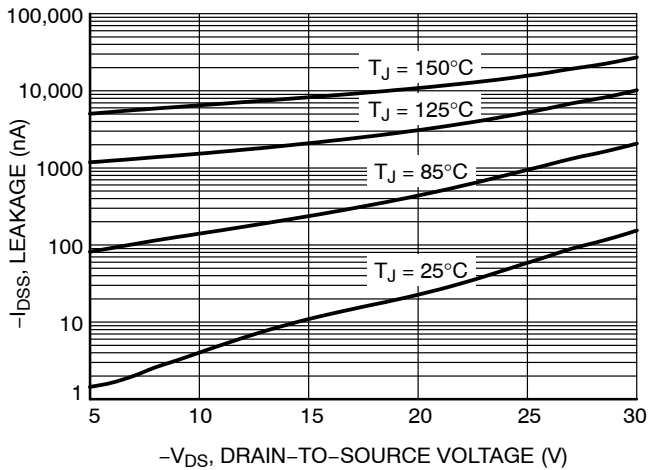

Figure 5. On−Resistance Variation with Temperature
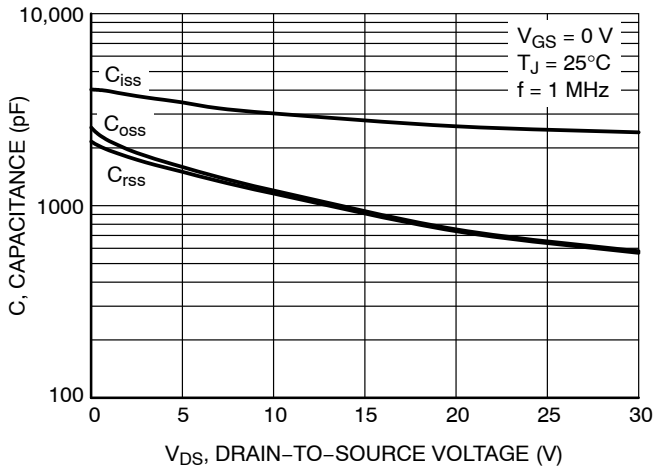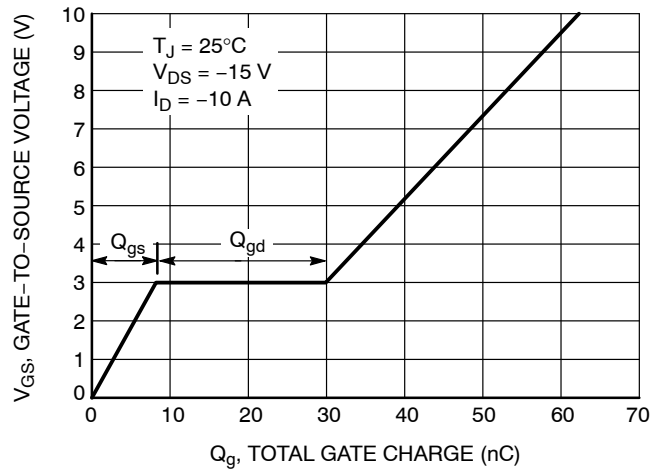

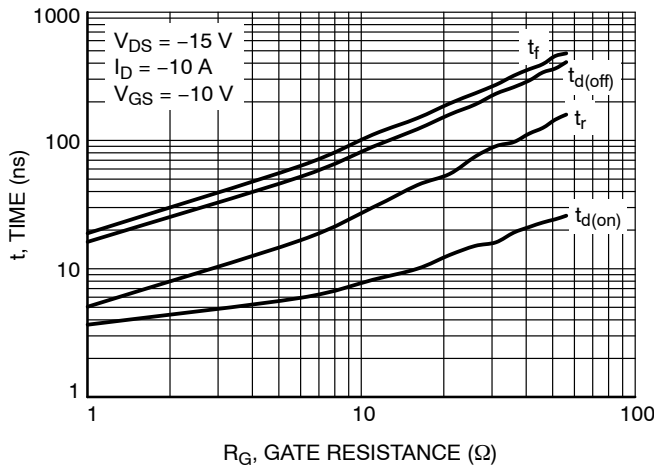Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

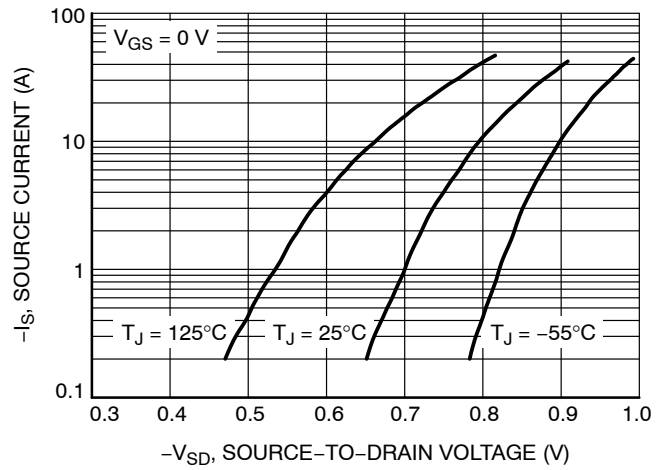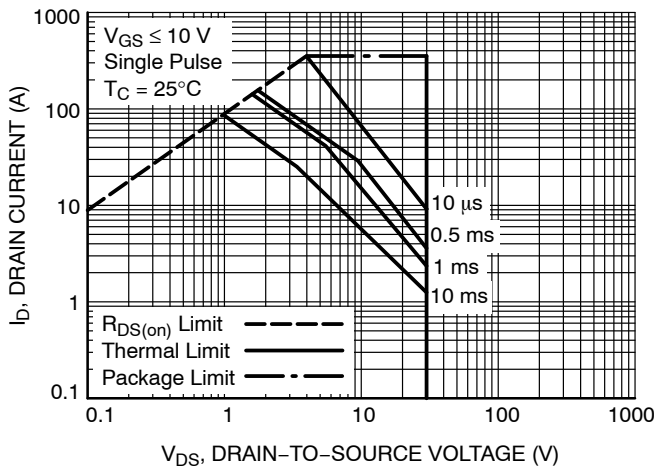**Figure 7. Capacitance Variation**

Figure 8. Gate−to−Source vs. Total Charge

Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

Figure 11. Maximum Rated Forward Biased Safe Operating Area
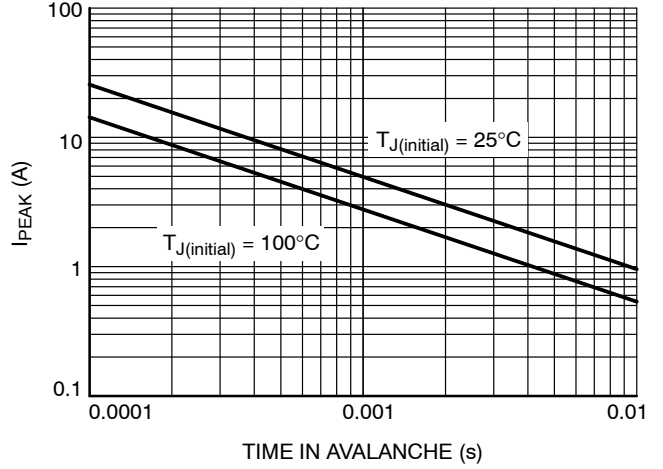
Figure 12. Maximum Drain Current vs. Time in Avalanche

NVTFS015P03P8Z

TYPICAL CHARACTERISTICS
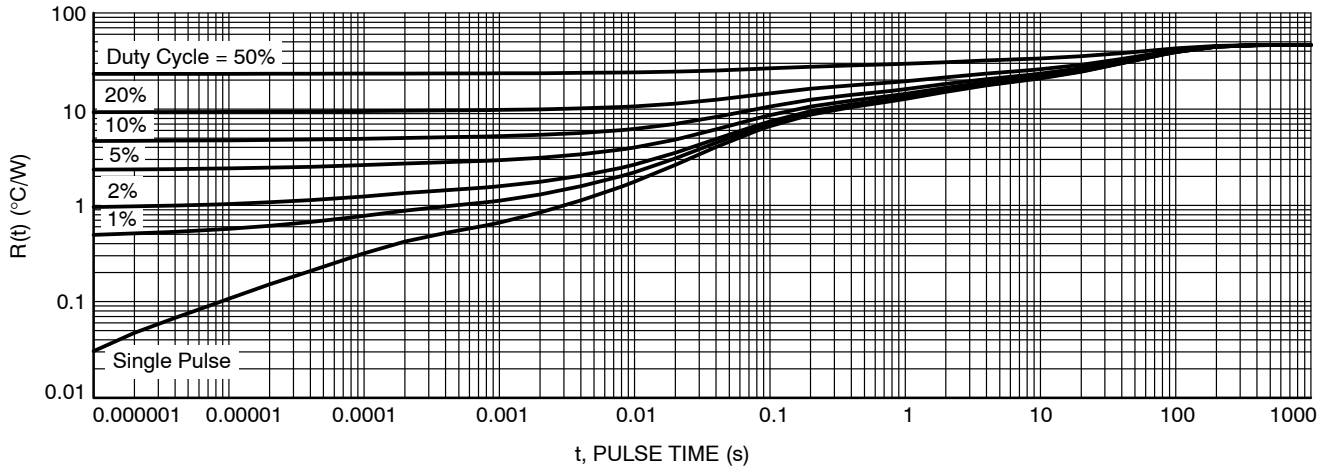
Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVTFS015P03P8ZTAG	15P3	WDFN8 (Pb−Free)	1500 / Tape & Reel
NVTFWS015P03P8ZTAG	15PW	WDFN8 (Pb−Free, Wettable Flanks)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

onsemi

WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

SCALE 2:1

DATE 23 APR 2012
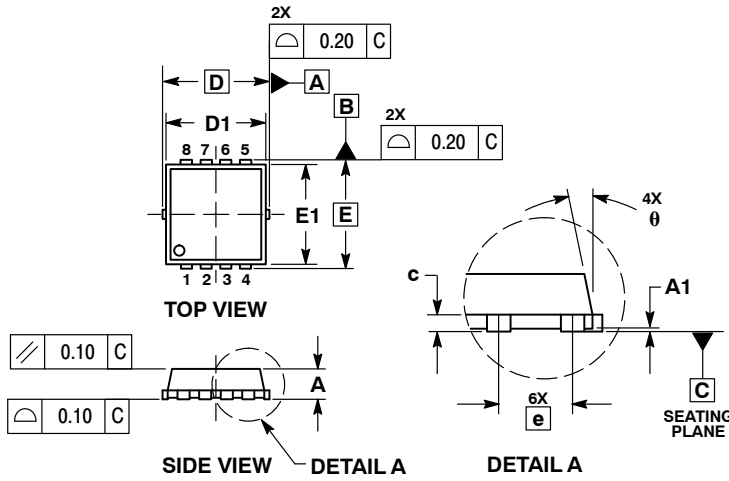
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

2X $\bigtriangleup$ | 0.20 | C

D | A
B
2X $\bigtriangleup$ | 0.20 | C

8 7 6 5
E1 | E
1 2 3 4

TOP VIEW

$\varnothing$ | 0.10 | C
$\bigtriangleup$ | 0.10 | C
A

SIDE VIEW — **DETAIL A**

4X θ
c
A1
6X e
C SEATING PLANE

DETAIL A

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °
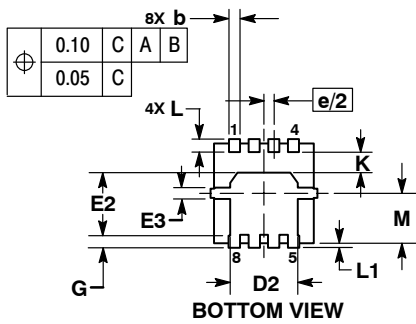
8X b
$\oplus$ | 0.10 | C | A | B
| 0.05 | C
4X L
e/2
1 4
K
E2
E3
M
G
8 5
D2
L1

BOTTOM VIEW

GENERIC MARKING DIAGRAM*

1 o
XXXXX
AYWW■
■
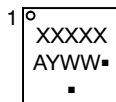
XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
■ = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*

8X 0.42
0.65 PITCH
4X 0.66
PACKAGE OUTLINE
3.60
2.30
0.75 0.57
0.47
2.37
3.46

DIMENSION: MILLIMETERS
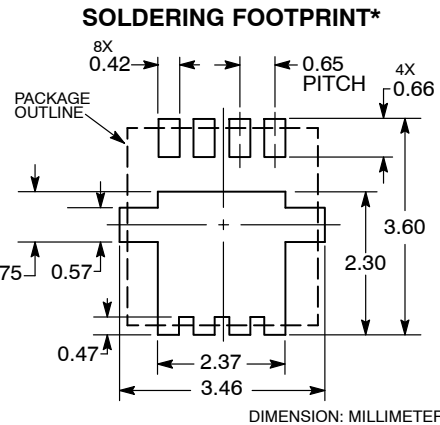
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON30561E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	WDFN8 3.3X3.3, 0.65P		PAGE 1 OF 1

ON Semiconductor®
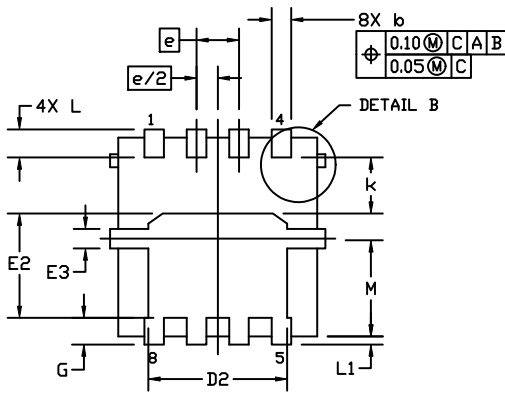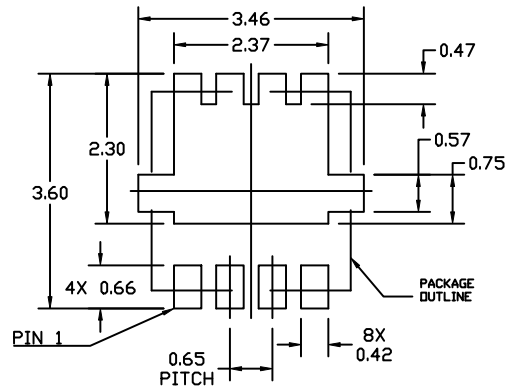
WDFNW8 3.3x3.3, 0.65P (Full–Cut μ8FL WF)
CASE 515AN
ISSUE O

DATE 25 AUG 2020
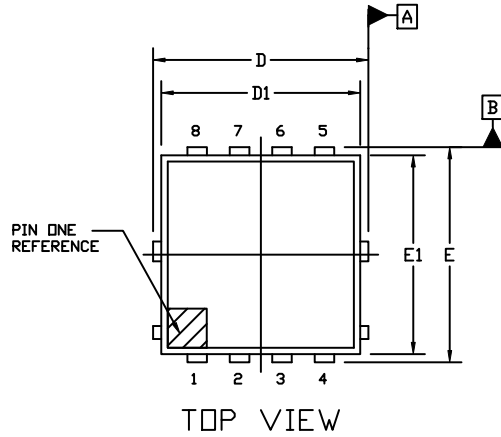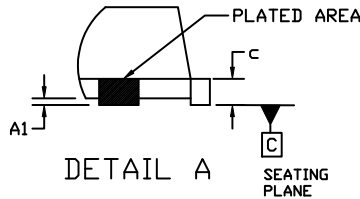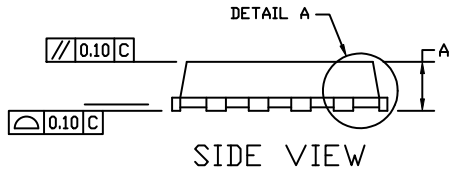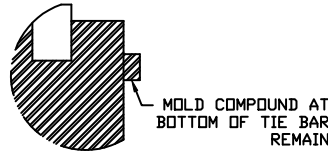
NOTES:

1. DIMENSIONING AND TOLERANCING PER.ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

PIN ONE REFERENCE

TOP VIEW

PLATED AREA

DETAIL A

SEATING PLANE

// 0.10 C

⌒ 0.10 C

SIDE VIEW

DETAIL A

MOLD COMPOUND AT BOTTOM OF TIE BAR REMAIN

DETAIL B

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.30	0.40
c	0.15	0.20	0.25
D	3.05	3.30	3.55
D1	2.95	3.05	3.15
D2	1.98	2.11	2.24
E	3.05	3.30	3.55
E1	2.95	3.05	3.15
E2	1.47	1.60	1.73
E3	0.23	0.30	0.40
e	0.65 BSC		
G	0.30	0.41	0.51
K	0.65	0.80	0.95
L	0.30	0.43	0.59
L1	0.06	0.13	0.20
M	1.40	1.50	1.60

8X b
⊕ 0.10 Ⓜ C A B
  0.05 Ⓜ C

4X L

DETAIL B

BOTTOM VIEW

3.46
2.37
0.47
2.30
0.57
0.75
3.60
4X 0.66
PIN 1
0.65 PITCH
8X 0.42
PACKAGE OUTLINE

RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*
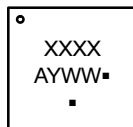
XXXX
AYWW▪
▪

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb–Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	WDFNW8 3.3x3.3, 0.65P (Full–Cut μ8FL WF)	PAGE 1 OF 1

ADDITIONAL INFORMATION

◊