AOZ8802ADI

Ultra-Low Capacitance TVS Diode Array

General Description

The AOZ8802ADI is a transient voltage suppressor array designed to protect high speed data lines such as HDMI, MDDI, USB, SATA, and Gigabit Ethernet from damaging ESD events.

This device incorporates four surge rated, low capacitance steering diodes and a TVS in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground.

The AOZ8802ADI provides a typical line to line capacitance of 0.3pF and low insertion loss up to 6GHz providing greater signal integrity making it ideally suited for HDMI 1.3 applications, such as Digital TVs, DVD players,
set-top boxes and USB applications in mobile computing devices.

The AOZ8802ADI comes in a RoHS compliant and Halogen Free 1.6mm x 1.0mm x 0.55mm DFN-6 package and is rated -40°C to +85°C junction temperature range.

Features

- ESD protection for high-speed data lines:
  - IEC 61000-4-2, level 4 (ESD) immunity test
  - Air discharge: ±15kV; Contact discharge: ±15kV
  - IEC61000-4-4 (EFT) 40A (5/50nS)
  - IEC61000-4-5 (Lightning) 2.5A (8/20μS)
  - Human Body Model (HBM) ±24kV
- Array of surge rated diodes with internal TVS diode
- Small package saves board space
- Protects two I/O lines
- Low capacitance between I/O lines: 0.3pF
- Low clamping voltage
- Low operating voltage: 5.0V

Applications

- USB, MDDI, SATA ports
- Monitors and flat panel displays
- Set-top box
- Video graphics cards
- Digital Video Interface (DVI)
- Notebook computers

Green Product

Typical Application

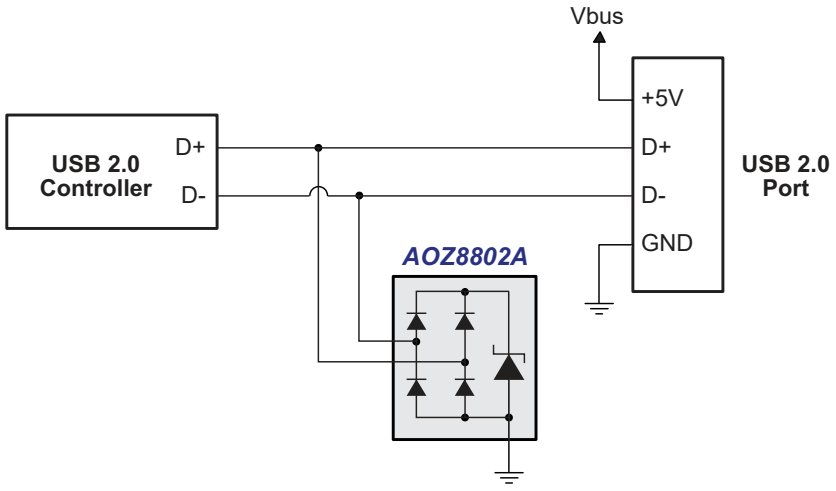


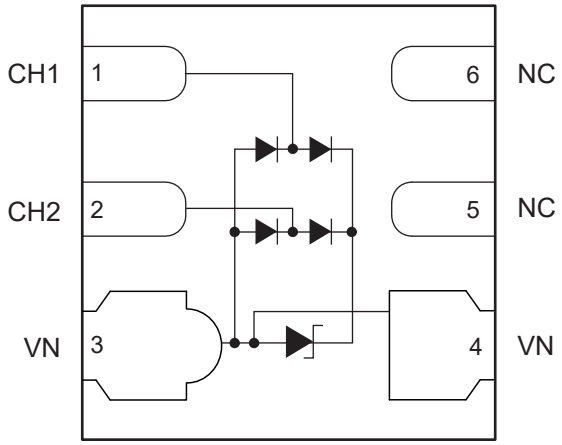
Figure 1. USB Port

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ8802ADI	-40°C to +85°C	DFN-6	Green Product RoHS Compliant

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration



DFN-6
(Top View)

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating per IEC61000-4-2, contact(1)	±15kV
ESD Rating per IEC61000-4-2, air(1)	±15kV
ESD Rating per Human Body Model(2)	±24kV

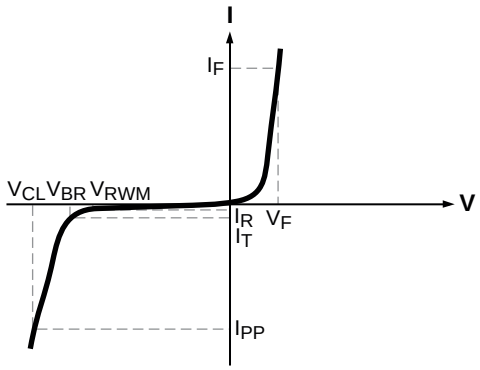
Notes:
1. IEC 61000-4-2 discharge with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330Ω.
2. Human Body Discharge per MIL-STD-883, Method 3015 $C_{Discharge}$ = 100pF, $R_{Discharge}$ = 1.5kΩ.

Maximum Operating Ratings

Parameter	Rating
Junction Temperature (T_J)	-40°C to +125°C

Electrical Characteristics

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Diagram
I_{PP}	Maximum Reverse Peak Pulse Current	
V_{CL}	Clamping Voltage @ I_{PP}	
V_{RWM}	Working Peak Reverse Voltage	
I_R	Maximum Reverse Leakage Current	
V_{BR}	Breakdown Voltage	
I_F	Forward Current	
V_F	Forward Voltage	
P_{PK}	Peak Power Dissipation	
C_J	Max. Capacitance @ V_R = 0 and f = 1MHz	

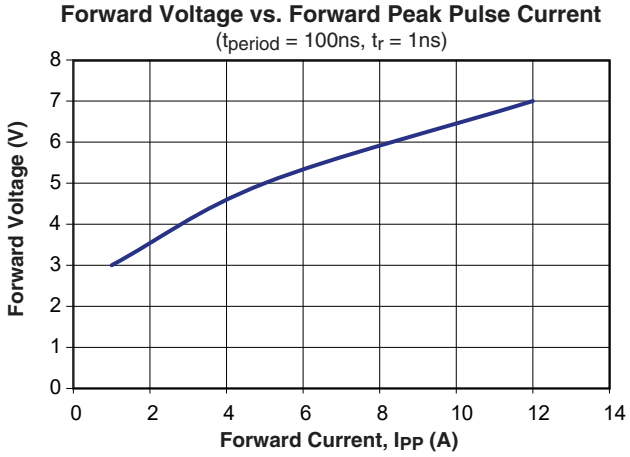
Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

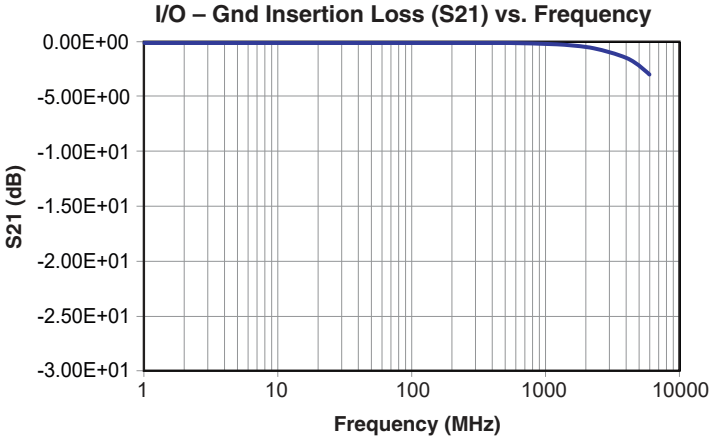
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{RWM}	Reverse Working Voltage	Between I/O and VN[3]			5.0	V
V_{BR}	Reverse Breakdown Voltage	I_T = 1mA, between I/O and VN[4]	6.0			V
I_R	Reverse Leakage Current	V_{RWM} = 5V, between I/O and VN			1	µA
V_F	Diode Forward Voltage	I_F = 15mA	0.70	0.85	1	V
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 1A, tp = 100ns, any I/O pin to Ground[5]			 12 -3	 V V
	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 5A, tp = 100ns, any I/O pin to Ground[5]			 14 -5	 V V
	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 12A, tp = 100ns, any I/O pin to Ground[5]			 16.5 -7	 V V
C_j	Channel Input Capacitance	V_R = 0V, f = 1MHz, between I/O pins		0.30	0.35	pF
		V_R = 0V, f = 1MHz, any I/O pin to Ground		0.60	0.75	pF

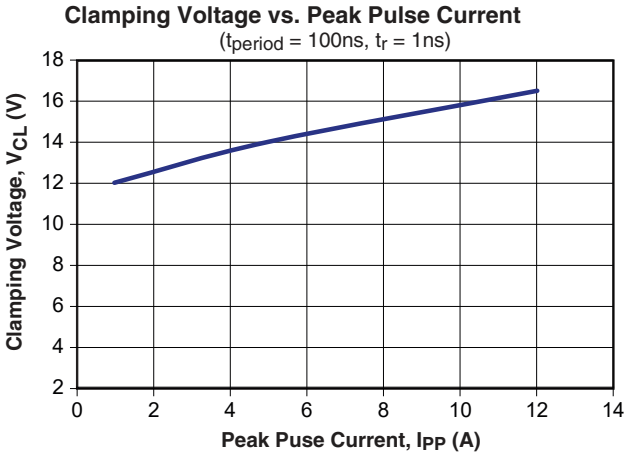
Notes:

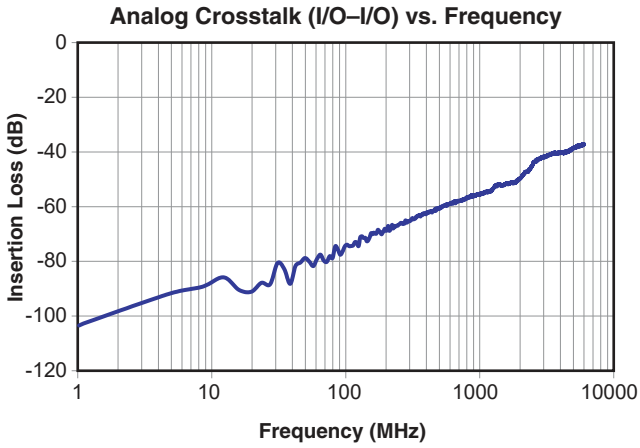
3. The working peak reverse voltage, V_{RWM}, should be equal to or greater than the DC or continuous peak operating voltage level.
4. V_{BR} is measured at the pulse test current I_T.
5. Measurements performed using a 100ns Transmission Line Pulse (TLP) system.

Typical Performance Characteristics









Protecting USB Ports from ESD

Because electrostatic discharge (ESD) is common in electronic systems, a device that provides protection from the undesirable effects of ESD must be included in the system design. Designing ESD protection structures is becoming more and more challenging with the system bus and I/O operating more often at high-speed data rates. An Integrated Circuit (IC) connected to external ports can be damaged by ESD from the operating environment. The result of ever-shrinking IC process technology is the decrease of ESD robustness because of the smaller geometry of the silicon die.

Since USB is a hot insertion and removal system, the USB components are subjected to ESD and cable discharge event more frequently. Traditional methods of ESD protection include metal oxide varistors (MOVs), and regular CMOS or bipolar clamping diodes. At higher data rates the parasitic characteristics of those devices can cause distortion, deterioration and data loss of the signal integrity. AOZ8802ADI offers ESD protection for high-speed data rates and for diode array chips for ease of design.

The very low 0.6pF (typical) line capacitance of the AOZ8802ADI ensures less distortion of the 480 Mbit/s USB 2.0 signal; the chips also protect against electrostatic discharge up to the stringent IEC61000-4-2 level 4, 8kV (Contact Discharge) and 15kV standard (Air Discharge). They also provide ultra low matching capacitance to help improve the signal quality of differential data lines. Monolithic integration provides high device reliability, and an optimized pin-out allows EMI-free board layouts. Figure 2 illustrates the flow through design of the PCB layout with the AOZ8802ADI package design. The pinout of the AOZ8802ADI is designed to simply drop onto the IO lines of a USB 2.0 design without having to divert the signal lines that may add more parasitic inductance. Pins 1, 2 & 3 is connected to the internal TVS devices and ground. and pins 4, 5, 6 are no connects. The no connects is in place so the package can be securely soldered onto the PCB surface.

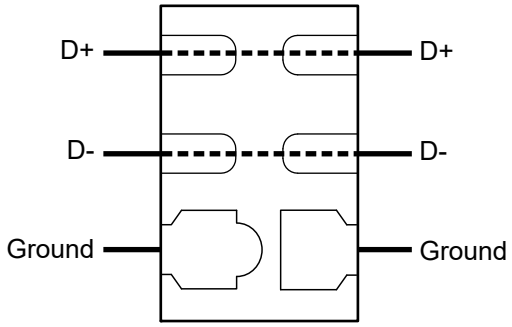


Figure 2. Flow-through Layout

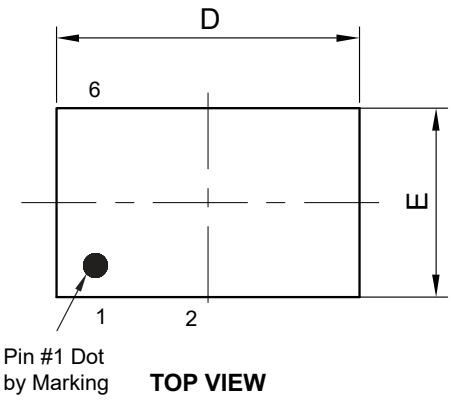
USB 2.0 PCB Layout Guidelines

Printed circuit board layout is the key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the simplest and most important design rule to follow. The AOZ8802ADI devices should be located as close as possible to the noise source. The placement of the AOZ8802ADI devices should be used on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the AOZ8802ADI devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse can be coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to

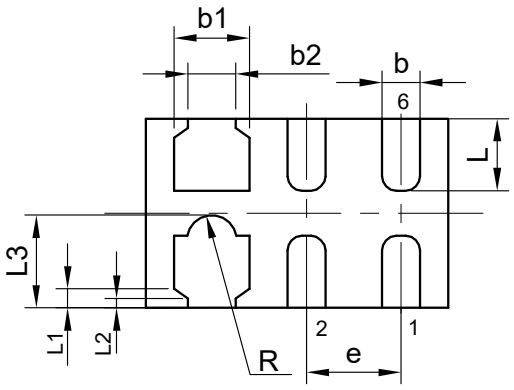
low impedance, which ensures that the surge energy will be dissipated by the AOZ8802ADI device. Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced. Minimize interconnecting line lengths by placing devices with the most interconnect as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground can cause ground bounce. The clamping performance of TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic

inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design.

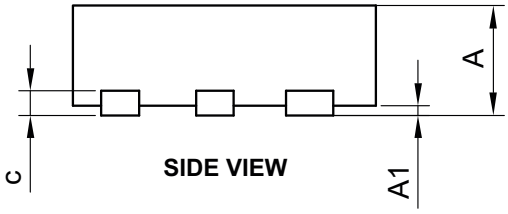
Package Dimensions, DFN-6 1.6mm x 1.0mm x 0.55mm



TOP VIEW

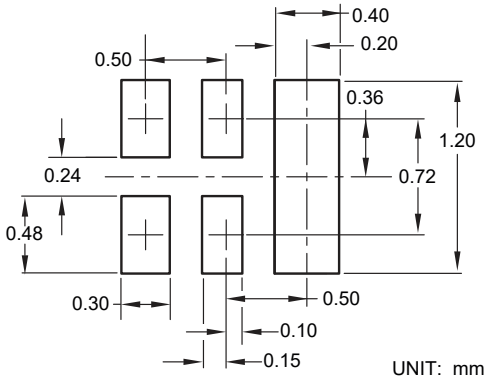


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



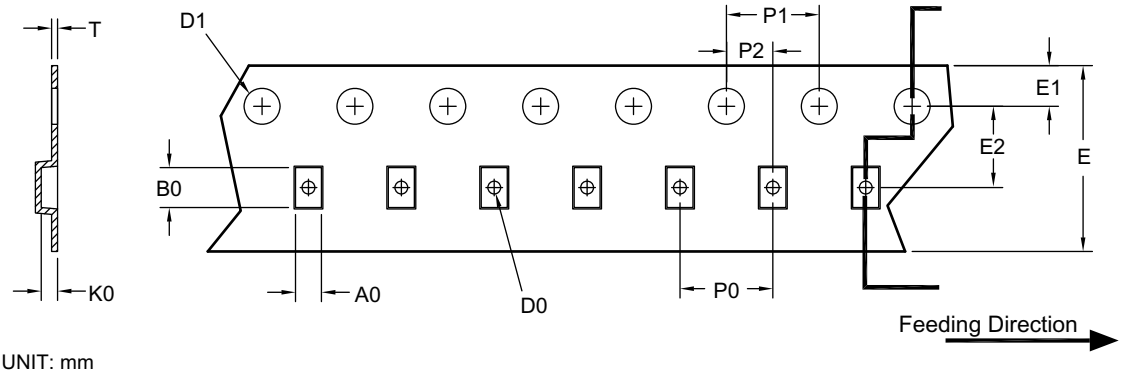
UNIT: mm

	Dimensions in Millimeters			Dimensions in Inches		
Symbol	**Min.**	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A	0.50	0.55	0.60	0.0196	0.0216	0.0236
A1	—	0.02	0.05	—	0.0007	0.0019
b	0.15	0.20	0.25	0.0059	0.0078	0.0098
b1	0.35	0.40	0.45	0.0137	0.0157	0.0177
b2	0.20	0.25	0.30	0.0078	0.0098	0.0118
c	0.10	0.15	0.20	0.0039	0.0059	0.0078
D	1.55	1.60	1.65	0.0610	0.0629	0.0649
e	0.50 BSC			0.0196 BSC		
E	0.95	1.00	1.05	0.0374	0.0393	0.0413
L	0.33	0.38	0.43	0.0129	0.0150	0.0169
L1	0.10 BSC			0.0039 BSC		
L2	0.05 BSC			0.0019 BSC		
L3	0.49 BSC			0.0192 BSC		
R	0.08	0.13	0.18	0.0031	0.0051	0.0071

Note:
4. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, DFN-6 1.6mm x 1.0mm x 0.55mm

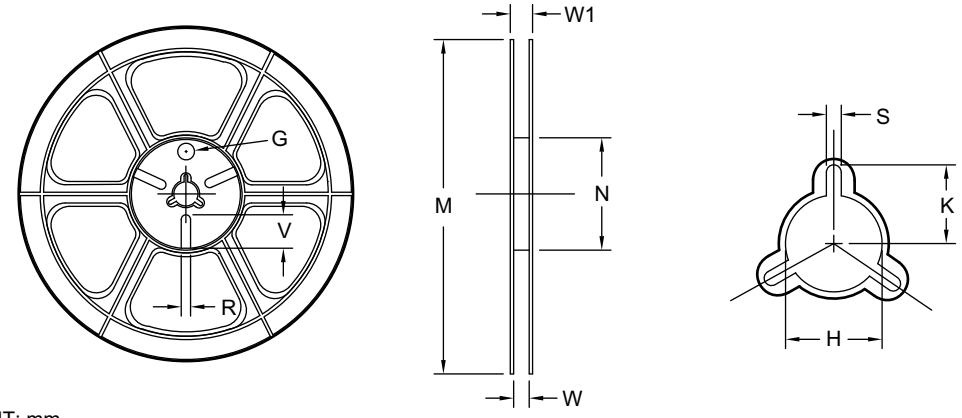
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN 1.6 x 1.0 (8 mm)	1.12 ±0.05	1.72 ±0.05	0.70 ±0.05	0.55 ±0.05	1.55 ±0.10	8.00 +0.30/-0.10	1.75 ±0.10	3.50 ±0.05	4.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.25 ±0.05

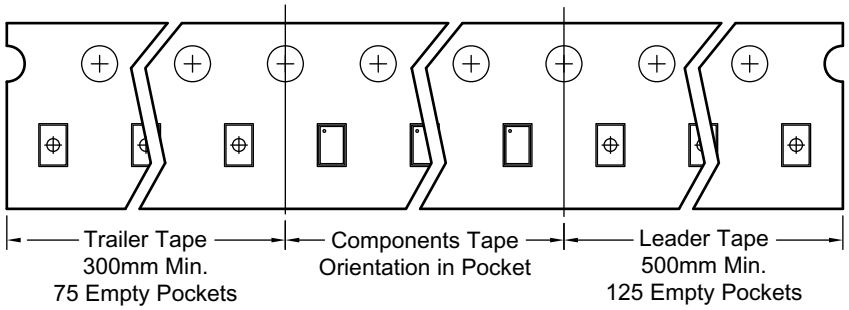
Reel



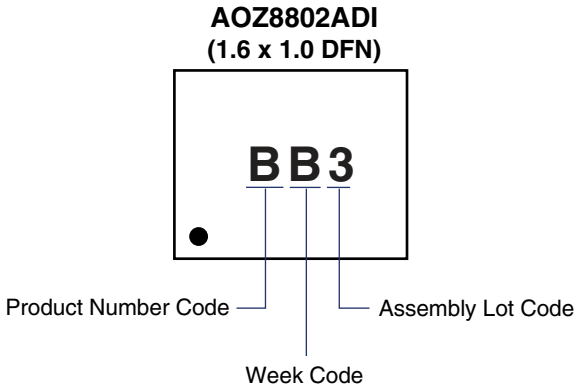
UNIT: mm

Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
8mm	ø178	ø178.0 ±0.50	ø60.0 ±1	9.0 ±0.5	N/A	ø13.0 +0.5/-0.2	10.25 ±0.2	2.40 ±0.10	ø9.8	N/A	N/A

Leader / Trailer & Orientation



Part Marking



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