General Purpose Transistor

NPN Silicon

Features

- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector – Emitter Voltage	V_{CEO}	32	Vdc
Collector – Base Voltage	V _{CBO}	32	Vdc
Emitter – Base Voltage	V _{EBO}	5.0	Vdc
Collector Current – Continuous	Ic	100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board (Note 1) T _A = 25°C Derate above 25°C	P _D	225 1.8	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{ heta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate (Note 2), T _A = 25°C Derate above 25°C	P _D	300 2.4	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T _J , T _{stg}	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. $FR-5 = 1.0 \times 0.75 \times 0.062$ in.
- 2. Alumina = $0.4 \times 0.3 \times 0.024$ in. 99.5% alumina.

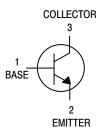


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SOT-23 (TO-236) CASE 318-08 STYLE 6



MARKING DIAGRAM



D3 = Specific Device Code

M = Date Code*

= Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping [†]
BCW33LT1G	SOT-23 (Pb-Free)	3,000/Tape & Reel
SBCW33LT1G	SOT-23 (Pb-Free)	3,000/Tape & Reel
BCW33LT3G	SOT-23 (Pb-Free)	10,000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector – Emitter Breakdown Voltage (I _C = 2.0 mAdc, I _B = 0)	V _{(BR)CEO}	32	_	Vdc
Collector – Base Breakdown Voltage ($I_C = 10 \mu Adc$, $I_B = 0$)	V _{(BR)CBO}	32	-	Vdc
Emitter – Base Breakdown Voltage ($I_E = 10 \mu Adc, I_C = 0$)	V _{(BR)EBO}	5.0	_	Vdc
Collector Cutoff Current $(V_{CB} = 32 \text{ Vdc}, I_E = 0)$ $(V_{CB} = 32 \text{ Vdc}, I_E = 0, T_A = 100^{\circ}\text{C})$	Ісво		100 10	nAdc μAdc
ON CHARACTERISTICS				
DC Current Gain (I _C = 2.0 mAdc, V _{CE} = 5.0 Vdc)	hFE	420	800	-
Collector – Emitter Saturation Voltage (I _C = 10 mAdc, I _B = 0.5 mAdc)	V _{CE(sat)}	-	0.25	Vdc
Base – Emitter On Voltage ($I_C = 2.0 \text{ mAdc}$, $V_{CE} = 5.0 \text{ Vdc}$)	V _{BE(on)}	0.55	0.70	Vdc
SMALL-SIGNAL CHARACTERISTICS	•		•	•
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 1.0 MHz)	C _{obo}	-	4.0	pF
Noise Figure ($V_{CE}=5.0~Vdc,~I_{C}=0.2~mAdc,~R_{S}=2.0~k\Omega,~f=1.0~kHz,~BW=200~Hz)$	NF	-	10	dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

EQUIVALENT SWITCHING TIME TEST CIRCUITS

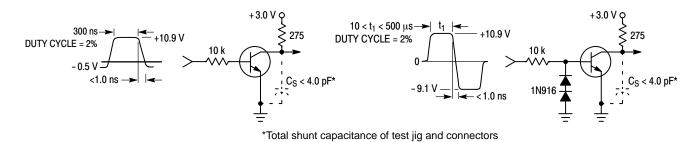


Figure 1. Turn-On Time

Figure 2. Turn-Off Time

TYPICAL NOISE CHARACTERISTICS

 $(V_{CE} = 5.0 \text{ Vdc}, T_A = 25^{\circ}C)$

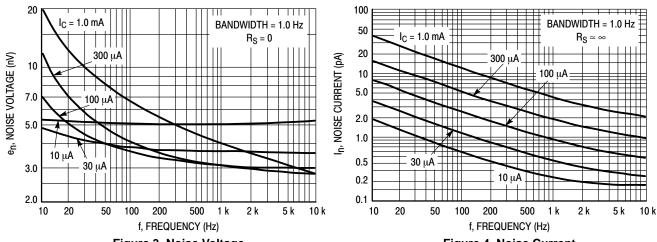


Figure 3. Noise Voltage

Figure 4. Noise Current

NOISE FIGURE CONTOURS

 $(V_{CE}=5.0~Vdc,~T_{A}=25^{\circ}C)$

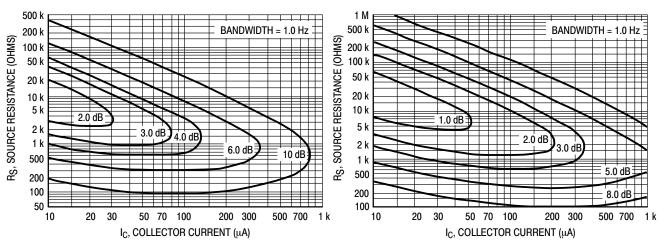


Figure 5. Narrow Band, 100 Hz

Figure 6. Narrow Band, 1.0 kHz

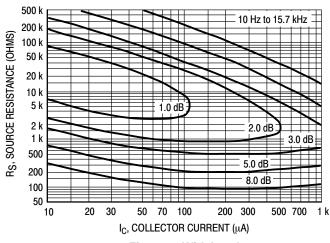


Figure 7. Wideband

Noise Figure is defined as:

NF =
$$20 \log_{10} \left(\frac{e_n^2 + 4KTR_S + I_n^2 R_S^2}{4KTR_S} \right)^{1/2}$$

e_n = Noise Voltage of the Transistor referred to the input. (Figure 3)

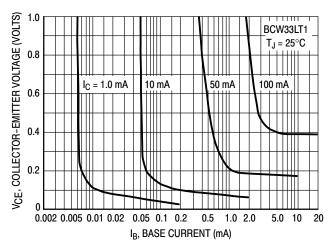
In = Noise Current of the Transistor referred to the input. (Figure 4)

 $K = Boltzman's Constant (1.38 x 10^{-23} j/{}^{\circ}K)$

T = Temperature of the Source Resistance (°K)

R_S = Source Resistance (Ohms)

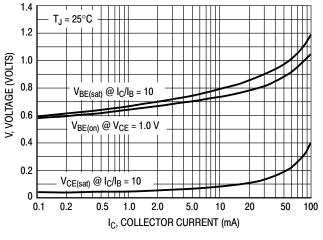
TYPICAL STATIC CHARACTERISTICS



100 T_A = 25°C I_B = 500 μA PULSE WIDTH = 300 μs IC, COLLECTOR CURRENT (mA) DUTY CYCLE ≤ 2.0% 80 400 μΑ 300 μA 60 200 μΑ 40 100 μΑ 20 0 5.0 10 15 20 25 30 35 0 40 V_{CE}, COLLECTOR-EMITTER VOLTAGE (VOLTS)

Figure 8. Collector Saturation Region

Figure 9. Collector Characteristics



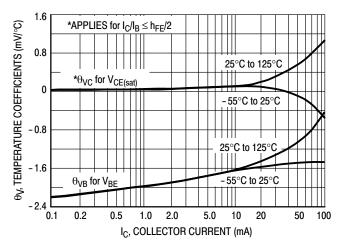
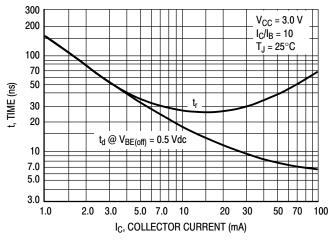


Figure 10. "On" Voltages

Figure 11. Temperature Coefficients



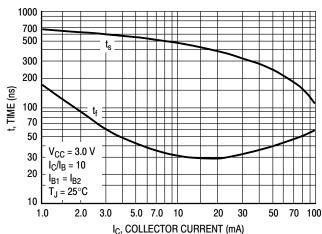
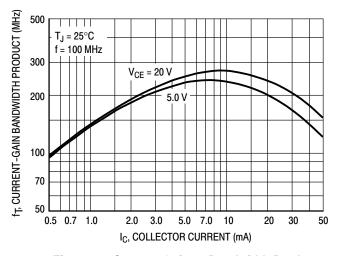


Figure 12. Turn-On Time

Figure 13. Turn-Off Time

TYPICAL DYNAMIC CHARACTERISTICS



10 f = 1.0 MHz 7.0 5.0 CAPACITANCE (pF) $C^{\dot{o}p}$ 3.0 2.0 0.1 0.2 2.0 0.05 0.5 1.0 5.0 10 50 VR, REVERSE VOLTAGE (VOLTS)

Figure 14. Current-Gain — Bandwidth Product

Figure 15. Capacitance

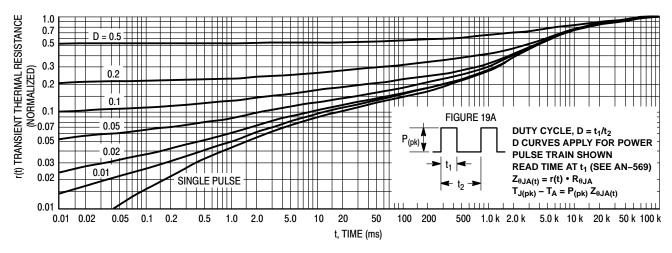


Figure 16. Thermal Response

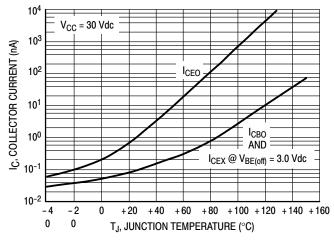


Figure 16A.

DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 16A. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 16 was calculated for various duty cycles.

To find $Z_{\theta JA(t)},$ multiply the value obtained from Figure 16 by the steady state value $R_{\theta JA}.$

Example:

The MPS3904 is dissipating 2.0 watts peak under the following conditions:

 $t_1 = 1.0 \text{ ms}, t_2 = 5.0 \text{ ms}. (D = 0.2)$

Using Figure 16 at a pulse width of 1.0 ms and D = 0.2, the reading of r(t) is 0.22.

The peak rise in junction temperature is therefore

 $\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88^{\circ}C.$

For more information, see AN-569.

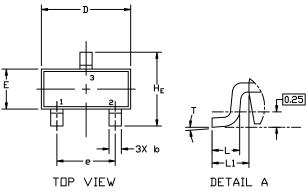




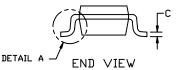
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DATE 01 MAR 2023









NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
- 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIM	ETERS		INCHES		
DIM	MIN.	N□M.	MAX.	MIN.	N□M.	MAX.
Α	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
С	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
HE	2.10	2.40	2.64	0.083	0.094	0.104
Т	0*		10°	0*		10°

GENERIC MARKING DIAGRAM*

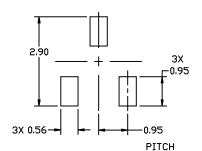


XXX = Specific Device Code

M = Date Code

■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SDLDERRM/D.

STYLES ON PAGE 2

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



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DATE 01 MAR 2023

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE	1	
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: I PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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