



PSMN8R5-100ES

N-channel 100 V 8.5 mΩ standard level MOSFET in I2PAK

11 October 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in a I2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- AC-to-DC power supply equipment
- Motor control
- Server power supplies
- Synchronous rectification

1.4 Quick reference data

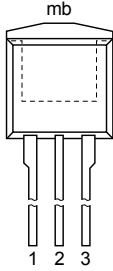
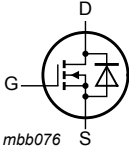
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$		-	-	100	V
I_D	drain current	$T_j = 25\text{ °C}; V_{GS} = 10\text{ V};$ Fig. 1	[1]	-	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Fig. 2		-	-	263	W
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ Fig. 13 ; Fig. 12		-	6.4	8.5	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; V_{DS} = 50\text{ V};$ Fig. 14 ; Fig. 15		-	33	-	nC
$Q_{G(tot)}$	total gate charge			-	111	-	nC
Avalanche Ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; I_D = 100\text{ A};$ $V_{sup} \leq 100\text{ V}; R_{GS} = 50\text{ Ω};$ unclamped; Fig. 3		-	-	219	mJ

[1] Continuous current limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>I2PAK (SOT226)</p>	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN8R5-100ES	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN8R5-100ES	PSMN8R5-100ES

5. Limiting values

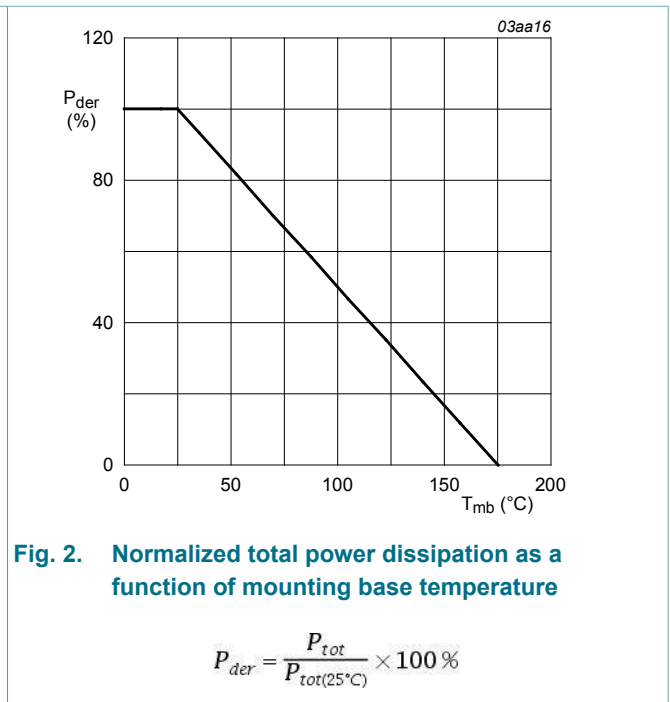
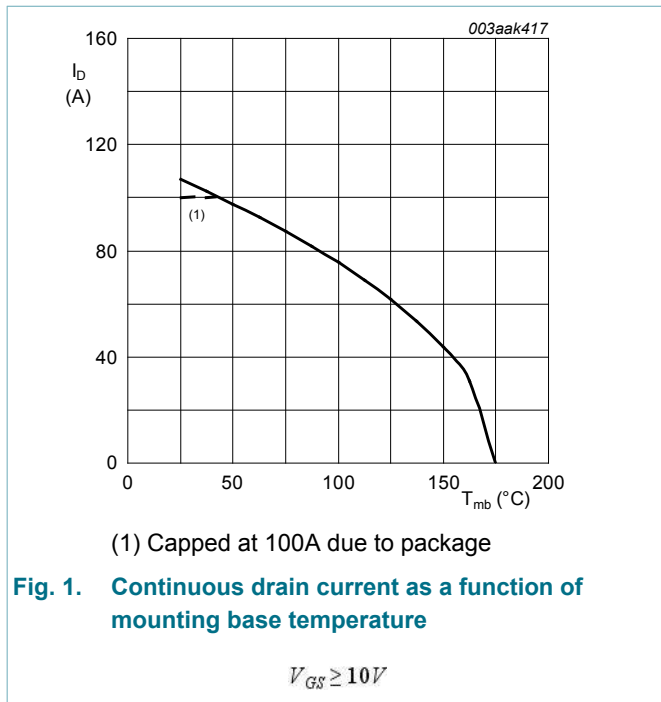
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 1	[1]	100	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 1		75	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 4	-	429	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2	-	263	W
T_{stg}	storage temperature		-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	-	100	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\ \mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	429	A
Avalanche Ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 100\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\ \Omega$; unclamped; Fig. 3		-	219	mJ

[1] Continuous current limited by package.



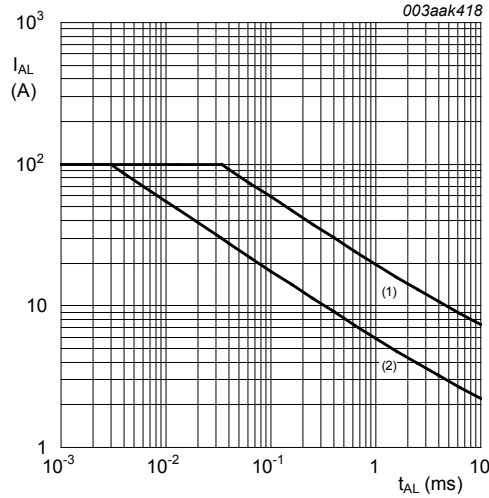


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j (int)} = 25^{\circ}C$; (2) $T_{j (int)} = 130^{\circ}C$

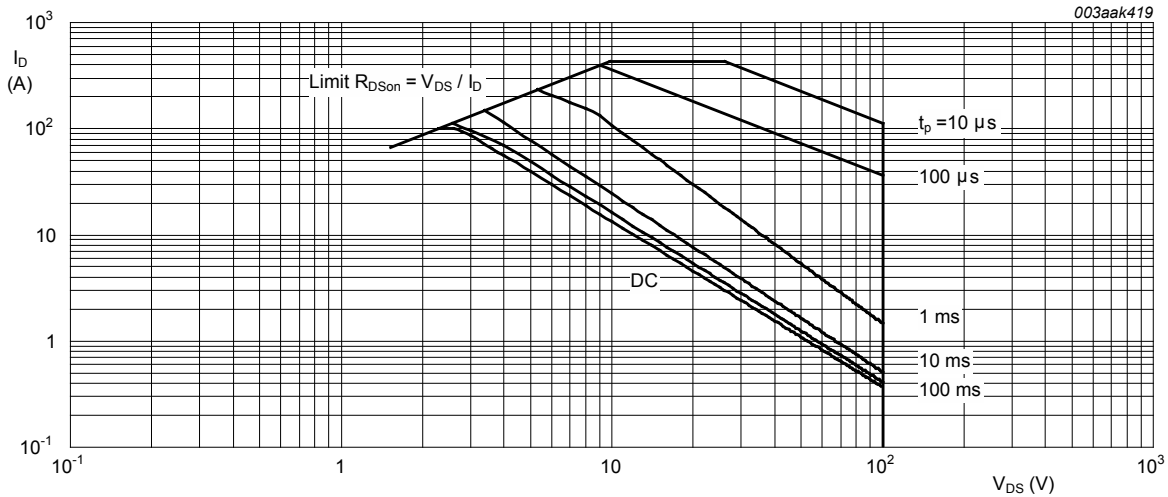


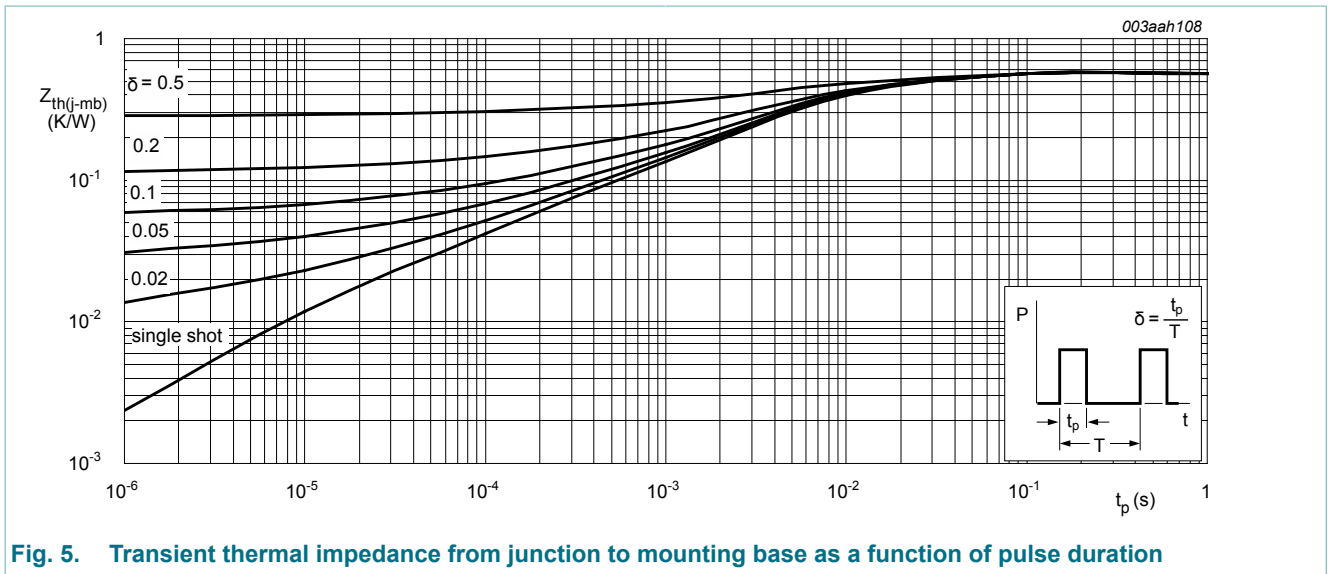
Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.49	0.57	K/W

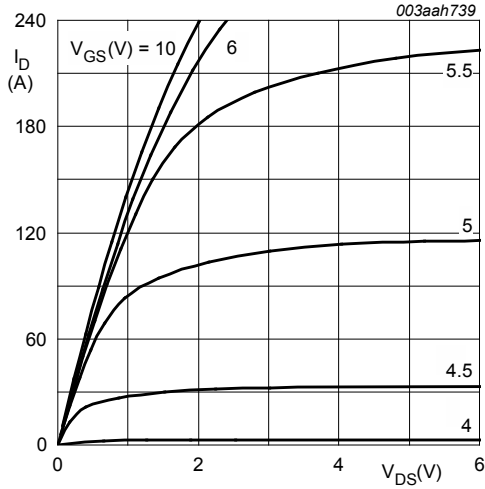


7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 10 ; Fig. 11	2.4	3	4	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 10	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 10	-	-	4.5	V
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.02	1	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 100 \text{ }^\circ C$	-	-	20	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C;$ Fig. 12	-	-	22.6	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ C;$ Fig. 12	-	-	14.9	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 13 ; Fig. 12	-	6.4	8.5	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	-	0.71	-	Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25 \text{ A}$; $V_{DS} = 50 \text{ V}$; $V_{GS} = 10 \text{ V}$; Fig. 14 ; Fig. 15	-	111	-	nC
Q_{GS}	gate-source charge		-	24	-	nC
$Q_{GS(\text{th})}$	pre-threshold gate-source charge		-	16	-	nC
$Q_{GS(\text{th-pl})}$	post-threshold gate-source charge		-	8	-	nC
Q_{GD}	gate-drain charge		-	33	-	nC
$V_{GS(\text{pl})}$	gate-source plateau voltage	$I_D = 15 \text{ A}$; $V_{DS} = 50 \text{ V}$; Fig. 14 ; Fig. 15	-	4.4	-	V
C_{iss}	input capacitance	$V_{DS} = 50 \text{ V}$; $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ °C}$; Fig. 16 ; Fig. 17	-	5512	-	pF
C_{oss}	output capacitance	$V_{DS} = 50 \text{ V}$; $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ °C}$; Fig. 16	-	380	-	pF
C_{rss}	reverse transfer capacitance	$V_{DS} = 50 \text{ V}$; $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ °C}$; Fig. 16 ; Fig. 17	-	256	-	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 50 \text{ V}$; $R_L = 2 \text{ } \Omega$; $V_{GS} = 10 \text{ V}$; $R_{G(\text{ext})} = 5 \text{ } \Omega$	-	20	-	ns
t_r	rise time		-	35	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	87	-	ns
t_f	fall time		-	43	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ °C}$; Fig. 18	-	0.82	1.2	V
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}$; $di_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 50 \text{ V}$	-	53	-	ns
Q_r	recovered charge		-	124	-	nC



$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

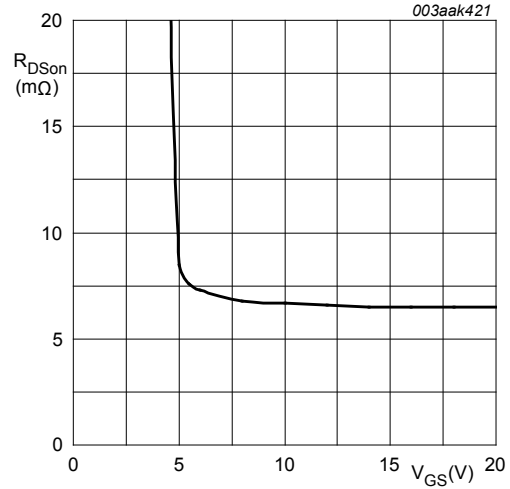


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}$; $I_D = 25\text{ A}$

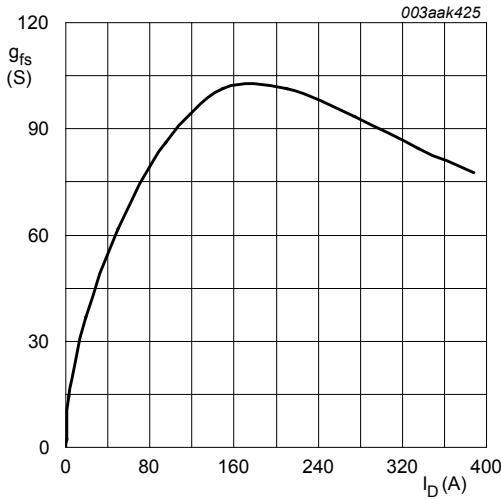


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25\text{ }^\circ\text{C}$; $V_{DS} = 10\text{ V}$

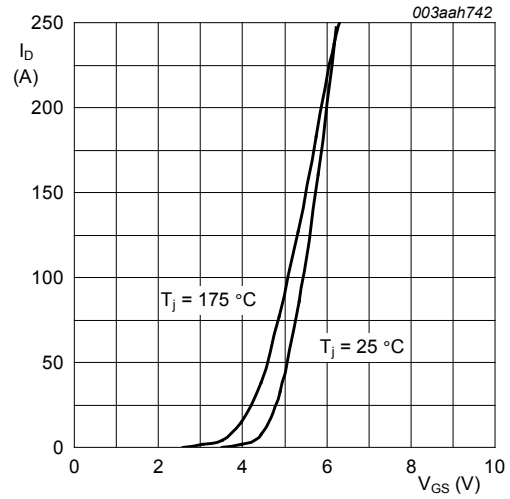


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{ V}$

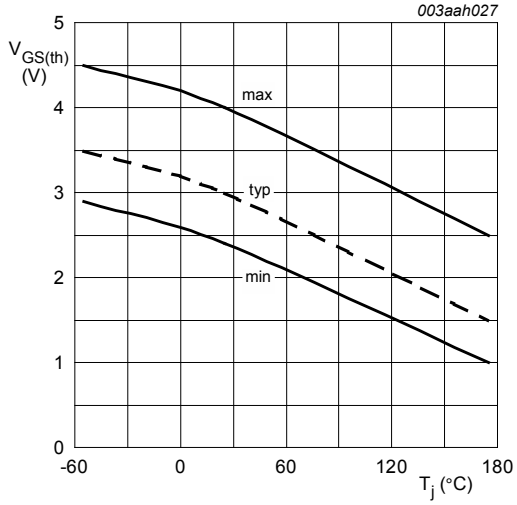


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

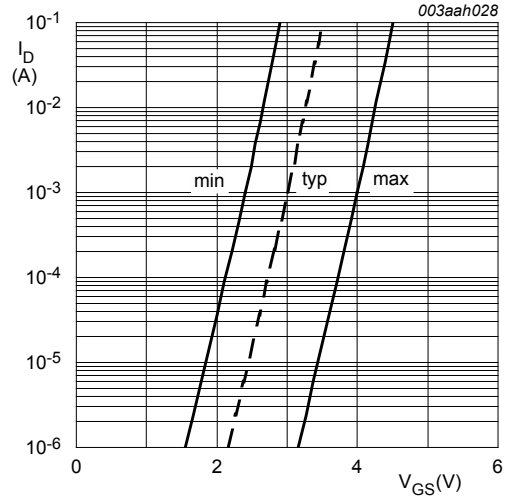


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

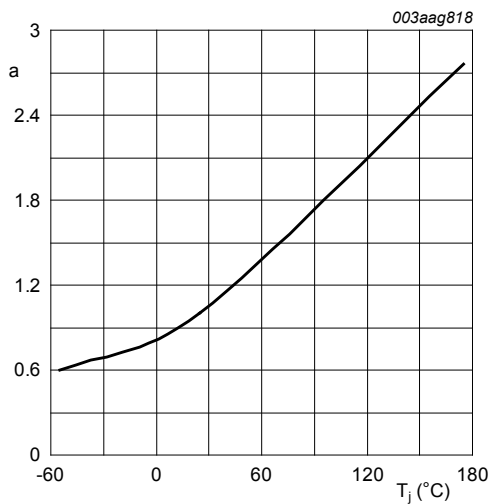


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

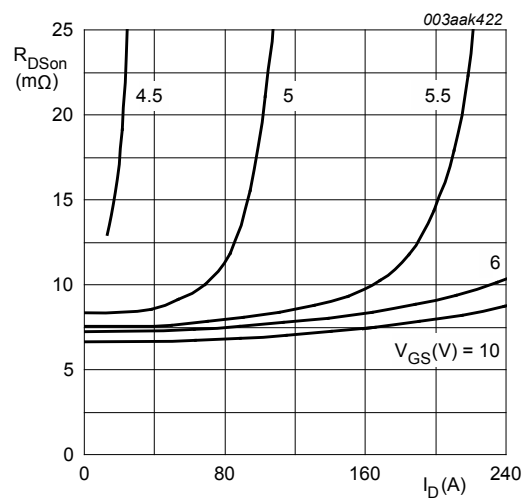


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

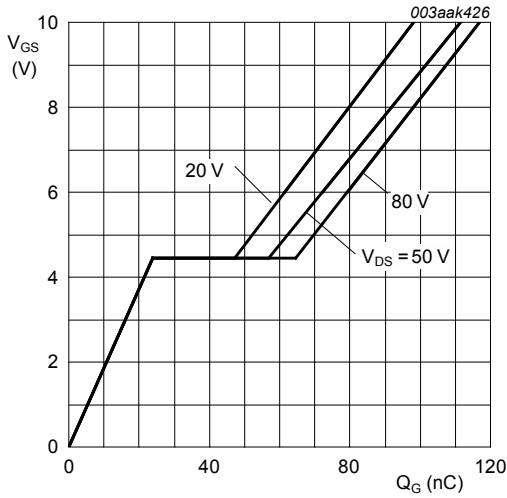


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ C; I_D = 25 A$

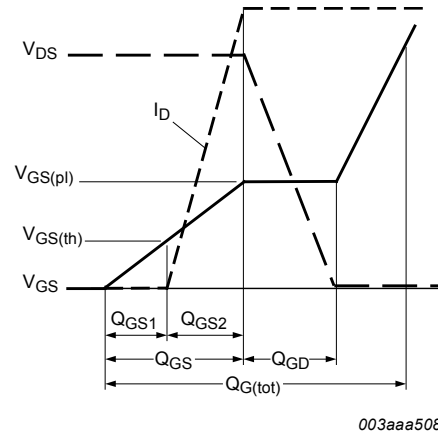


Fig. 15. Gate charge waveform definitions

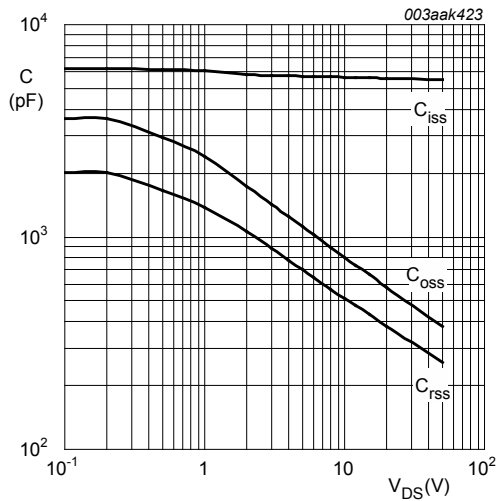


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0 V; f = 1 MHz$

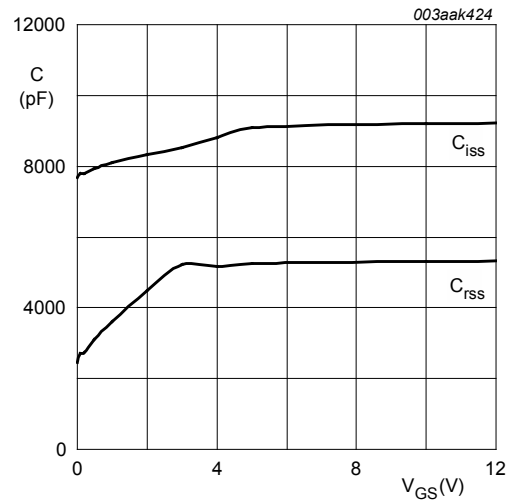


Fig. 17. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

$f = 1 MHz; V_{DS} = 0 V$

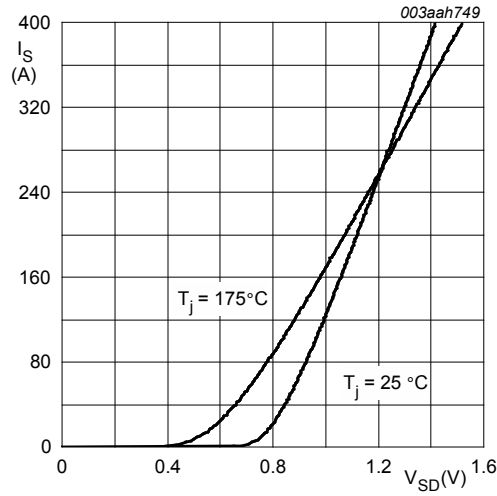


Fig. 18. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

8. Package outline

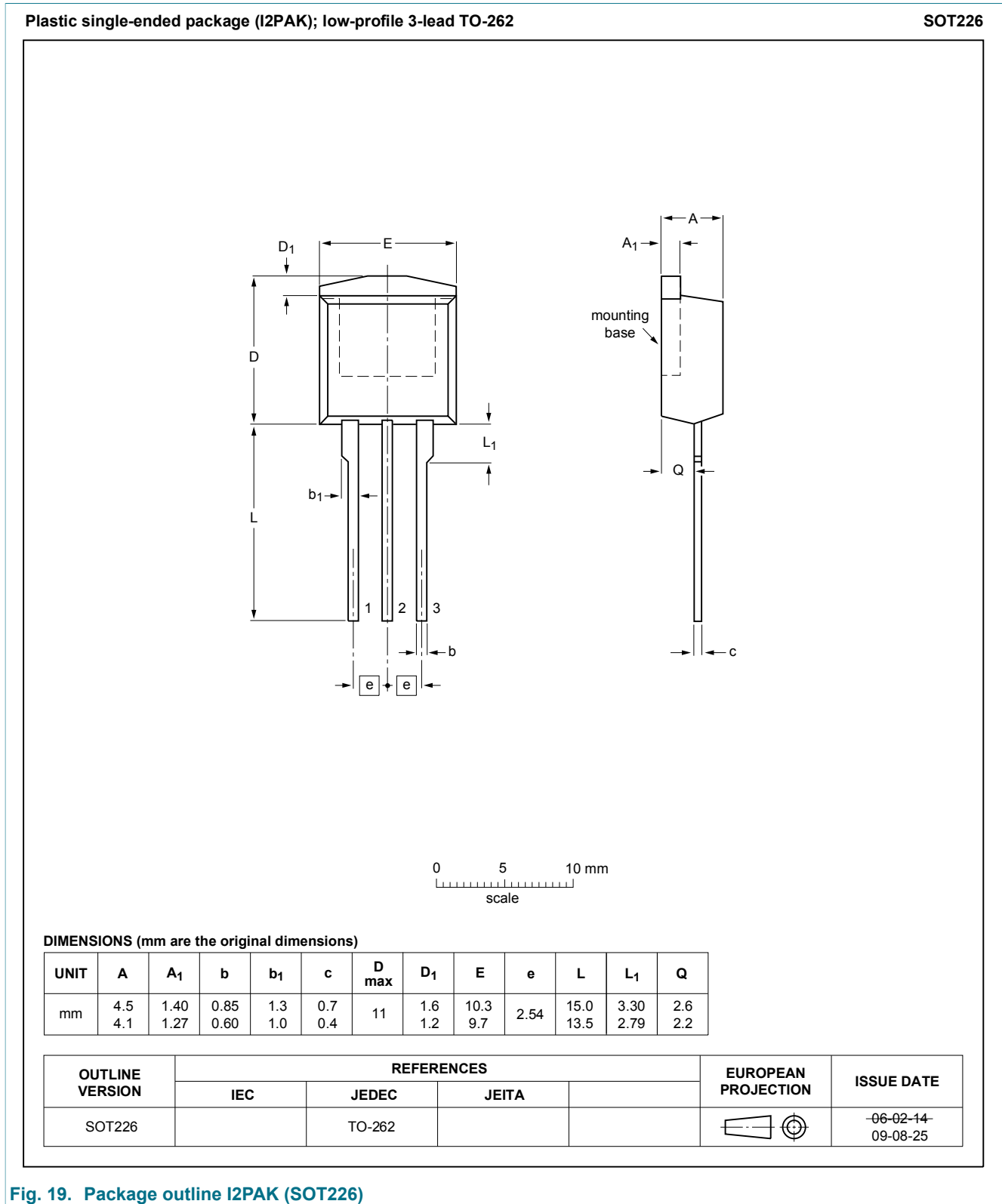


Fig. 19. Package outline I2PAK (SOT226)

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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