

## SNx4HCT245 Octal Bus Transceivers With 3-State Outputs

### 1 Features

- Operating Voltage Range of 4.5 V to 5.5 V
- High-Current 3-State Outputs Drive Bus Lines Directly or up To 15-LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Maximum  $I_{CC}$
- Typical  $t_{pd} = 14$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Maximum
- Inputs Are TTL-Voltage Compatible

### 2 Applications

- Factory Automation and Control
- Grid Infrastructure
- Electronic Point of Sale
- Multi-Function Printers
- Motor Drives
- Storage
- Telecom Infrastructure

### 3 Description

The SNx4HCT245 octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

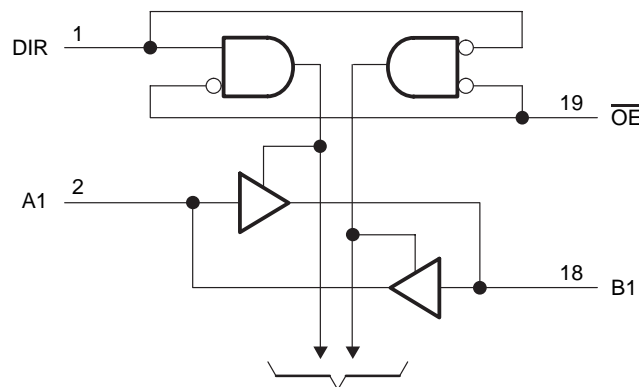
The SNx4HCT245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN54HCT245J	CDIP (20)	24.20 mm $\times$ 6.92 mm
SN54HCT245FK	LCCC (20)	8.89 mm $\times$ 8.89 mm
SN54HCT245W	CFP (20)	13.09 mm $\times$ 6.92 mm
SN74HCT245DW	SOIC (20)	12.80 mm $\times$ 7.50 mm
SN74HCT245N	PDIP (20)	24.33 mm $\times$ 6.35 mm
SN74HCT245NS	SOP (20)	12.60 mm $\times$ 5.30 mm
SN74HCT245PW	TSSOP (20)	6.50 mm $\times$ 4.40 mm
SN74HCT245DB	SSOP (20)	7.80 mm $\times$ 7.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



To Seven Other Channels

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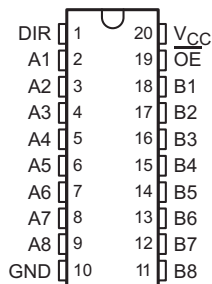
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

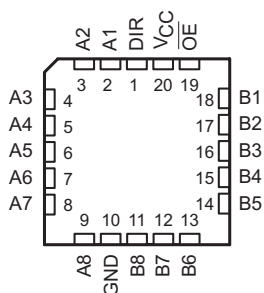
<b>Changes from Revision E (August 2003) to Revision F</b>	<b>Page</b>
• Deleted Ordering Information, see POA at the end of the datasheet. ....	<b>1</b>
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>
• Updated values in the <i>Thermal Information</i> table .....	<b>5</b>

## 5 Pin Configuration and Functions

SN54HCT245 . . . J OR W PACKAGE  
SN74HCT245 . . . DB, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HCT245 . . . FK PACKAGE  
(TOP VIEW)



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	DIR	I	Direction select. High = A to B, Low = B to A
2	A1	I/O	Channel 1 port A
3	A2	I/O	Channel 2 port A
4	A3	I/O	Channel 3 port A
5	A4	I/O	Channel 4 port A
6	A5	I/O	Channel 5 port A
7	A6	I/O	Channel 6 port A
8	A7	I/O	Channel 7 port A
9	A8	I/O	Channel 8 port A
10	GND	—	Ground
11	B8	O/I	Channel 1 port B
12	B7	O/I	Channel 2 port B
13	B6	O/I	Channel 3 port B
14	B5	O/I	Channel 4 port B
15	B4	O/I	Channel 5 port B
16	B3	O/I	Channel 6 port B
17	B2	O/I	Channel 7 port B
18	B1	O/I	Channel 8 port B
19	$\overline{OE}$	I	Output enable, active low. High = all ports in high impedance mode, Low = all ports active
20	V <sub>CC</sub>	—	Power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>		±20 mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±20 mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±35 mA
Continuous current through V <sub>CC</sub> or GND				±70 mA
T <sub>J</sub>	Operating virtual junction temperature			150 °C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1500
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±2000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V		2	V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		V
Δt/Δv	Input transition rise and fall time			500	ns
T <sub>A</sub>	Operating free-air temperature	SN54HCT245	-55	125	°C
		SN74HCT245	-40	85	

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the TI application report, [Implications of Slow or Floating CMOS Inputs](#) (SCBA004).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SNx4HCT245									UNIT
	J (CDIP)	W (CFP)	FK (LCCC)	DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)		
	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	—	—	—	84.6	70.4	43.4	68.9	94.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	38.7	60.8	37.1	44.3	36.5	29.5	34.7	30.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	49.8	100.4	36.1	40.2	38.1	24.3	36.4	45.7	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	—	—	—	11.1	11.3	15	11.6	1.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	—	—	—	39.7	37.7	24.2	36	45.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	11.5	8.5	4.3	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	T <sub>A</sub> = 25°C	4.5 V	4.4	4.499	V	
			SN54HCT245		4.4			
			SN74HCT245		4.4			
		I <sub>OH</sub> = -6 mA	T <sub>A</sub> = 25°C		3.98	4.3		
			SN54HCT245		3.7			
			SN74HCT245		3.84			
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	T <sub>A</sub> = 25°C	4.5 V	0.001	0.1	V	
			SN54HCT245		0.1			
			SN74HCT245		0.1			
		I <sub>OL</sub> = 6 mA	T <sub>A</sub> = 25°C		0.17	0.26		
			SN54HCT245		0.4			
			SN74HCT245		0.33			
I <sub>I</sub>	DIR or $\overline{\text{OE}}$	V <sub>I</sub> = V <sub>CC</sub> or 0	T <sub>A</sub> = 25°C	5.5 V	±0.1	±100	nA	
			SN54HCT245		±1000			
			SN74HCT245		±1000			
I <sub>OZ</sub>	A or B	V <sub>O</sub> = V <sub>CC</sub> or 0	T <sub>A</sub> = 25°C	5.5 V	±0.01	±0.5	μA	
			SN54HCT245		±10			
			SN74HCT245		±5			
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0,	I <sub>O</sub> = 0	T <sub>A</sub> = 25°C	5.5 V	8	μA		
			SN54HCT245		160			
			SN74HCT245		80			
ΔI <sub>CC</sub> <sup>(1)</sup>	One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>	T <sub>A</sub> = 25°C	5.5 V	1.4	2.4	mA		
				SN54HCT245	3			
				SN74HCT245	2.9			
C <sub>i</sub> <sup>(2)</sup>	DIR or $\overline{\text{OE}}$	T <sub>A</sub> = 25°C	4.5 V to 5.5 V	3	10	pF		
				SN54HCT245	10			
				SN74HCT245	10			

(1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

(2) Parameter C<sub>i</sub> does not apply to transceiver I/O ports.

**SN54HCT245, SN74HCT245**

SCLS020F – MARCH 1984 – REVISED AUGUST 2016

[www.ti.com](http://www.ti.com)
**6.6 Switching Characteristics:  $C_L = 50$  pF**

 over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>pd</sub>	A or B	B or A	4.5 V	T <sub>A</sub> = 25°C		16	22	ns
				SN54HCT245			33	
				SN74HCT245			28	
			5.5 V	T <sub>A</sub> = 25°C		14	20	
				SN54HCT245			30	
				SN74HCT245			25	
t <sub>en</sub>	$\overline{OE}$	A or B	4.5 V	T <sub>A</sub> = 25°C		25	46	ns
				SN54HCT245			69	
				SN74HCT245			58	
			5.5 V	T <sub>A</sub> = 25°C		22	41	
				SN54HCT245			62	
				SN74HCT245			52	
t <sub>dis</sub>	$\overline{OE}$	A or B	4.5 V	T <sub>A</sub> = 25°C		26	40	ns
				SN54HCT245			60	
				SN74HCT245			50	
			5.5 V	T <sub>A</sub> = 25°C		23	36	
				SN54HCT245			54	
				SN74HCT245			45	
t <sub>t</sub>		A or B	4.5 V	T <sub>A</sub> = 25°C		9	12	ns
				SN54HCT245			18	
				SN74HCT245			15	
			5.5 V	T <sub>A</sub> = 25°C		8	11	
				SN54HCT245			16	
				SN74HCT245			14	

### 6.7 Switching Characteristics: $C_L = 150 \text{ pF}$

over recommended operating free-air temperature range,  $C_L = 150 \text{ pF}$  (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd}$	A or B	B or A	4.5 V	$T_A = 25^\circ\text{C}$		20	30	ns
				SN54HCT245			45	
				SN74HCT245			38	
			5.5 V	$T_A = 25^\circ\text{C}$		18	27	
				SN54HCT245			41	
				SN74HCT245			34	
$t_{en}$	$\overline{\text{OE}}$	A or B	4.5 V	$T_A = 25^\circ\text{C}$		36	59	ns
				SN54HCT245			89	
				SN74HCT245			74	
			5.5 V	$T_A = 25^\circ\text{C}$		30	53	
				SN54HCT245			80	
				SN74HCT245			67	
$t_t$		A or B	4.5 V	$T_A = 25^\circ\text{C}$		17	42	ns
				SN54HCT245			63	
				SN74HCT245			53	
			5.5 V	$T_A = 25^\circ\text{C}$		14	38	
				SN54HCT245			57	
				SN74HCT245			48	

### 6.8 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per transceiver	No load	40	pF

### 6.9 Typical Characteristics

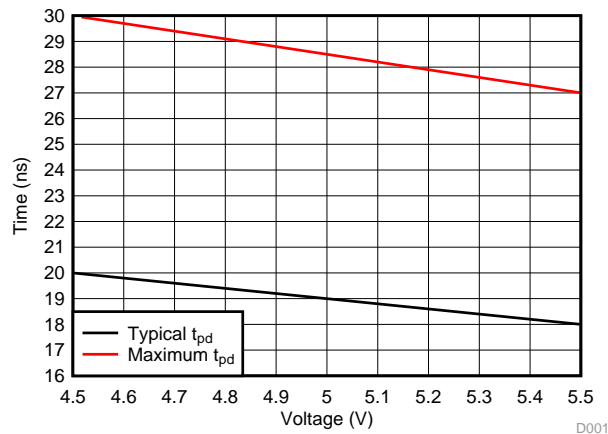
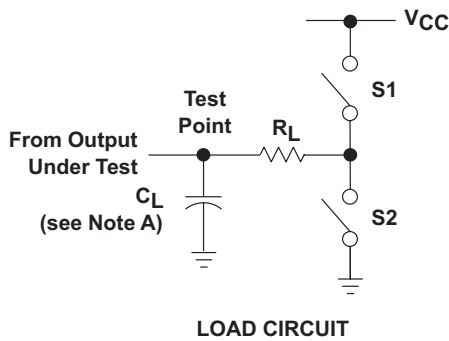
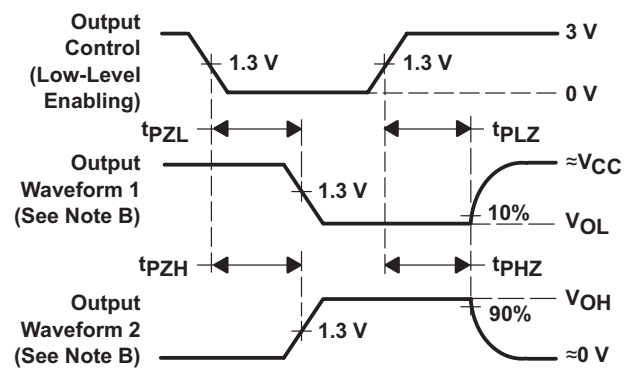
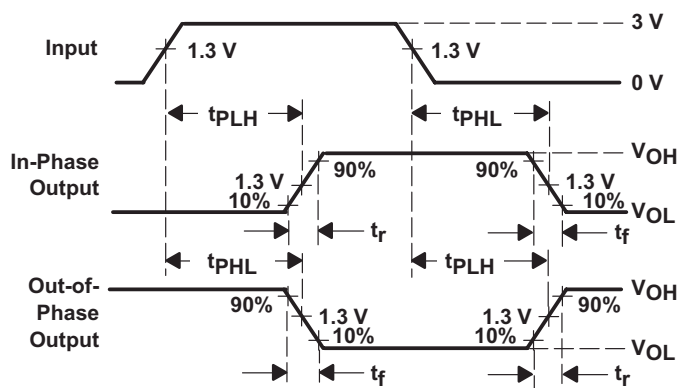
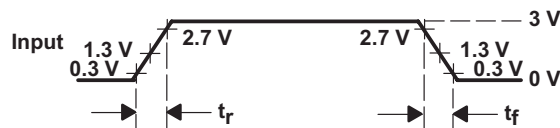


Figure 1. Propagation Delay Over Operating Voltage Range,  $T_A = 25^\circ\text{C}$

## 7 Parameter Measurement Information



PARAMETER		$R_L$	$C_L$	S1	S2
$t_{en}$	$t_{pZH}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
	$t_{pZL}$			Closed	Open
$t_{dis}$	$t_{pHZ}$	1 k $\Omega$	50 pF	Open	Closed
	$t_{pLZ}$			Closed	Open
$t_{pd}$ or $t_t$		—	50 pF or 150 pF	Open	Open



**PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES**

**ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS**

- A.  $C_L$  includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E.  $t_{pLZ}$  and  $t_{pHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{pZL}$  and  $t_{pZH}$  are the same as  $t_{en}$ .
- G.  $t_{pLH}$  and  $t_{pHL}$  are the same as  $t_{pd}$ .

**Figure 2. Load Circuit and Voltage Waveforms**

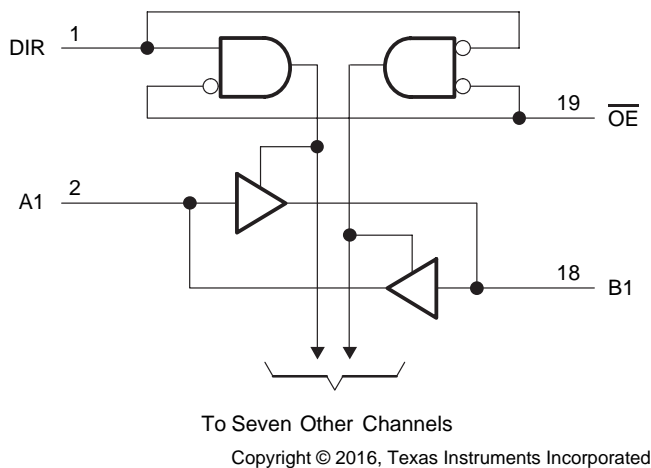


## 8 Detailed Description

### 8.1 Overview

The SNx4HCT245 is a bidirectional buffer with direction control and active low output enable. This device is commonly used in logic systems for isolation and increasing drive strength.

### 8.2 Functional Block Diagram



**Figure 3. Logic Diagram (Positive Logic)**

### 8.3 Feature Description

Voltage operating range from 4.5 V to 5.5 V is forgiving of 5-V power supply rail accuracy. Outputs can operate up to 15 LSTTL loads. This device has balanced propagation delay, typically 14 ns, and balanced output drive of  $\pm 6$  mA at 5 V. It has low power consumption of only 80- $\mu$ A maximum static supply current. The center  $V_{CC}$  and GND pin configurations minimize high-speed switching noise. Inputs are TTL-voltage compatible.

### 8.4 Device Functional Modes

This device is a standard '245 logic function. It has an active low output enable, a direction pin, and eight communication channels.

**Table 1. Function Table**

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## 9 Application and Implementation

### NOTE

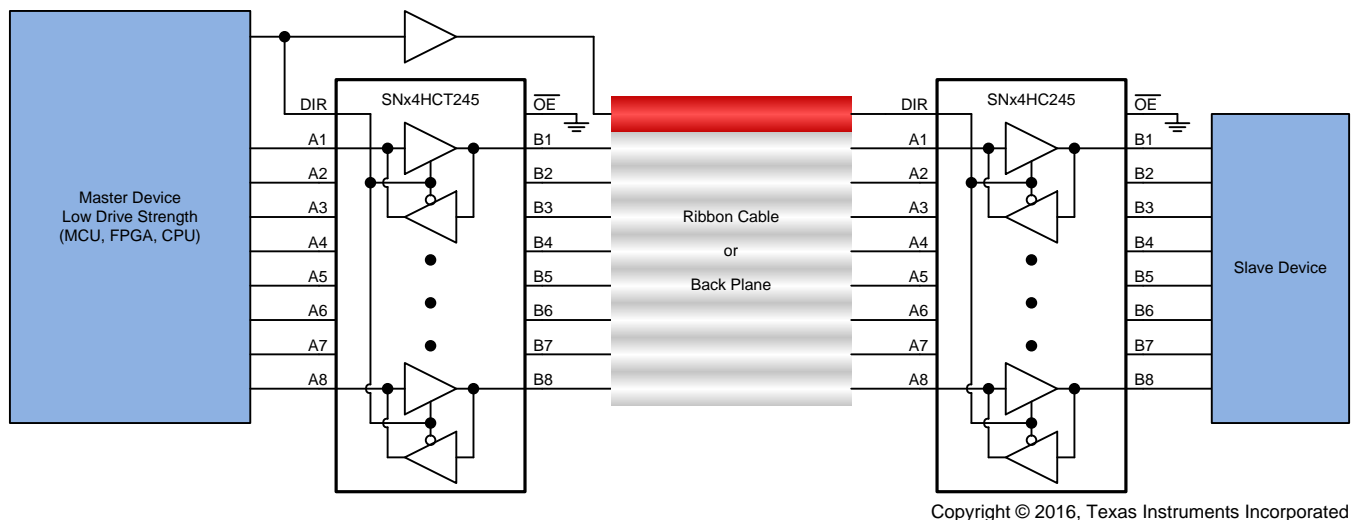
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SNx4HCT245 is a versatile device with many available applications. The application chosen as an example here is connecting a master and slave device through a ribbon cable. This configuration is common due to losses in this type of cable.

### 9.2 Typical Application

Logic transceivers are commonly seen in back plane and ribbon cable applications where a signal direct from an FPGA or MCU would be too weak to reach the distant end. The transceiver acts as an amplifier to get the signal across the line, and since it is bidirectional, data can be sent from master to slave or slave to master. The additional buffer on the direction line is necessary to ensure the direction signal can always reach the distant end.



**Figure 4. Typical application for SNx4HC245**

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care must be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive, but the high drive also creates faster edges into light loads, so routing and load conditions must be considered to prevent ringing.

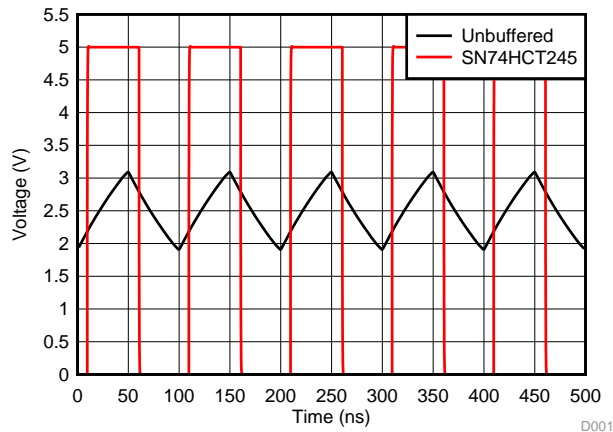
#### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - Rise time and fall time specs: See ( $\Delta t/\Delta V$ ) in the [Recommended Operating Conditions](#).
  - Specified high and low levels: See ( $V_{IH}$  and  $V_{IL}$ ) in the [Recommended Operating Conditions](#).
2. Recommended Output Conditions
  - Load currents should not exceed 35 mA per output and 70 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

**Typical Application (continued)**

**9.2.3 Application Curve**

It is common to see significant losses in ribbon cables and back planes. The plot shown in [Figure 5](#) is a simplified simulation of a ribbon cable from a 5-V, 10-MHz low drive strength source. It shows the difference between an input signal from a weak driver like an MCU or FPGA compared to a strong driver like the SN74HCT245 when measured at the distant end of the cable. By adding a high-current drive transceiver before the cable, the signal strength can be significantly improved, and subsequently the cable can be longer.



Unbuffered line is directly connected to low current source, SN74HCT245 line is buffered through the transceiver. Both signals are measured at the distant end of the ribbon cable.

**Figure 5. Simulated Outputs From Ribbon Cable With a 5-V, 10-MHz Source**

## 10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#). Each  $V_{CC}$  pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and a 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

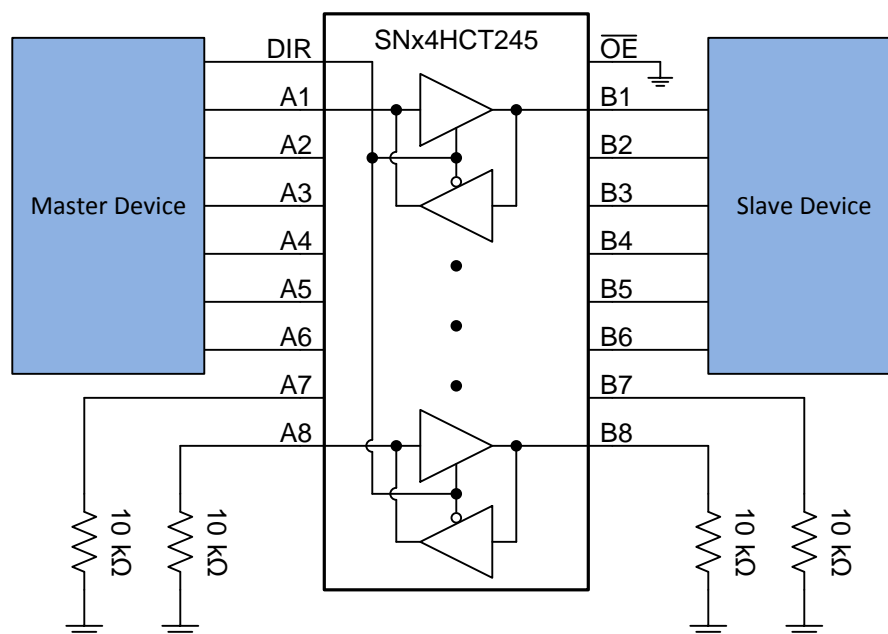
When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only six channels of an eight channel transceiver are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient.

The output enable pin disables the output section of the part when asserted. This does not disable the input section of the IOs, so they cannot float when disabled.

[Figure 6](#) shows the proper method to terminate unused channels using a large resistance (in this example, 10-k $\Omega$  resistors). This avoids overloading the outputs, and maintains a valid voltage on the inputs. Note that it is also valid to tie both sides of an unused transceiver directly to ground or  $V_{CC}$ ; however, the two sides must never be tied to different states directly.

### 11.2 Layout Example



**Figure 6. Proper Termination of  $\overline{\text{OE}}$  Pin And Unused Channels 7 and 8**

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#) (SCBA004)

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HCT245	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74HCT245	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8550601VRA	ACTIVE	CDIP	J	20	20	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8550601VR A SNV54HCT245J	<a href="#">Samples</a>
5962-8550601VSA	ACTIVE	CFP	W	20	25	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8550601VS A SNV54HCT245W	<a href="#">Samples</a>
85506012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	85506012A SNJ54HCT 245FK	<a href="#">Samples</a>
8550601RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8550601RA SNJ54HCT245J	<a href="#">Samples</a>
JM38510/65553BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 65553BRA	<a href="#">Samples</a>
JM38510/65553BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 65553BSA	<a href="#">Samples</a>
M38510/65553BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 65553BRA	<a href="#">Samples</a>
M38510/65553BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 65553BSA	<a href="#">Samples</a>
SN54HCT245J	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54HCT245J	<a href="#">Samples</a>
SN74HCT245DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT245	<a href="#">Samples</a>
SN74HCT245DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT245	<a href="#">Samples</a>
SN74HCT245DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT245	<a href="#">Samples</a>
SN74HCT245DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT245	<a href="#">Samples</a>
SN74HCT245DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT245	<a href="#">Samples</a>
SN74HCT245DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT245	<a href="#">Samples</a>
SN74HCT245DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT245	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT245N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT245N	<a href="#">Samples</a>
SN74HCT245NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT245N	<a href="#">Samples</a>
SN74HCT245NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT245	<a href="#">Samples</a>
SN74HCT245PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT245	<a href="#">Samples</a>
SN74HCT245PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT245	<a href="#">Samples</a>
SN74HCT245PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HT245	<a href="#">Samples</a>
SN74HCT245PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT245	<a href="#">Samples</a>
SN74HCT245PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT245	<a href="#">Samples</a>
SN74HCT245PWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT245	<a href="#">Samples</a>
SNJ54HCT245FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	85506012A SNJ54HCT 245FK	<a href="#">Samples</a>
SNJ54HCT245J	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8550601RA SNJ54HCT245J	<a href="#">Samples</a>
SNJ54HCT245W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ54HCT245W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

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**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54HCT245, SN54HCT245-SP, SN74HCT245 :**

● Catalog: [SN74HCT245](#), [SN54HCT245](#)

● Military: [SN54HCT245](#)

● Space: [SN54HCT245-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HCT245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HCT245NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HCT245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74HCT245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HCT245PWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

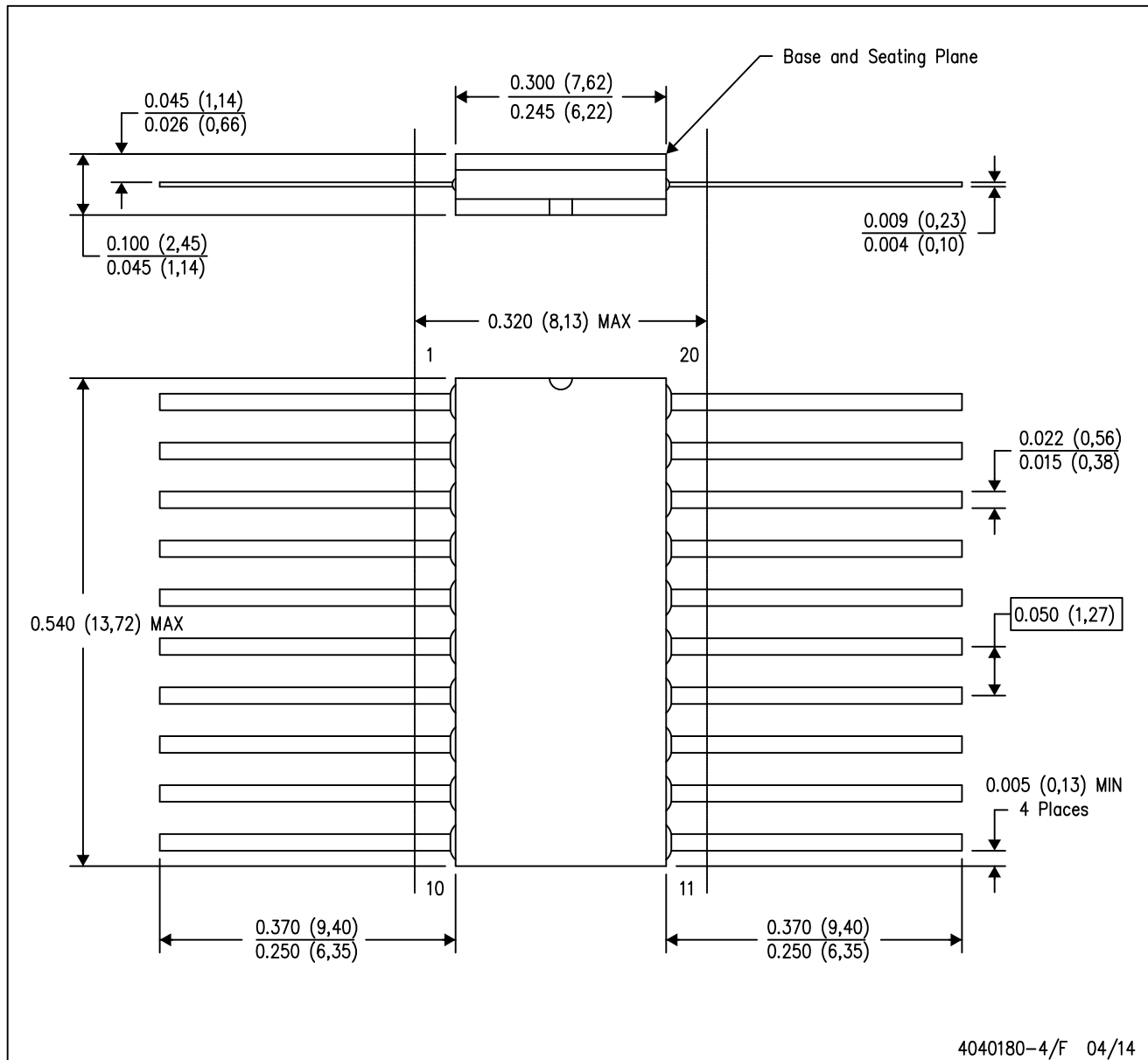
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT245DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74HCT245DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HCT245NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HCT245PWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74HCT245PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74HCT245PWT	TSSOP	PW	20	250	367.0	367.0	38.0

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



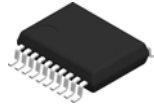
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

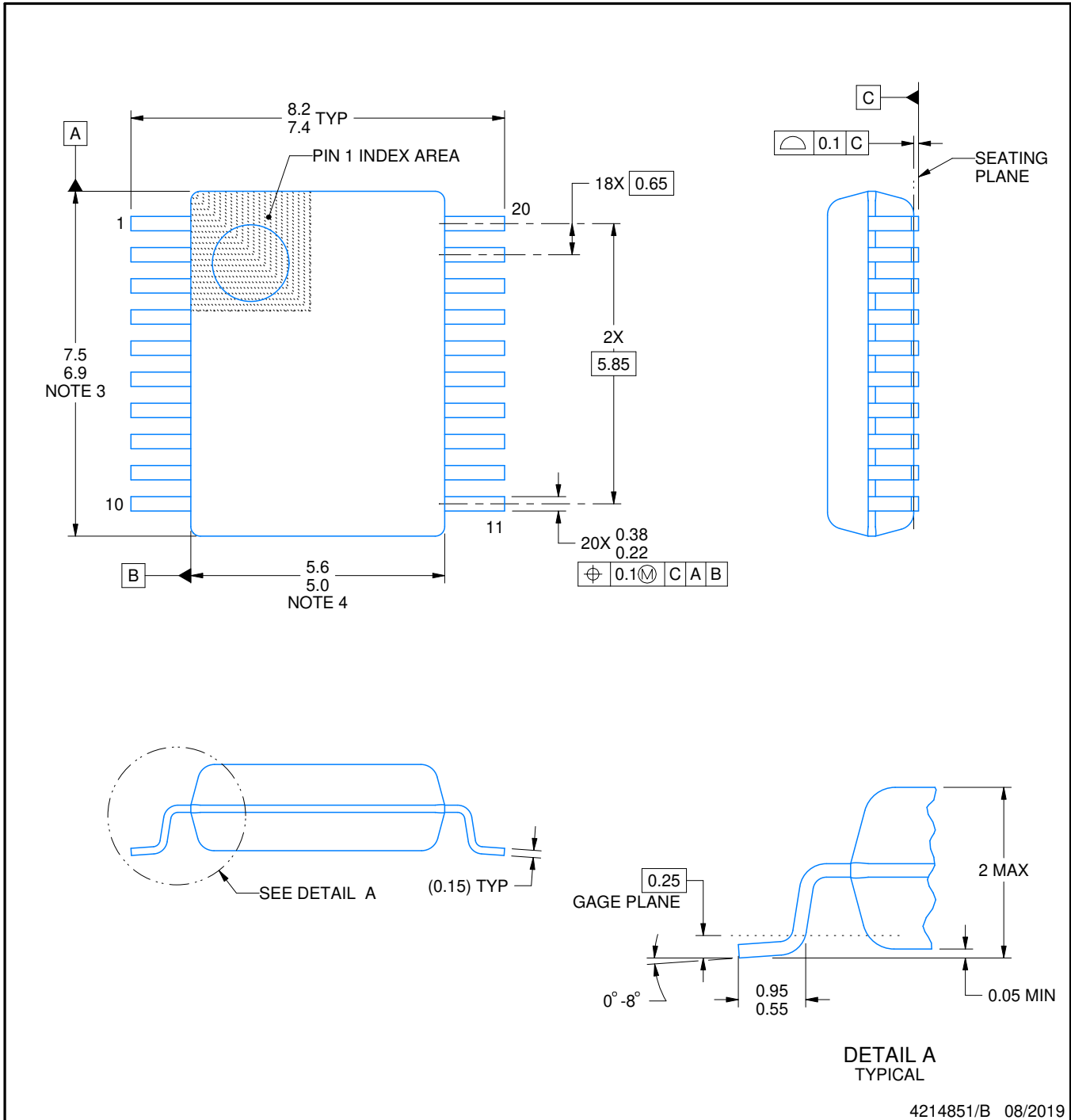
# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

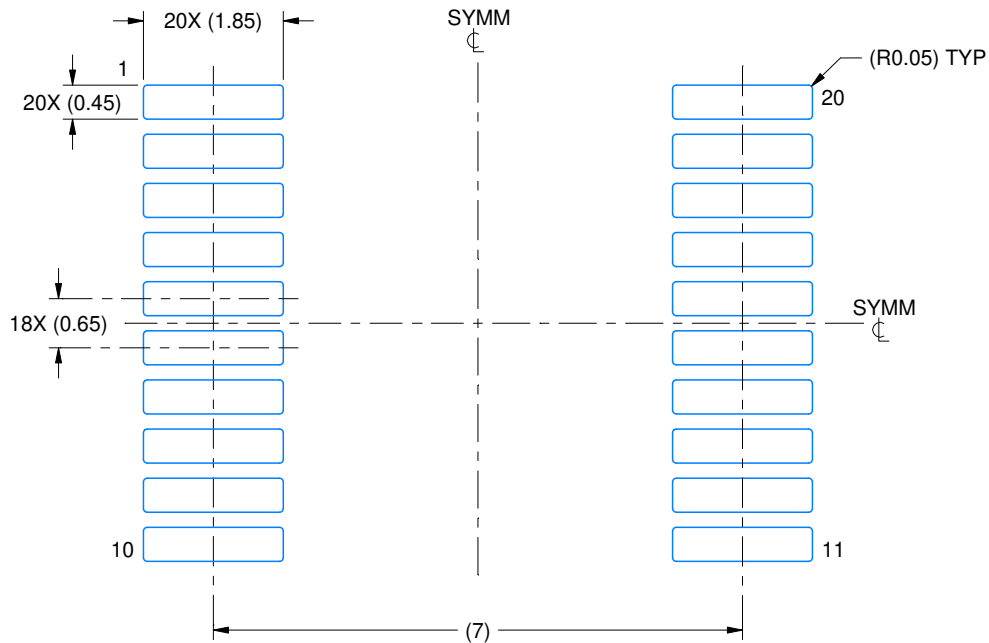
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

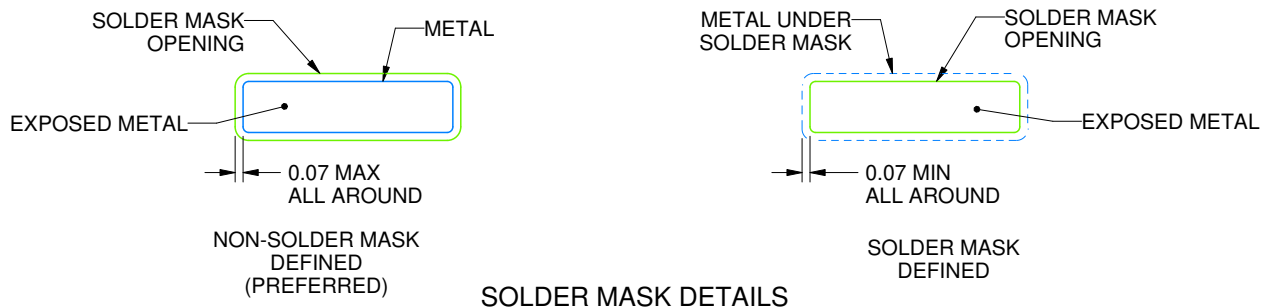
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

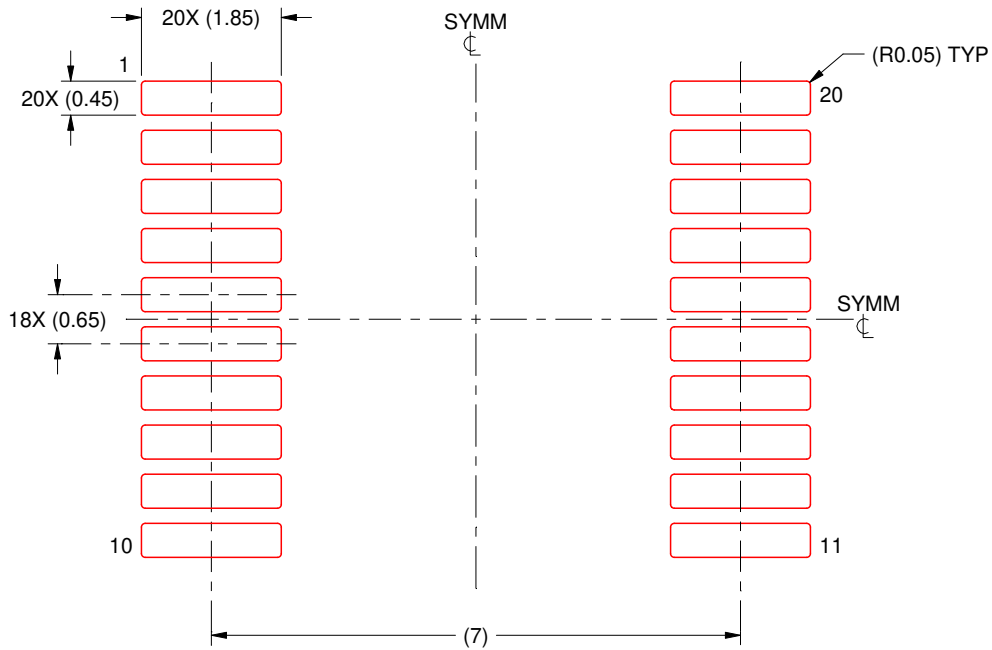
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

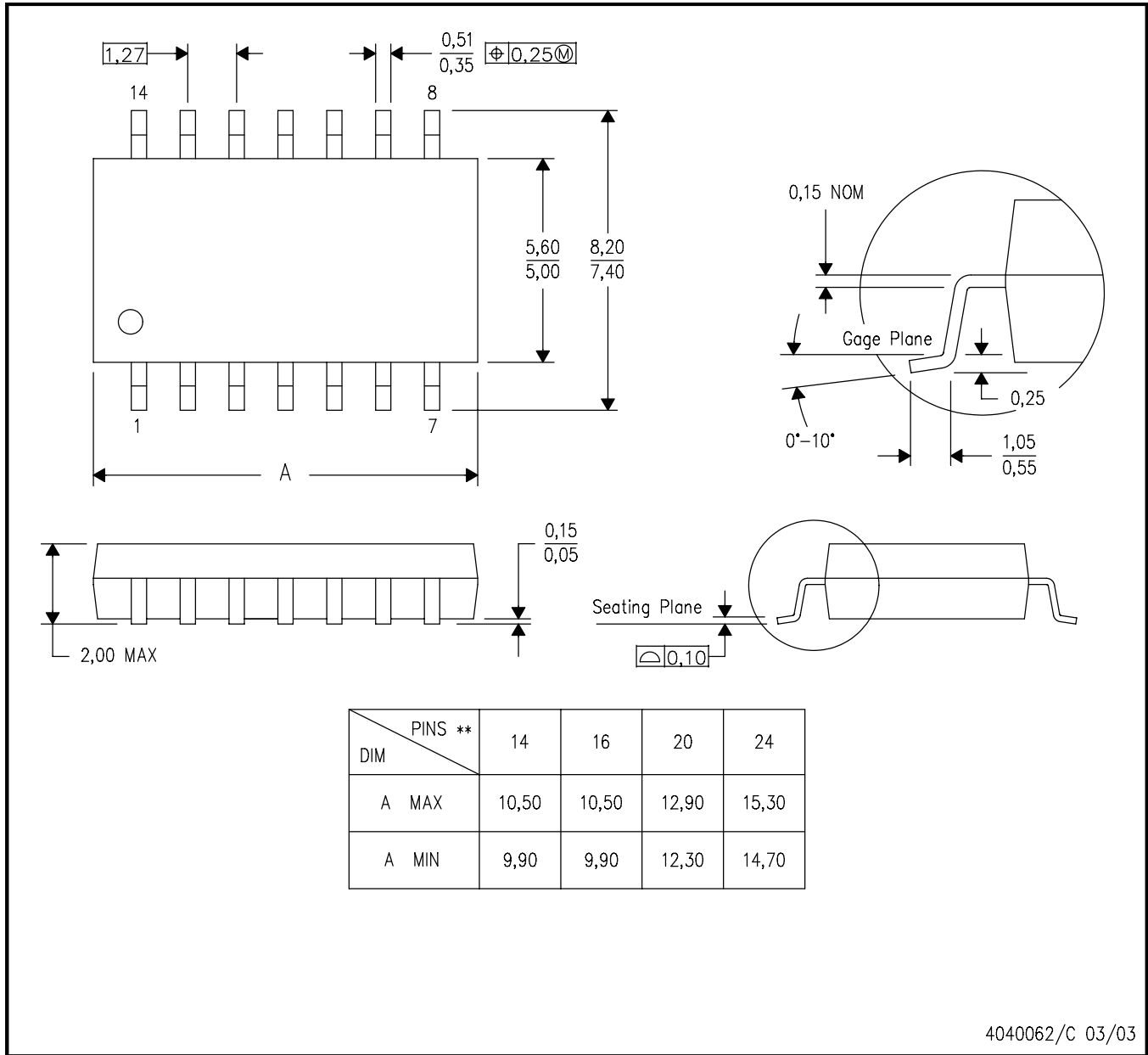
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



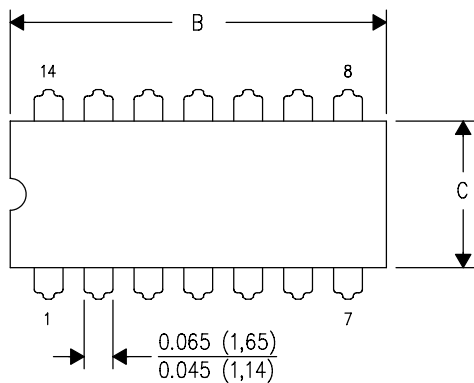
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



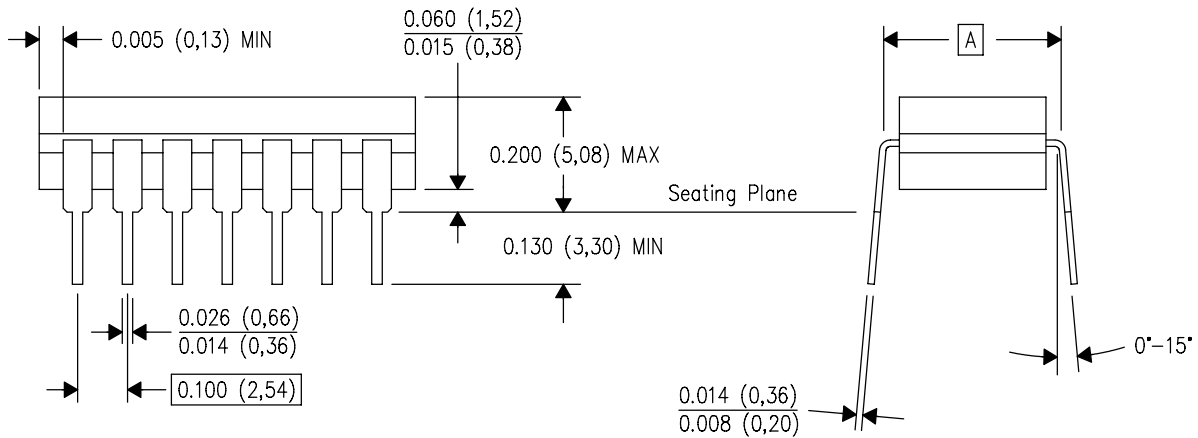
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

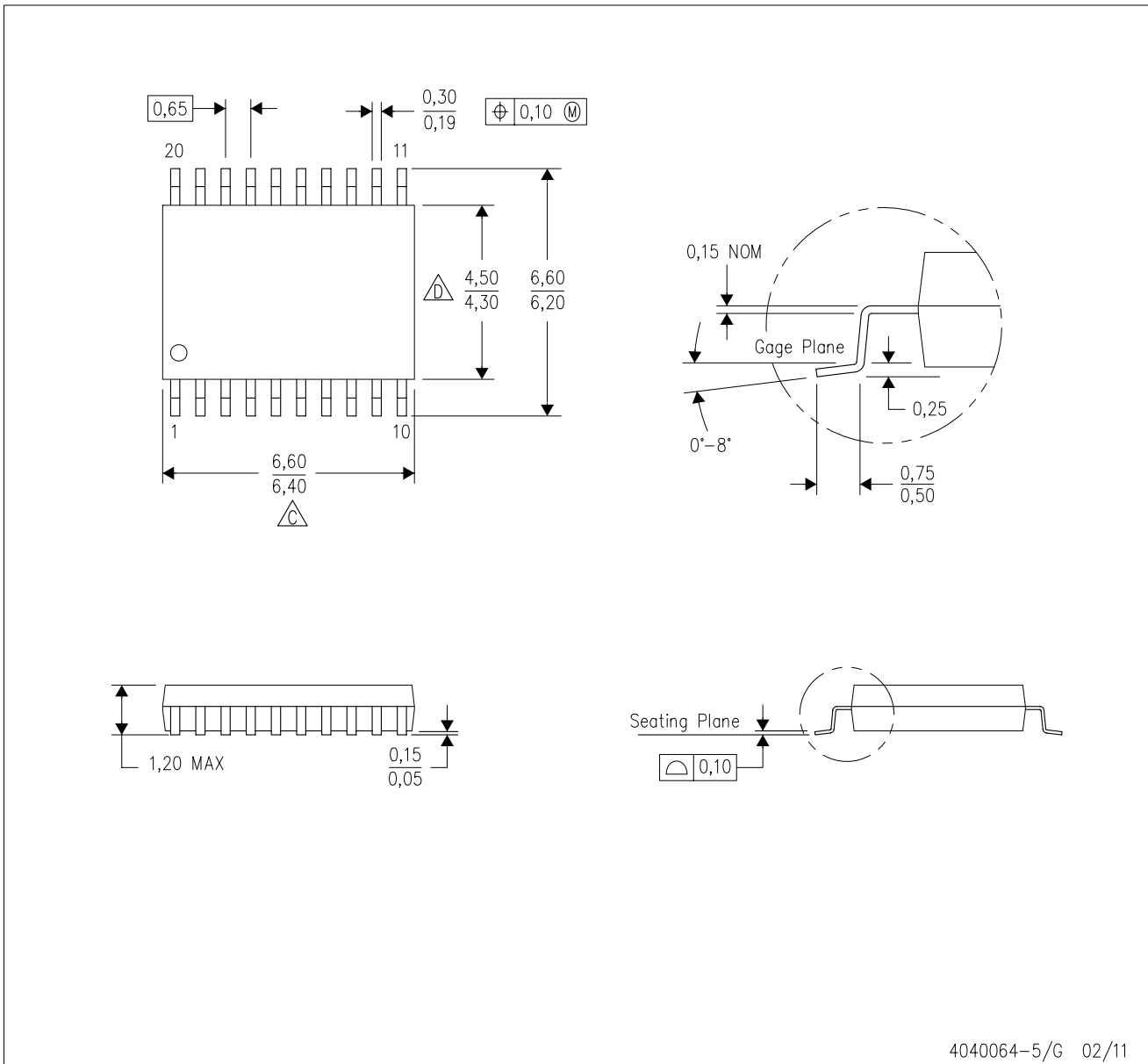


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

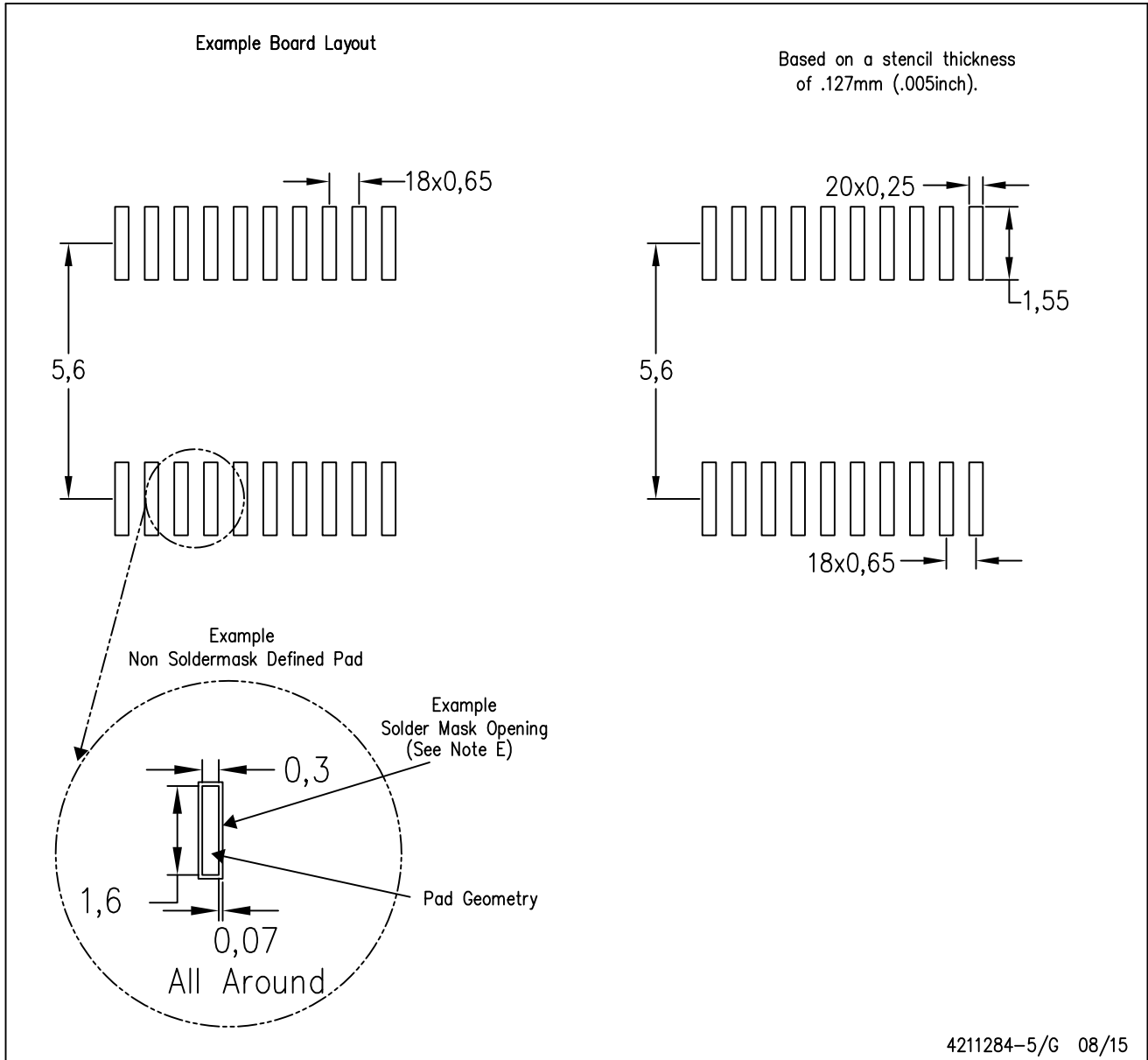


4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

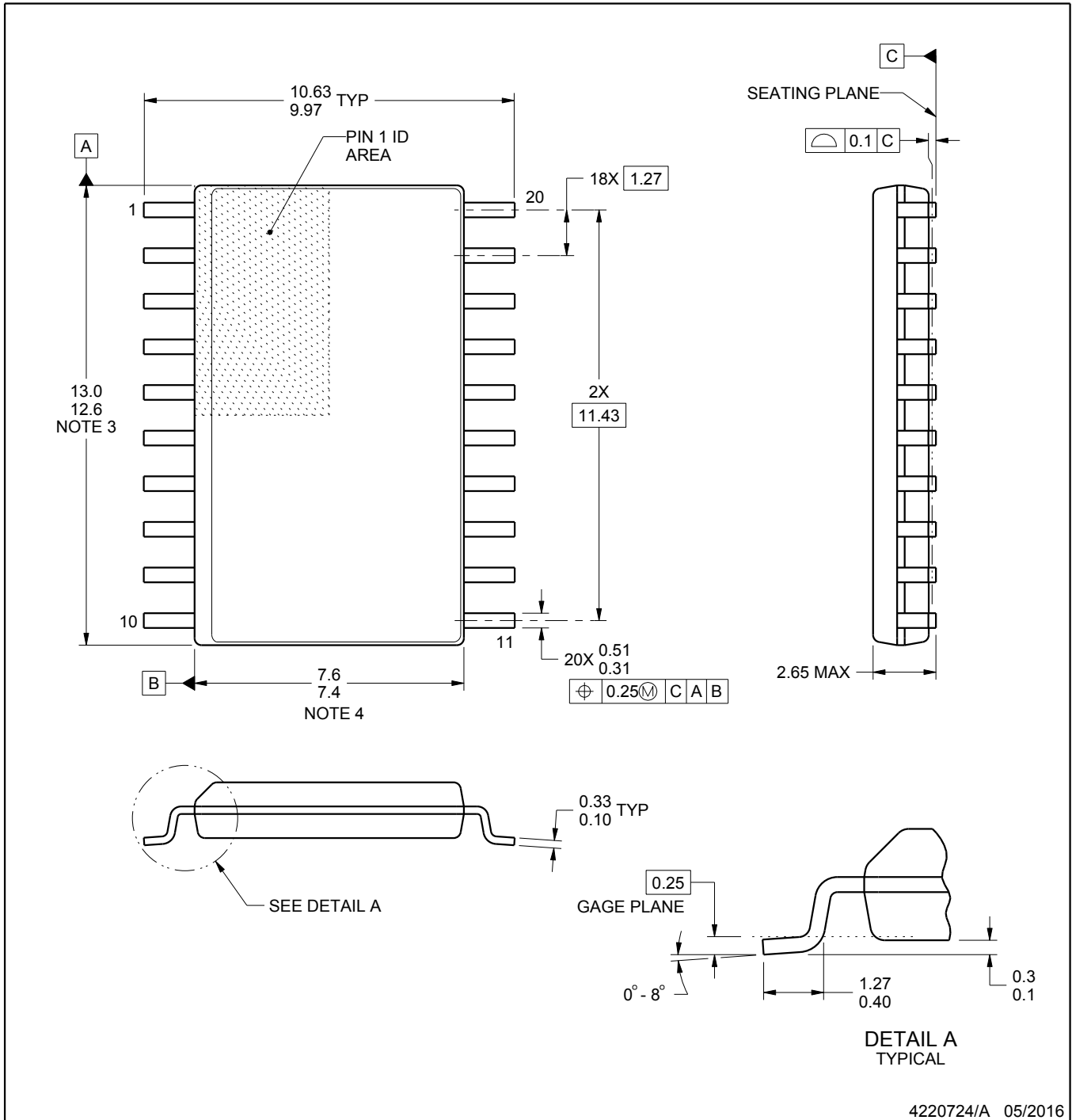
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

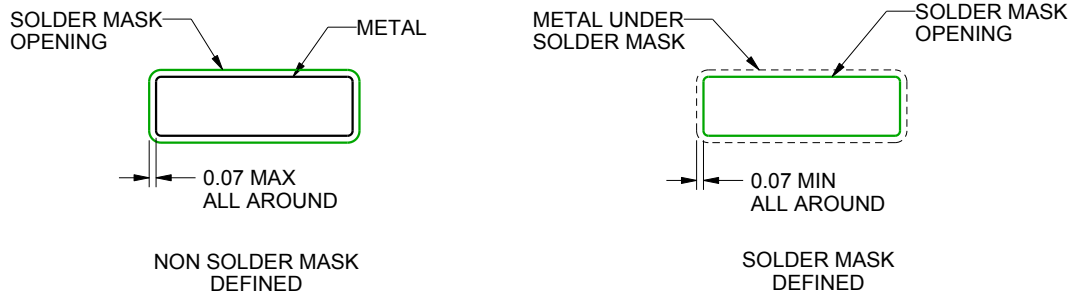
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

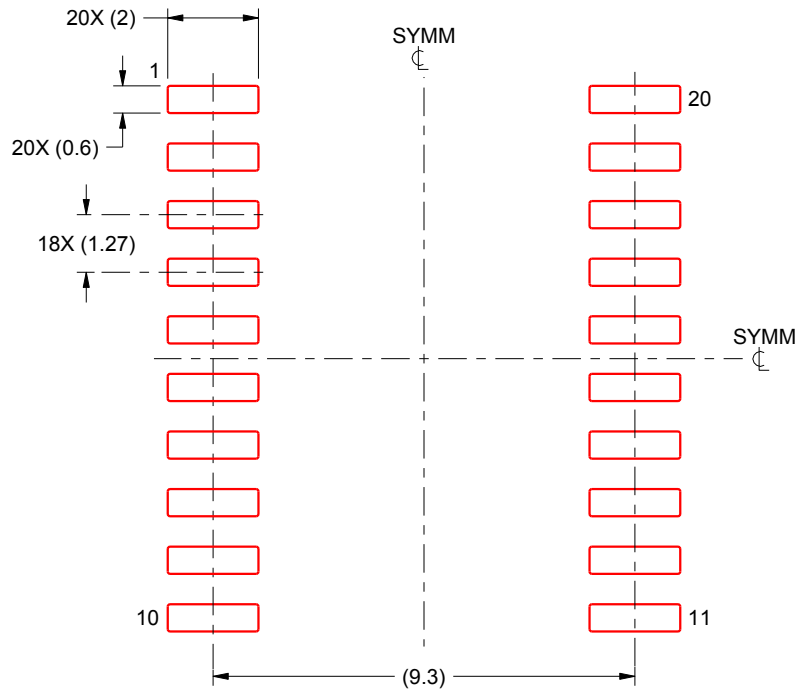
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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