S72XS-R MCP

256 Mb (16M x 16 bit), 1.8V MirrorBit® Flash and DDR DRAM

Features

- Power supply voltage
  - 1.7V to 1.95V
- Burst speed
  - Flash = 83 MHz, 104 MHz or 108 MHz
  - DDR DRAM = 166 MHz
- Packages
  - 8.0 × 8.0 mm, 133-ball MCP
- Temperature range
  - Wireless: –25 °C to +85 °C
  - Industrial: –40 °C to +85 °C

General Description

This datasheet contains information on the S72XS-R Multi-Chip Product (MCP) stacked products. Refer to the S29VS256R, S29VS128R, S29XS256R, S29XS128R datasheet (002-00833) for full electrical specifications of the Flash memory component.

The S72XS series is a product line of stacked products (MCPs), and consists of:

- S29XS family Address-High, Address-Low, Data Multiplexed Flash memory die
- DDR DRAM

Table 1 and Table 2 lists the products covered in this datasheet.

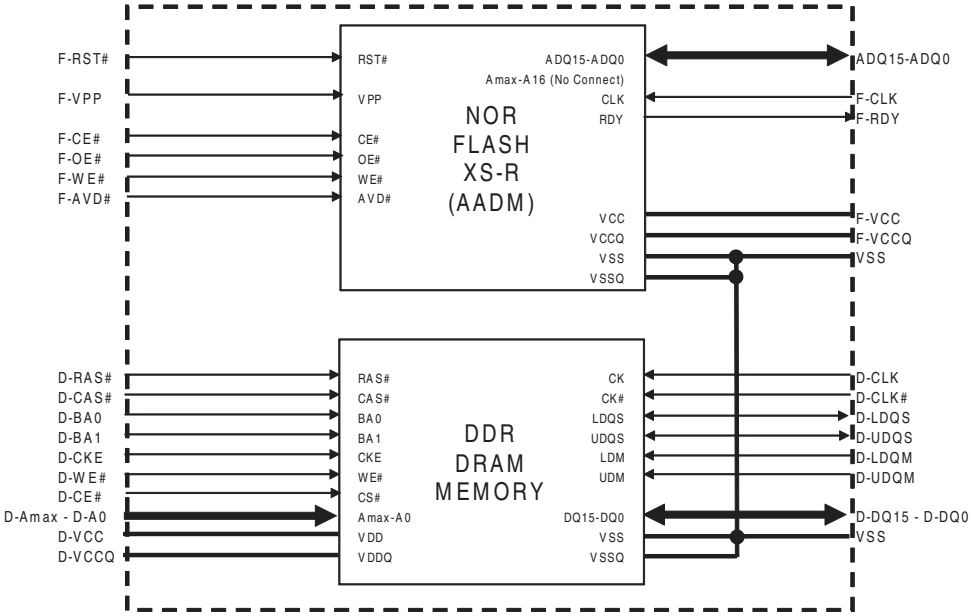
Table 1. Memory Density

Flash Density	DRAM Density
256 Mb	S72XS256RE0

Table 2. DDR DRAM Specification Reference

Density	Reference Name	Document Identification Number
256 Mb	256 Mb (16M × 16-bit) DDR DRAM	SDM256D166D1R/D3R

Block Diagram



Notes
1. Amax indicates highest address bit for memory component: Amax = A12 for 256 Mb DDR DRAM.
2. For Flash, A15 - A0 is tied to DQ15 - DQ0.

Pin Diagram

Figure 1. 133-Ball Fine-Pitch Ball Grid Array MCP

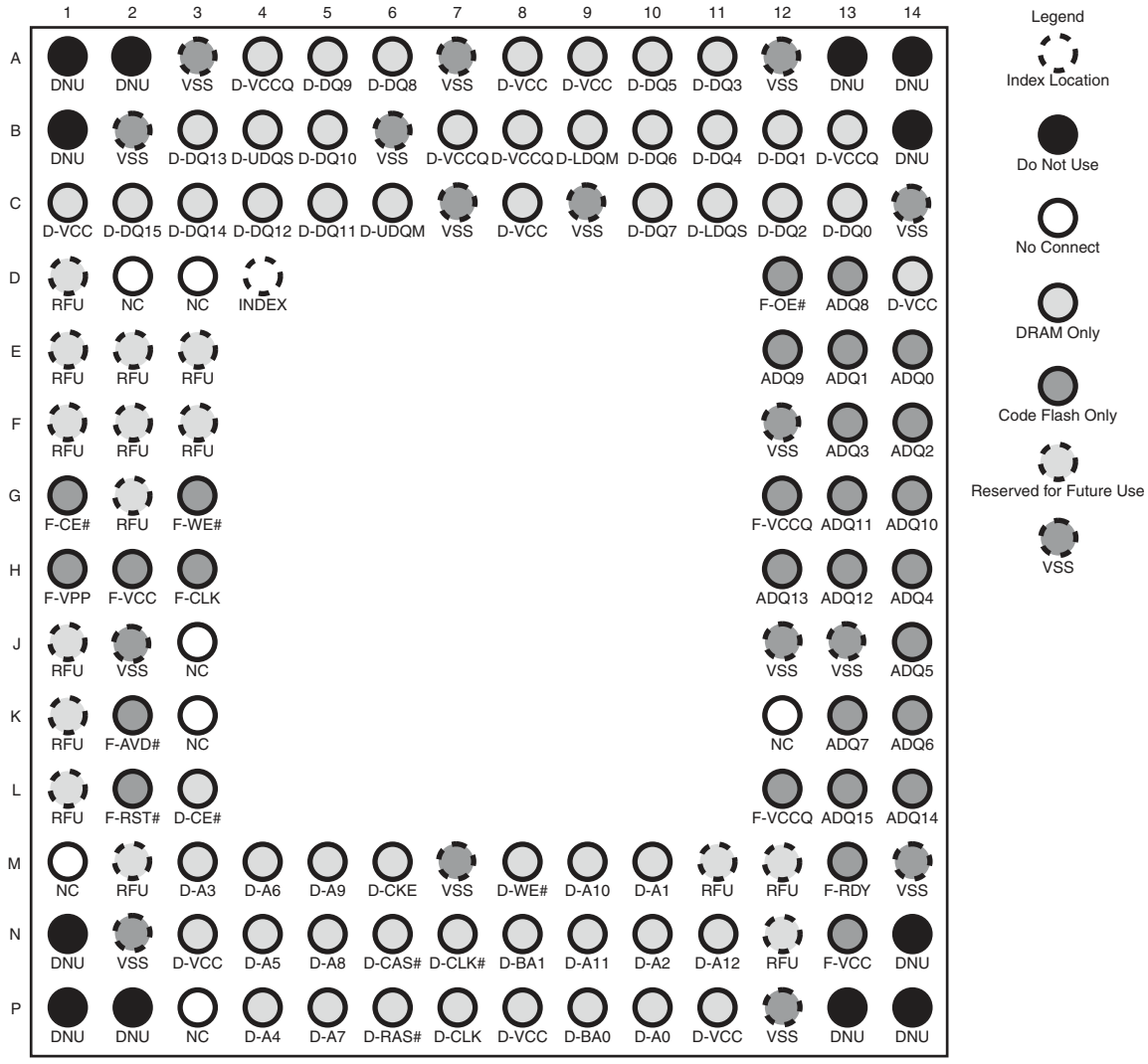


Table 3. DRAM Address Maximum

MCP Device ID	DDR DRAM Density	D-Amax
S72XS256RE0	256 Mb	D-A12

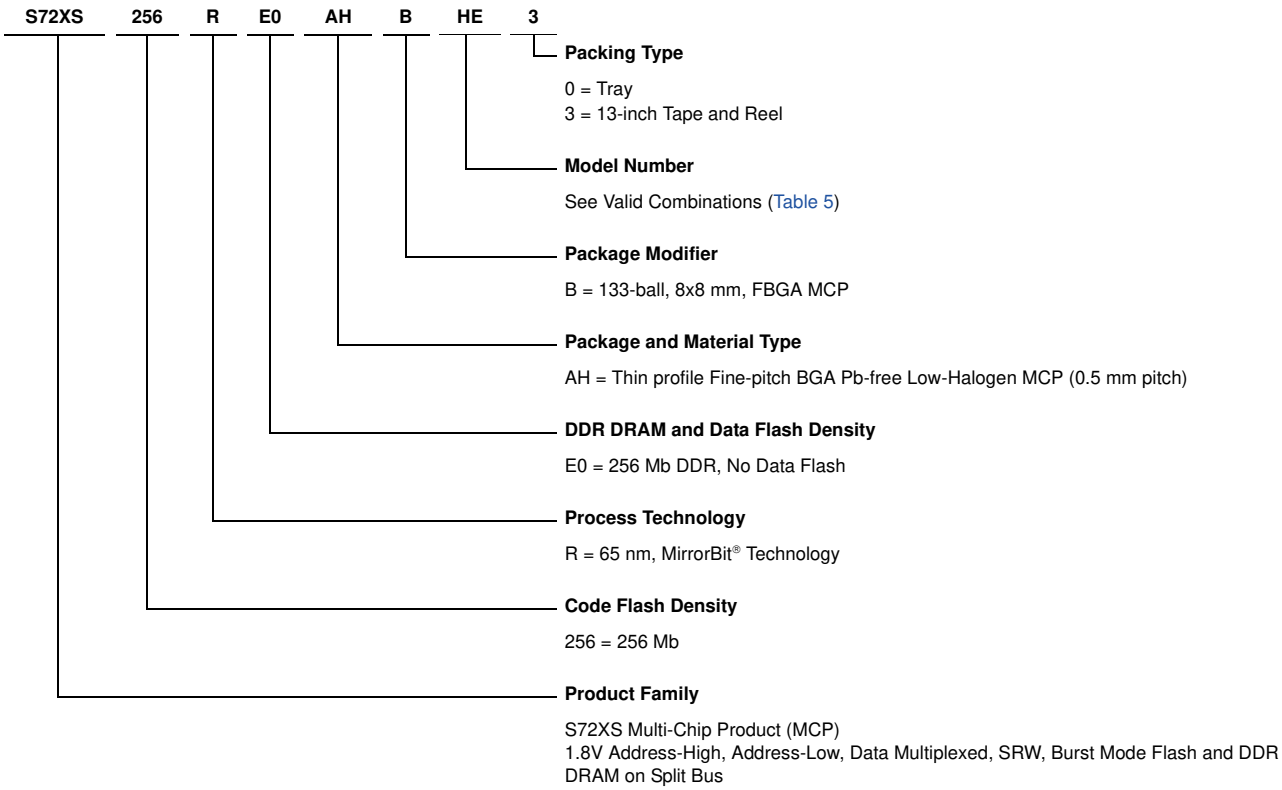
Signal Description

Table 4. Input/Output Description

Symbol	Description	Flash	RAM
ADQ15 – ADQ0	Flash multiplexed Address and Data	X	–
F-CE#	Flash Chip-enable input	X	–
F-OE#	Flash Output Enable input. Asynchronous relative to CLK for Burst mode.	X	–
F-WE#	Flash Write Enable input	X	–
F-VCC	Flash device power supply (1.7 V to 1.95 V)	X	–
F-VCCQ	Flash Input/Output Buffer power supply	X	–
VSS	Ground	X	X
F-RDY	Flash ready output. Indicates the status of the Burst read. V_{OL} = Data invalid, V_{OH} = Data valid.	X	–
F-CLK	Flash Clock. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.	X	–
F-AVD#	Flash Address Valid input. Indicates to device that the valid address is present on the address inputs. V_{IL} = For asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH} = Device ignores address inputs.	X	–
F-RST#	Flash hardware reset input. V_{IL}= device resets and returns to reading array data.	X	–
F-VPP	Flash accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.	X	–
D-Amax – D-A0	DRAM Address input	–	X
D-DQ15 – D-DQ0	DRAM Data input/output	–	X
D-CLK	DRAM System Clock	–	X
D-CE#	DRAM Chip Select	–	X
D-CKE	DRAM Clock Enable	–	X
D-BA1 – BA0	DRAM Bank Select	–	X
D-RAS#	DRAM Row Address Strobe	–	X
D-CAS#	DRAM Column Address Strobe	–	X
D-UDQM – D-LDQM	DRAM Data Input Mask	–	X
D-WE#	DRAM Write Enable input	–	X
D-VCCQ	DRAM Input/Output Buffer power supply	–	X
D-VCC	DRAM device power supply	–	X
D-UDQS	DRAM Upper Data Strobe, output with read data and input with write data	–	X
D-LDQS	DRAM Lower Data Strobe, output with read data and input with write data	–	X
D-CLK#	DDR Clock for negative edge of CLK	–	X
RFU	Reserved for Future Use. No device internal signal is currently connected to the package connector but there is potential future use for the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.	–	–
NC	Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).	–	–
DNU	Do Not Use. A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.	–	–

Ordering Information

The order number (Valid Combination) is formed by the following:



Valid Combinations

Valid combinations in Table 5 list the configurations planned to be supported in volume for this device. Contact your local sales office to confirm the availability of specific valid combinations and to check on newly released combinations.

Table 5. Valid Combinations

Base OPN[4]	Package	Model Number	Packing Type[3, 4]	Flash Boot	Temperature Range	Electronic Serial Number	Flash Density	DDR DRAM Density	Flash Speed (MHz)	DRAM Speed (MHz)	DRAM Specification	Package
S72XS256RE0	AHB	H1	0, 3	Top	Wireless	Yes	256 Mb	256 Mb	108	166	SDM256D166 D1R	8.0 × 8.0 mm 133-ball MCP (RSC133)
		J1		Bottom		No					SDM256D166 D3R	
		HH		Top	Industrial	Yes						
		JH		Bottom								
		H2		Top								
		J2		Bottom								

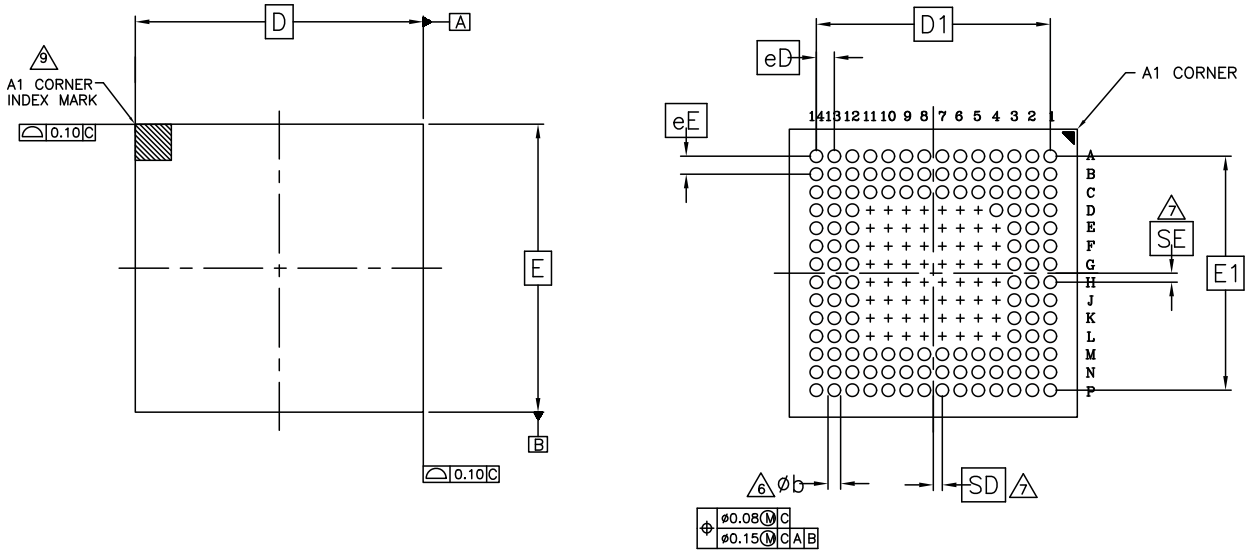
Electronic Serial Number

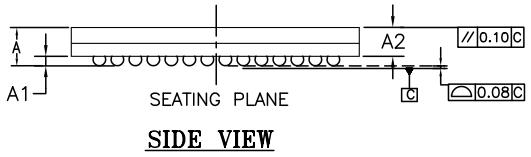
For applicable devices, the Factory Secured Silicon Area contains a random, 128-bit ESN, stored in the address range 000000h-000007h.

Notes
3. Packing Type 0 is standard. Specify other options as required.
4. BGA package marking omits leading “S” and packing type designator from ordering part number.

Package Diagram

Figure 2. RSC133 – 133-Ball Fine-Pitch Ball Grid Array (FBGA) 8.0 × 8.0 mm





PACKAGE	RSC 133			NOTE
JEDEC	N/A			
D X E	8.00mm X 8.00mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	
A	–	–	1.00	PROFILE
A1	0.18	–	–	BALL HEIGHT
A2	0.62	–	0.74	BODY THICKNESS
D		8.00 BSC		BODY SIZE
E		8.00 BSC		BODY SIZE
D1		6.50 BSC		MATRIX FOOTPRINT
E1		6.50 BSC		MATRIX FOOTPRINT
MD		14		MATRIX SIZE D DIRECTION
ME		14		MATRIX SIZE E DIRECTION
n		133		BALL COUNT
øb	0.25	0.30	0.35	BALL DIAMETER
e		0.50 BSC		BALL PITCH
SE / SD		0.25 BSC		SOLDER BALL PLACEMENT
	D5–D11, E4–E11, F4–F11, G4–G11 H4–H11, J4–J11, K4–K11, L4–L11			DEPOPULATED SOLDER BALL

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP–010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3643/16-038.63/12.16.09

Document History Page

Document Title: S72XS-R MCP, 256 Mb (16M x 16 bit), 1.8V MirrorBit® Flash and DDR DRAM Document Number: 002-00772				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	BWHA	10/07/2008	Initial release
*A	—	BWHA	01/13/2009	Global: Added section Electronic Serial Number
*B	—	BWHA	12/18/2009	Global: Added SDM128D166D1K OPN Product Block Diagram: Figure: Updated D-VSS and D-VSSQ connections. Removed D-TEST signal Physical Dimensions: Updated with RSC133
*C	—	BWHA	02/01/2010	Connection Diagrams: Updated figure: changed Ball A2 with DNU
*D	—	BWHA	08/19/2010	Global: Updated references for Low Power DDR SDRAM to SDM128D166D1R DDR Specification Reference: Added reference for 256 Mb DDR DRAM Product Selector Guide: Added “not recommended for new designs” note to OPN S72XS128RD0AHBH60 Added OPN S72XS256RE0AHBH1 Removed OPN S72XS256RD0AHBHE Product Block Diagram: Updated block diagram to show common Ground. Updated Note 1b. Connection Diagrams: Updated connection diagram to show common Ground Updated to show D-A12 Added table to show D-Amax value for related MCP Balls F1, M2 and M12 changed from NC to RFU Input/Output Descriptions: Replaced F-VSS, D-VSS, D-VSSQ with VSS Corrected F-ACC to F-VPP Refreshed descriptions for DNU, NC, RFU Ordering Information/Valid Combinations: Updated for new OPN S72XS256RE0AHBH1
*E	—	BWHA	12/10/2010	Global: Updated 256 Mb DRAM specification reference
*F	—	BWHA	03/17/2011	Global: Removed SDM128D166D1K references Removed OPN S72XS128RD0AHBH60, Added OPN S72XS256RE0AHBJ1
*G	—	BWHA	10/05/2011	Ordering Information: Replaced Product Selector Guide section Valid Combinations: Made a separate section Added OPNs: S72XS128RD0AHBHD, S72XS256RE0AHBHH/JH
*H	—	BWHA	04/17/2012	Ordering Information: Added ESN support for S72XS256RE0AHBH1
*I	4960467	BWHA	10/13/2015	Updated to new template.
*J	5181007	NFB	03/18/2016	Removed S72XS128RD0 as it is EOL’d.

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