TPD3S716-Q1 Automotive USB 2.0 Interface Protection with Adjustable Current Limit and Short-to-Battery, Short-Circuit Protection

1 Features

- AEC-Q100 Qualified (Grade 1)
  - Operating Temperature Range: –40°C to +125°C
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Short-to-Battery (up to 18 V) and Short-to-Ground Protection on V_{BUS_CON}
- Short-to-Battery (up to 18 V) and Short-to-V_{BUS} Protection on VD+, VD–
- IEC 61000-4-2 ESD Protection on V_{BUS_CON}, VD+, VD–
  - ±8-kV Contact Discharge
  - ±15-kV Air Gap Discharge
- ISO 10605 330-pF, 330-Ω ESD Protection on V_{BUS_CON}, VD+, VD–
  - ±8-kV Contact Discharge
  - ±15-kV Air Gap Discharge
- Low R_{ON} nFET V_{BUS} Switch (63 mΩ typical)
- High Speed Data Switches (1-GHz, 3-dB Bandwidth)
- Adjustable Hiccup Current Limit up to 2.4 A
- Fast Over-voltage Response Time
  - 2-µs typical (V_{BUS} switch)
  - 200-ns typical (Data switches)
- Independent V_{BUS} and Data enable pins for configuring both Host and Client/OTG mode
- Fault Output Signal
- Thermal Shutdown Feature
- Flow-through layout in 16-Pin SSOP Package (4.9 mm x 3.9 mm)

2 Applications

- End Equipment
  - Head Units
  - Rear Seat Entertainment
  - Telematics
  - USB Hubs
  - Navigation Modules
  - Media Interface
- Interfaces
  - USB 2.0

3 Description

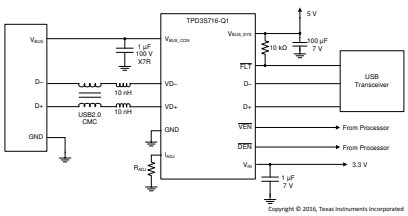
The TPD3S716-Q1 is a single-chip solution for short-to-battery, short-circuit, and ESD protection with an adjustable current-limit for the USB connector's V_{BUS} and data lines in automotive applications. The integrated data switches provide best-in-class bandwidth for minimal signal degradation while simultaneously providing 18 V short-to-battery protection. The high bandwidth of 1 GHz allows for USB2.0 high-speed data rates for applications like Car Play. Extra margin in bandwidth above 720-MHz also helps to maintain a clean USB 2.0 eye diagram with the long captive cables that are common in the automotive USB environment. The short-to-battery protection isolates the internal system circuits from any over-voltage conditions at the V_{BUS_CON}, VD+, and VD– pins. On these pins, the TPD3S716-Q1 can handle over-voltage protection up to 18 V for hot plug and DC events. The over-voltage protection circuit provides the most reliable short-to-battery isolation in the industry, shutting off the data switches in 200 ns and protecting the upstream circuitry from harmful voltage and current spikes.

The V_{BUS_CON} pin also provides an adjustable current limited load switch and handles short-to-ground protection. The device supports V_{BUS} currents up to 2.4 A, allowing support for charging USB BC1.2, USB Type-C 5V/1.5A, and proprietary charging schemes up to 2.4 A. The separate enable pins for data and VBUS allow for both host and client-OTG mode. TPD3S716-Q1 also integrates system level IEC 61000-4-2 and ISO 10605 ESD protection on its V_{BUS_CON}, VD+, and VD– pins removing the need to provide external high voltage, low capacitance diodes.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD3S716-Q1	SSOP (16)	4.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Schematic

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4 Revision History

Changes from Revision C (June 2016) to Revision D (August 2020)	Page
• Added functional safety link to the *Features* section	1
• Updated the numbering format for tables, figures and cross-references throughout the document	1

Changes from Revision B (April 2016) to Revision C (June 2016)	Page
• Changed *Adjustable Hiccup Current Limit* from 1.7 A to 2.4 A in the *Features* section	1
• Updated *Description* section	1
• Changed *Current through V_{BUS} switch* from 1.7 A to 2.4 A	4
• Updated the R_{ADJ} minimum resistance to 57 kΩ in *Recommended Operating Conditions* table	4
• aDDED new current limit values to *Electrical Characteristics* table	5
• Updated Figure 8-1	14
• Updated *I_{VBUS} Operating Maximum* in Figure 9-7 to go up to 2.4 A	21

Changes from Revision A (April 2016) to Revision B (April 2016)	Page
• Made changes to the *Electrical Characteristics* table	1

Changes from Revision * (March 2016) to Revision A (April 2016)	Page
• Changed device status from *Product Preview* to *Production Data*	1

5 Pin Configuration and Functions

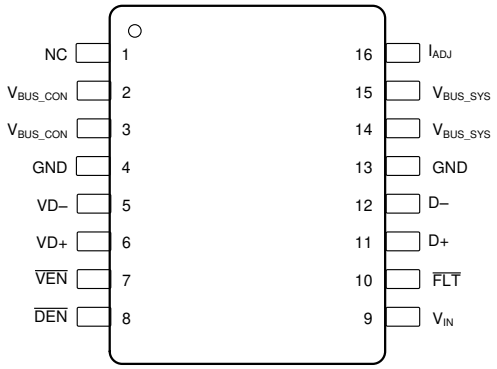


Figure 5-1. DBQ Package 16-Pin SSOP Top View

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	NC	NC	No connect, leave floating or connect to ground. Do not connect to V_{BUS_CON}
2	V_{BUS_CON}	O	Connect to USB connector V_{BUS}; provides IEC 61000-4-2 ESD protection
3	V_{BUS_CON}	O	
4	GND	Ground	Connect to PCB ground plane
5	VD–	I/O	Connect to USB connector D–; provides IEC 61000-4-2 ESD protection
6	VD+	I/O	Connect to USB connector D+; provides IEC 61000-4-2 ESD protection
7	$\overline{VEN}$	I	Enable Active-Low Input. Drive $\overline{VEN}$ low to enable the V_{BUS} path of the device. Drive $\overline{VEN}$ high to disable the V_{BUS} path of the device
8	$\overline{DEN}$	I	Enable Active-Low Input. Drive $\overline{DEN}$ low to enable the data path of the device. Drive $\overline{DEN}$ high to disable the data path of the device
9	V_{IN}	I	Connect to 3.3-V I/O. Controls the OVP threshold for VD+/VD–
10	$\overline{FLT}$	O	Open-Drain fault pin. See the *Detailed Description* section for operation
11	D+	I/O	Connect to the internal transceiver D+ pin
12	D–	I/O	Connect to the internal transceiver D– pin
13	GND	Ground	Connect to PCB ground plane
14	V_{BUS_SYS}	I	Connect to internal V_{BUS} plane
15	V_{BUS_SYS}	I	
16	I_{ADJ}	I	Connect to a resistor to GND to adjust the current limit threshold

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
V_{BUS_CON}	Supply voltage from USB connector	–0.3	18	V
V_{BUS_SYS}	Internal Supply DC voltage Rail on the PCB	–0.3	6	V
VD+, VD–	Voltage range from connector-side USB data lines	–0.3	18	V
D+, D–	Voltage range for internal USB data lines	–0.3	V_{IN} + 0.3	V
V_{IN}	Voltage range for V_{IN} supply input	–0.3	4	V
$\overline{DEN}$	Voltage on enable pins		7	V
$\overline{VEN}$			7	V
I_{BUS}	Maximum DC output current on V_{BUS_CON} pin(3)		2.4	A
V_{IADJ}	Voltage range for I_{ADJ} pin	–0.3	V_{VBUS_SYS} + 0.3	V
$V_{\overline{FLT}}$	Voltage range for the $\overline{FLT}$ pin	–0.3	7	V
T_A	Operating free air temperature(3)	–40	125	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) Thermal limits and power dissipation limits must be observed.

6.2 ESD Ratings—AEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2, V_{BUS_CON}, VD+, VD– pins	Contact discharge(1)	±8000	V
			Air-gap discharge(1)	±15000	

(1) See Figure 7-2 for details on system level ESD testing setup.

6.4 ESD Ratings—ISO Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ISO 10605 (330 pF, 330 Ω), V_{BUS_CON}, VD+, VD– pins	Contact discharge(1)	±8000	V
			Air-gap discharge(1)	±15000	

(1) See Figure 7-2 for details on system level ESD testing setup.

6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{BUS_CON}	Supply voltage from USB connector			5.9	V
V_{BUS_SYS}	Internal supply DC voltage Rail on the PCB	4.75		5.9	V
VD+, VD–	Voltage range from connector-side USB data lines	0		V_{IN} + 0.3	V

6.5 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
D+, D–	Voltage range for internal USB data lines		0		V_{IN} + 0.3	V
V_{IN}	Voltage range for V_{IN} supply		3		3.6	V
I_{BUS}	Current through V_{BUS} switch(1)				2.4	A
$\overline{VEN}$, $\overline{DEN}$	Voltage range for enable		0		5.9	V
C_{SYS}	Input capacitance(2)	V_{BUS_SYS} pin		100		µF
C_{LOAD}	Output load capacitance(2)	V_{BUS_CON} pin	1			µF
C_{VIN}	V_{IN} capacitance(2)	V_{IN} pin	1			µF
R_{ADJ}	Resistance of R_{ADJ} resistor(2)	I_{ADJ} pin	57			kΩ

(1) Depending on your I_{BUS} current level, maximum operating junction temperature derating may be required. For I_{BUS} > 1.5A, care should be taken in the PCB design to improve the board's thermal coefficient. Please see both the Power Dissipation and Junction Temperature and Layout Optimized for Thermal Performance sections for more details.
(2) See the Figure 9-1 for configuration details.

6.6 Thermal Information

THERMAL METRIC(1)		TPD3S716-Q1 DBQ (SSOP) 16 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	98.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	48.0	°C/W
θ_{JB}	Junction-to-board thermal resistance	41.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.2	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	°C/W
$\theta_{JA(Custom)}$	See the *Layout Optimized for Thermal Performance* section	57.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.7 Electrical Characteristics

over operating free-air temperature range, $\overline{VEN}$ = 0 V, $\overline{DEN}$ = 0 V, V_{BUS_SYS} = 5 V, V_{IN} = 3.3 V, VD+/VD–/D+/D–/V_{BUS_CON} = float (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT CONSUMPTION						
I_{VBUS_SLEEP}	V_{BUS} Sleep current consumption	Measured at V_{BUS_SYS} pin, $\overline{VEN}$ = 5 V, $\overline{DEN}$ = 5 V		45	150	µA
I_{VBUS}	V_{BUS} Operating current consumption	Measured at V_{BUS_SYS} pin		285	380	µA
I_{VIN}	Leakage current for V_{IN}	Measured at V_{IN} pin, V_{IN} = 3.6 V		12	20	µA
$I_{ON(LEAK)}$	Leakage into V_{BUS_SYS} while shorted to battery and powered on	Measured flowing into V_{BUS_SYS} pin, V_{BUS_SYS} = 5 V, V_{BUS_CON} = 18 V		225	300	µA
$I_{OFF(LEAK)}$	Leakage through V_{BUS} path while shorted to battery and unpowered	Measured flowing out of V_{BUS_SYS} pin, V_{BUS_SYS} = 0 V, V_{BUS_CON} = 18 V			50	µA
$I_{D(OFF\_LEAK)}$	Leakage out of data path while shorted to battery and unpowered	Measured flowing out of D+ or D– pins, V_{BUS_SYS} = 0 V, VD+ or VD– = 18 V, V_{IN} = 0 V, D+/D– = 0 V	–1		1	µA
$I_{D(ON\_LEAK)}$	Leakage out of data path while shorted to battery and powered on	Measured flowing out of D+ or D– pins, V_{BUS_SYS} = 5 V, VD+ or VD– = 18 V, V_{IN} = 3.3 V, D+/D– = 0 V	–1		1	µA
$I_{VD(OFF\_LEAK)}$	Leakage into data path while shorted to battery and unpowered	Measured flowing in to VD+ or VD– pins, V_{BUS_SYS} = 0 V, VD+ or VD– = 18 V, V_{IN} = 0 V, D+/D– = 0 V			85	µA
$I_{VD(ON\_LEAK)}$	Leakage into data path while shorted to battery and powered on	Measured flowing in to VD+ or VD– pins, V_{BUS_SYS} = 5 V, VD+ or VD– = 18 V, V_{IN} = 3.3 V D+/D– = 0 V			85	µA
V_{IN} PIN						

6.7 Electrical Characteristics (continued)

over operating free-air temperature range, $\overline{VEN}$ = 0 V, $\overline{DEN}$ = 0 V, V_{BUS_SYS} = 5 V, V_{IN} = 3.3 V, VD+/VD–/D+/D–/V_{BUS_CON} = float (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO(RISING)}$	Undervoltage lockout rising for V_{IN}	V_{IN}	Ramp V_{IN} up until V_{BUS} and Data FETs turn on, $\overline{VEN}$ =0 V, $\overline{DEN}$ = 0 V	2.6	2.7	2.9	V
$V_{UVLO(FALLING)}$	Undervoltage lockout falling for V_{IN}		Ramp V_{IN} down until V_{BUS} and Data FETs turn off, $\overline{VEN}$ =0 V, $\overline{DEN}$ = 0 V	2.5	2.6	2.8	
$\overline{VEN}$, $\overline{DEN}$, $\overline{FLT}$ PINS							
V_{IH}	High-level input voltage	$\overline{VEN}$, $\overline{DEN}$	Set $\overline{VEN}$ ($\overline{DEN}$)= 0 V; Sweep $\overline{VEN}$ ($\overline{DEN}$) to 1.4 V; Measure when V_{BUS} (Data) FET turns off	1.2			V
V_{IL}	Low-level input voltage	$\overline{VEN}$, $\overline{DEN}$	Set $\overline{VEN}$ ($\overline{DEN}$) = 3.3 V; Sweep $\overline{VEN}$ ($\overline{DEN}$) from 3.3 V to 0.5 V; Measure when V_{BUS} (Data) FET turns on			0.8	V
I_{IL}	Input Leakage Current	$\overline{VEN}$, $\overline{DEN}$	$V_{(\overline{VEN})}$ ($V_{(\overline{DEN})}$)= 3.3 V ; Measure Current into $\overline{VEN}$ ($\overline{DEN}$) pin			1	µA
V_{OL}	Low-level output voltage	$\overline{FLT}$	I_{OL} = 3 mA			0.4	V
OCP CIRCUIT—V_{BUS}							
I_{LIM}	Overcurrent limit, R_{ADJ} = 280 kΩ ± 1%	V_{BUS}	Progressively load V_{BUS_CON} until device asserts $\overline{FLT}$	505		620	mA
I_{LIM}	Overcurrent limit, R_{ADJ} = 158 kΩ ± 1%	V_{BUS}	Progressively load V_{BUS_CON} until device asserts $\overline{FLT}$	0.905		1.1	A
I_{LIM}	Overcurrent limit, R_{ADJ} = 143 kΩ ± 1%	V_{BUS}	Progressively load V_{BUS_CON} until device asserts $\overline{FLT}$	1.005		1.2	A
I_{LIM}	Overcurrent limit, R_{ADJ} = 93.1 kΩ ± 1%	V_{BUS}	Progressively load V_{BUS_CON} until device asserts $\overline{FLT}$	1.505		1.8	A
I_{LIM}	Overcurrent limit, R_{ADJ} = 76.8 kΩ ± 1%	V_{BUS}	Progressively load V_{BUS_CON} until device asserts $\overline{FLT}$	1.8		2.16	A
I_{LIM}	Overcurrent limit, R_{ADJ} = 66.5 kΩ ± 1%	V_{BUS}	Progressively load V_{BUS_CON} until device asserts $\overline{FLT}$	2.105		2.57	A
I_{LIM}	Overcurrent limit, R_{ADJ} = 57.6 kΩ ± 1%	V_{BUS}	Progressively load V_{BUS_CON} until device asserts $\overline{FLT}$	2.405		2.93	A
I_{LIM}	Overcurrent limit, I_{ADJ} = GND	V_{BUS}	Progressively load V_{BUS_CON} until device asserts $\overline{FLT}$	550	700	850	mA
I_{LIM}	Overcurrent limit, I_{ADJ} = V_{BUS_SYS}	V_{BUS}	Progressively load V_{BUS_CON} until device asserts $\overline{FLT}$	1.1	1.4	1.7	A
OVER TEMPERATURE PROTECTION							
$T_{SD(RISING)}$	The rising over-temperature protection shutdown threshold		V_{BUS_SYS} = 5 V, $\overline{VEN}$ = 0 V, $\overline{DEN}$ = 0 V, No Load on V_{BUS_CON}, T_A stepped up until $\overline{FLT}$ is asserted	150	165	180	℃
$T_{SD(FALLING)}$	The falling over-temperature protection shutdown threshold		V_{BUS_SYS} = 5 V, $\overline{VEN}$ = 0 V, $\overline{DEN}$ = 0 V, No Load on V_{BUS_CON}, T_A stepped down from $T_{SD(RISING)}$ until $\overline{FLT}$ is deasserted	125	130	142	℃
$T_{SD(HYST)}$	The over-temperature protection shutdown threshold hysteresis		$T_{SD(RISING)}$ – $T_{SD(FALLING)}$	10	35	55	℃
OVP CIRCUIT—V_{BUS}							
$V_{OVP(RISING)}$	Input overvoltage protection threshold	V_{BUS_CON}	Increase V_{BUS_CON} from 5 V to 7 V. Measure when $\overline{FLT}$ is asserted	5.6	5.8	6	V
$V_{HYS(OVP)}$	Hysteresis on OVP	V_{BUS_CON}	Difference between rising and falling OVP thresholds on V_{BUS_CON}		50		mV
$V_{OVP(FALLING)}$	Input overvoltage protection threshold	V_{BUS_CON}	Decrease V_{BUS_CON} from 7 V to 5 V. Measure when $\overline{FLT}$ is deasserted	5.52	5.75	5.98	V
$V_{REV\_SUPPLY(RISING)}$	Reverse supply detection threshold	V_{BUS_CON} – V_{BUS_SYS}	Set V_{BUS_SYS} to 5 V. Increase V_{BUS_CON} from V_{BUS_SYS} to V_{BUS_SYS} + 300 mV. Measure the value of V_{BUS_CON} – V_{BUS_SYS} when $\overline{FLT}$ asserts. 25°C ≤ T_A ≤ 125°C	140	200	260	mV
$V_{REV\_SUPPLY(FALLING)}$	Reverse supply detection threshold	V_{BUS_CON} – V_{BUS_SYS}	Set V_{BUS_SYS} to 5 V. Decrease V_{BUS_CON} from V_{BUS_SYS} + 300 mV to V_{BUS_SYS}. Measure the value of V_{BUS_CON} – V_{BUS_SYS} when $\overline{FLT}$ deasserts. 25°C ≤ T_A ≤ 125°C	70	120	165	mV
$V_{REV\_SUPPLY(HYST)}$	Hysteresis on reverse supply detection	V_{BUS_CON} – V_{BUS_SYS}	Difference between rising and falling reverse supply detection thresholds		80		mV

6.7 Electrical Characteristics (continued)

over operating free-air temperature range, $\overline{VEN}$ = 0 V, $\overline{DEN}$ = 0 V, V_{BUS_SYS} = 5 V, V_{IN} = 3.3 V, VD+/VD–/D+/D–/V_{BUS_CON} = float (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO(SYS\_RISING)}$	Undervoltage lockout rising for V_{BUS_SYS}	V_{BUS_SYS}	V_{BUS_SYS} voltage rising from 0 V to 5 V	3.1	3.3	3.6	V
$V_{HYS(UVLO\_SYS)}$	V_{BUS_SYS} UVLO Hysteresis	V_{BUS_SYS}	Difference between rising and falling UVLO thresholds on V_{BUS_SYS}	50	75	100	mV
$V_{UVLO(SYS\_FALLING)}$	Undervoltage lockout falling for V_{BUS_SYS}	V_{BUS_SYS}	V_{BUS_SYS} voltage falling from 5 V to 2.9 V	3	3.2	3.5	V
$V_{SHRT(RISING)}$	Short-to-ground comparator rising threshold	V_{BUS_CON}	Increase V_{BUS_CON} voltage from 0 V until the device transitions from the short-circuit to over-current mode of operation	2.5	2.6	2.7	V
$V_{SHRT(FALLING)}$	Short-to-ground comparator falling threshold	V_{BUS_CON}	Set V_{BUS_SYS} = 5 V; V_{IN} = 3.3 V; $\overline{VEN}$ = 0 V, $\overline{DEN}$ = 0 V; Decrease V_{BUS_CON} voltage from 5 V until the device transitions from the over-current to short-circuit mode of operation	2.4	2.5	2.6	V
$V_{SHRT(HYST)}$	Short-to-ground comparator hysteresis	V_{BUS_CON}	Difference between $V_{SHRT(RISING)}$ and $V_{SHRT(FALLING)}$		125		mV
I_{SHRT}	Short-to-ground current source	V_{BUS_CON}	Current sourced from V_{BUS_SYS} when device is in short-circuit mode	150		350	mA
OVP CIRCUIT—VD+/VD–							
$V_{OVP(RISING)}$	Input overvoltage protection threshold	VD+/VD–	Increase VD+ or VD– (with D+ and D–) from 3.3 V to 4.5 V. Measure the value at which $\overline{FLT}$ is asserted	V_{IN} + 0.6	V_{IN} + 0.8	V_{IN} + 1	V
$V_{HYS(OVP)}$	Hysteresis on OVP	VD+/VD–	Difference between rising and falling OVP thresholds on VD+/VD–		50		mV
$V_{OVP(FALLING)}$	Input overvoltage protection threshold	VD+/VD–	Decrease VD+ or VD– (with D+ or D–) from 4.5 V to 2 V. Measure the value at $\overline{FLT}$ is deasserted	V_{IN} + 0.525	V_{IN} + 0.75	V_{IN} + 0.975	V
SHORT TO BATTERY							
$V_{(VBUS\_STB)}$	V_{BUS} hotplug short-to-battery tolerance	V_{BUS_CON}	Charge battery-equivalent capacitor to test voltage then discharge to pin under test through a 1 meter, 18 gauge wire. (See Figure 7-1 for more details)			18	V
$V_{(DATA\_STB)}$	Data line hotplug short-to-battery tolerance	VD+/VD–				18	V
DATA LINE SWITCHES—VD+ to D+ or VD– to D–							
C_{ON}	Equivalent On Capacitance		Capacitance of D+/D– switches when enabled – measure on connector side at VDx = 0.4 V		6.9		pF
R_{ON}	On Resistance		Measure resistance between D+ and VD+ or D– and VD–, voltage between 0 V and 0.4 V		4	6.5	Ω
$R_{ON(Flat)}$	On Resistance flatness		Measure resistance between D+ and VD+ or D– and VD–, sweep voltage between 0 V and 0.4 V		0.2	1	Ω
BW_{ON}	On Bandwidth (–3dB)		Measure S_{21} bandwidth from D+ to VD+ or D– to VD– with voltage swing = 400 mVpp, V_{CM}= 0.2 V		910		MHz
BW_{ON_DIFF}	On Bandwidth (–3dB)		Measure S_{DD21} bandwidth from D+ to VD+ and D– to VD– with voltage swing = 800 mVpp differential, V_{CM}= 0.2 V		1050		MHz
X_{talk}	Crosstalk		Measure S_{21} bandwidth from D+ to VD– or D– to VD+ with voltage swing = 400 mVpp. Make sure to terminate open sides to 50 ohms. f = 480 MHz		–28		dB
nFET SWITCH—V_{BUS}							
$R_{(DISCHARGE)}$	Output discharge resistance		$\overline{VEN}$ = 5 V, $\overline{DEN}$ = 5 V, Set V_{BUS_CON} = 5 V and measure current flow to ground		18	30	kΩ
R_{ON}	V_{BUS} path ON resistance		V_{BUS_CON} = 5 V, I_{OUT} = 1.5 A. See Figure 9-8 for a plot of the maximum V_{BUS} R_{ON} possible at a given junction temperature		63	135	mΩ

6.8 Timing Characteristics

over operating free-air temperature range, $\overline{VEN}$ = 0 V, $\overline{DEN}$ = 0 V, V_{BUS_SYS} = 5 V, V_{IN} = 3.3 V, D+/D– = 45 Ω to GND, VD+/VD–/V_{BUS_CON} = float (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE PIN					

over operating free-air temperature range, $\overline{VEN}$ = 0 V, $\overline{DEN}$ = 0 V, V_{BUS_SYS} = 5 V, V_{IN} = 3.3 V, D+/D– = 45 Ω to GND, VD+/VD–/V_{BUS_CON} = float (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON_HOST}	Host mode enable on time	Time between $\overline{VEN}$ and $\overline{DEN}$ asserted low and V_{BUS} and Data FETs turn on, C_{VBUS_CON} = 0 µF		5.7		ms
t_{ON_CLIENT}	Client mode enable on time	Time between $\overline{DEN}$ asserted low and Data FETs turn on. $\overline{VEN}$ remains high		2.4		ms
t_{OFF_HOST}	Host mode disable time	Time between $\overline{VEN}$ and $\overline{DEN}$ deasserted high and V_{BUS} and Data FETs turn off, C_{VBUS_CON} = 0 µF		30		µs
t_{OFF_CLIENT}	Client mode disable time	Time between $\overline{DEN}$ deasserted high and Data FETs turn off. $\overline{VEN}$ remains high		5		µs
$t_{HOST\_TO\_CLIENT}$	Host to Client mode transition time	Time between $\overline{VEN}$ deasserted high and V_{BUS} FET turns off. $\overline{DEN}$ remains low, C_{VBUS_CON} = 0 µF		70		µs
$t_{CLIENT\_TO\_HOST}$	Client to Host mode transition time	Time between $\overline{VEN}$ asserted low and V_{BUS} FET turns on. $\overline{DEN}$ remains low, C_{VBUS_CON} = 0 µF		3.4		ms
OVER CURRENT PROTECTION						
t_{BLANK}	Overcurrent blanking time	Time from overcurrent condition until $\overline{FLT}$ assertion and V_{BUS} FET turn off			2	ms
t_{RETRY}	Overcurrent retry time	Time from overcurrent FET shut off until FET turns back on		100		ms
t_{RECV}	Overcurrent recovery time	Time from end of t_{RETRY} until $\overline{FLT}$ deassertion if overcurrent condition is removed		8		ms
OVER VOLTAGE PROTECTION						
$t_{OVP\_response}$	OVP Response time – V_{BUS}	Measured from OVP Condition to FET turnoff		2	4	µs
$t_{OVP\_response}$	OVP Response time – data switches	Measured from OVP Condition to FET turnoff		200		ns
$t_{OVP\_\overline{FLT}\_ASSERT}$	OVP $\overline{FLT}$ assertion time	Measured from an OVP Condition to $\overline{FLT}$ assertion		14		µs
SHORT TO GROUND PROTECTION						
t_{SHRT}	Short to ground response time	Time from short condition until current falls below 120% of I_{SHRT}, C_{VBUS_CON} = 0 µF		2	4	µs
t_{SHRT_FLTZ}	Short to ground $\overline{FLT}$ assertion time	Time from short condition until $\overline{FLT}$ is asserted, C_{VBUS_CON} = 0 µF		20		µs
REVERSE SUPPLY DETECTION						
$t_{REV\_SUPPLY\_BLANK}$	Reverse supply blanking time	Time from reverse current condition until $\overline{FLT}$ assertion			2	ms

6.9 Typical Characteristics

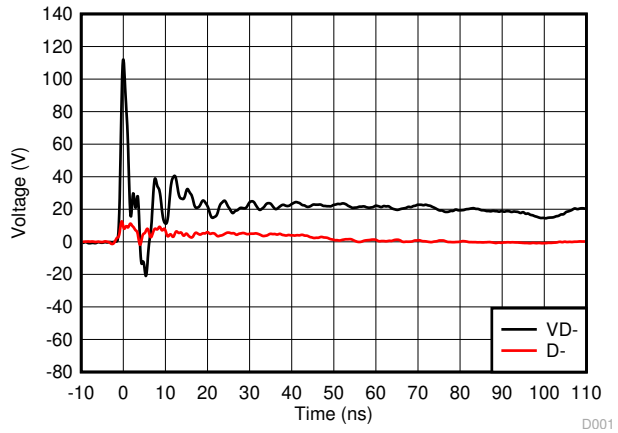


Figure 6-1. 8-kV IEC Contact Waveform

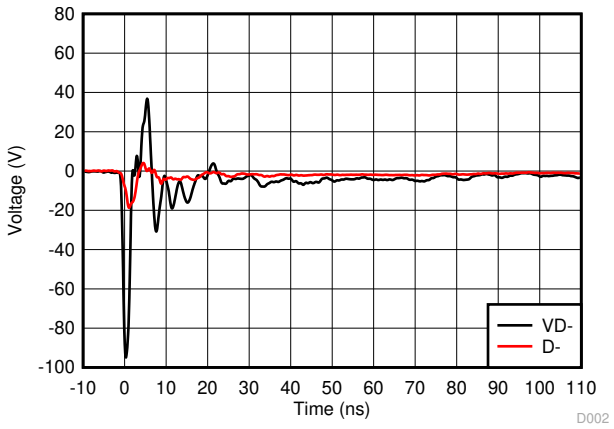


Figure 6-2. –8-kV IEC Contact Waveform

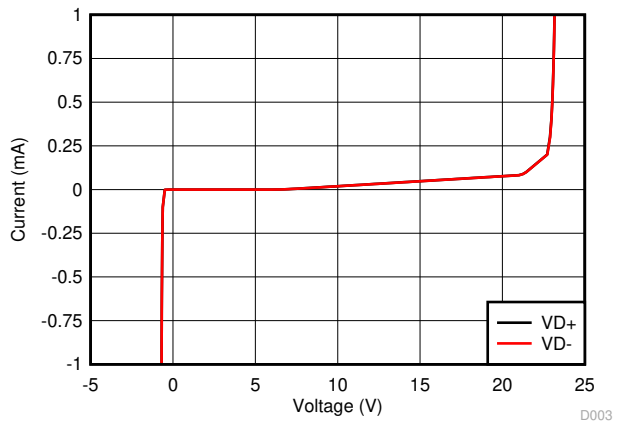


Figure 6-3. Data Line I-V Curve

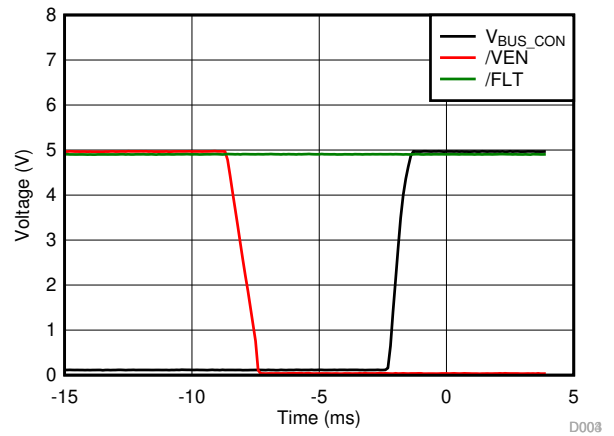


Figure 6-4. V_{BUS} t_{ON} Time

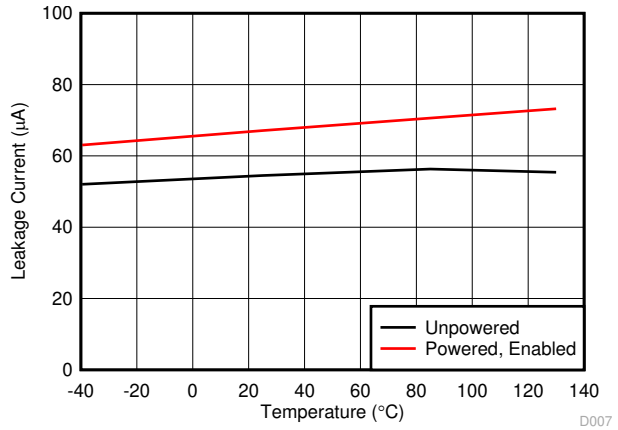


Figure 6-5. VD± Leakage Current at 18-V across Temperature

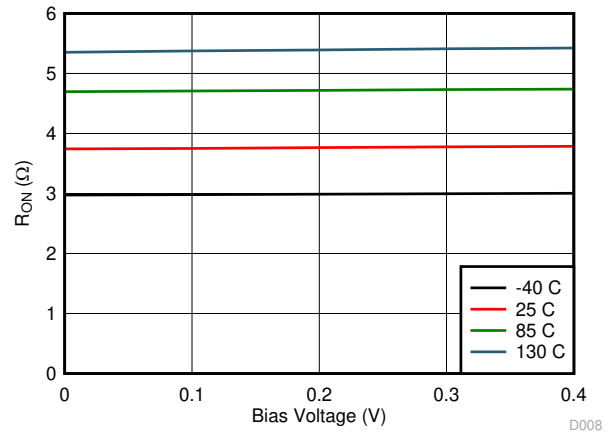


Figure 6-6. Data Switch R_{ON} vs Bias Voltage

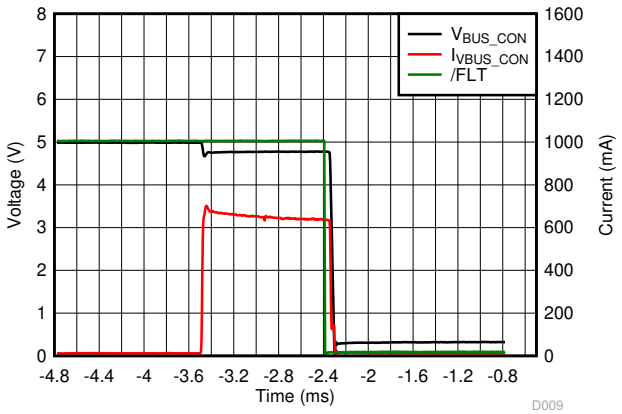


Figure 6-7. Overcurrent t_{BLANK} Response Waveform

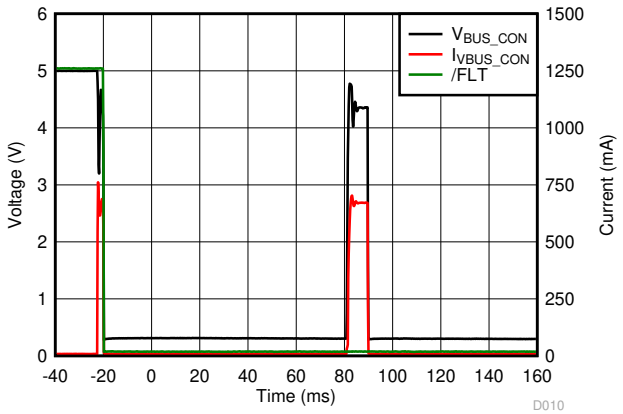


Figure 6-8. Overcurrent t_{BLANK_RETRY} Response Waveform

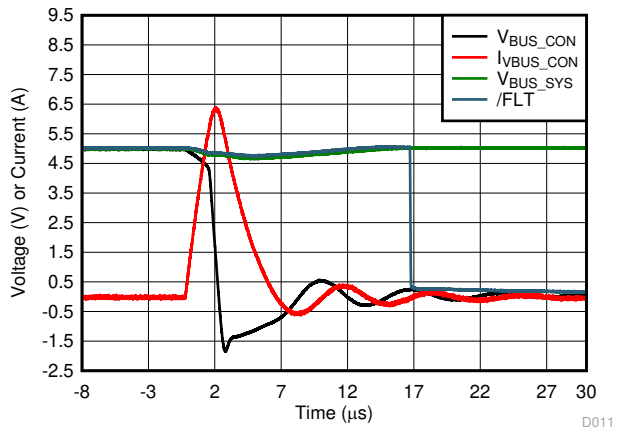


Figure 6-9. V_{BUS} Short-to-Ground Response Waveform

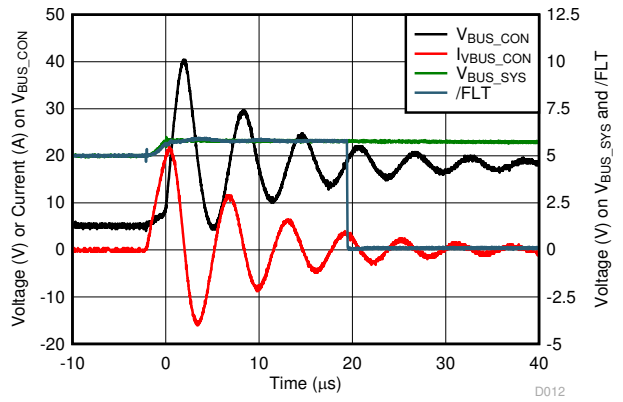


Figure 6-10. V_{BUS} Short-to-18 V Response Waveform

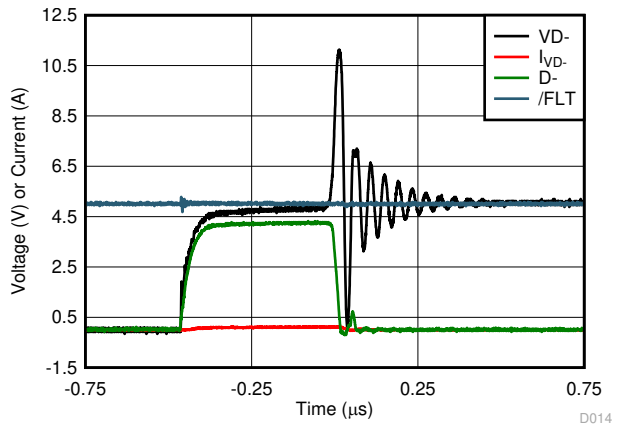


Figure 6-11. Data Switch Short-to-5 V Response Waveform

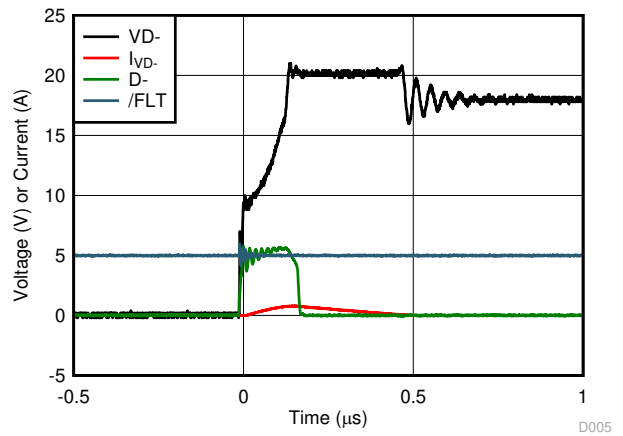


Figure 6-12. Data Switch Short-to-18 V Response Waveform

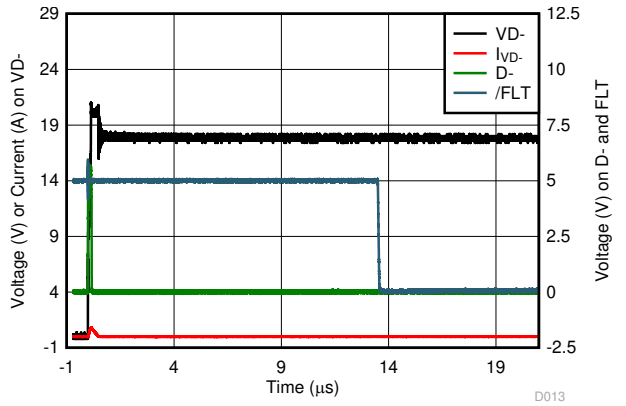


Figure 6-13. Data Switch Short-to-18 V Response Waveform (Long)

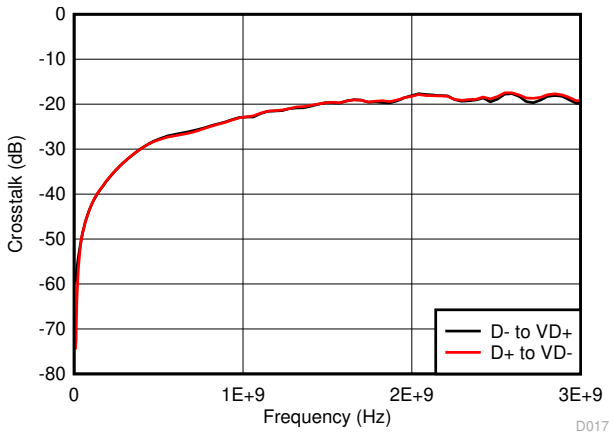


Figure 6-14. Data Switch Crosstalk

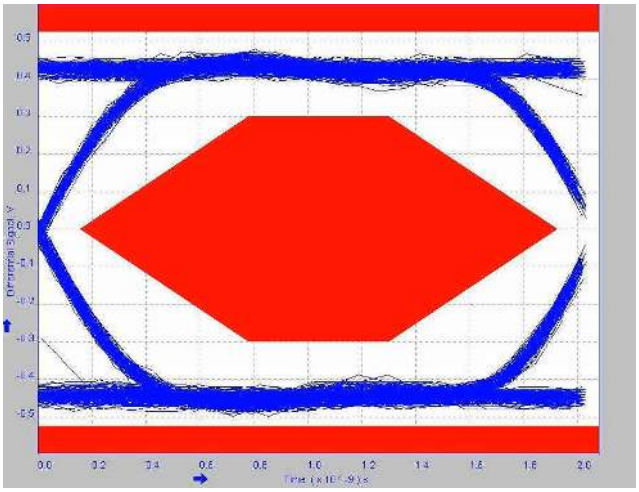


Figure 6-15. USB2.0 Eye Diagram (no TPD3S716-Q1)

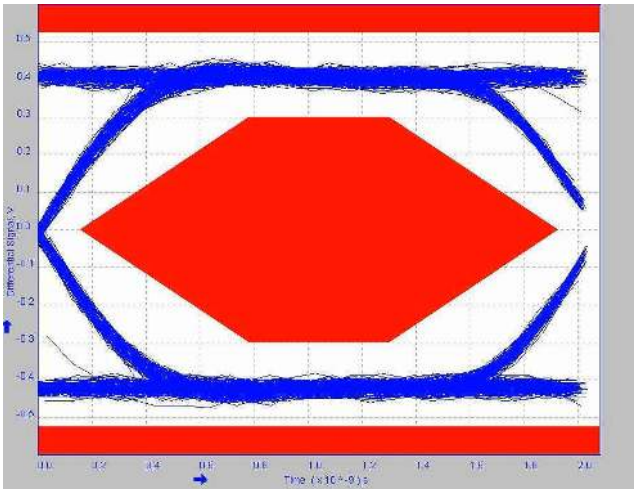


Figure 6-16. USB2.0 Eye Diagram (with TPD3S716-Q1)

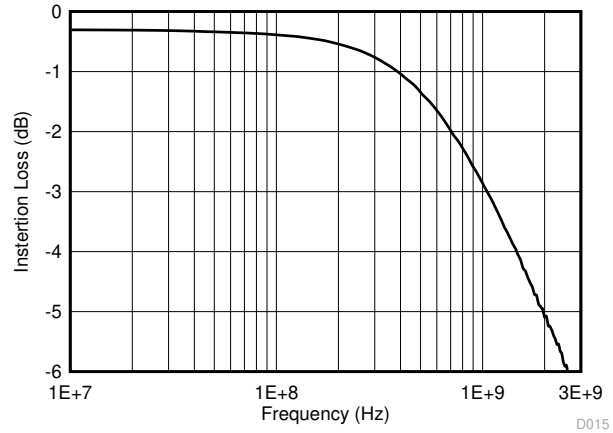


Figure 6-17. Data Switch Differential Bandwidth

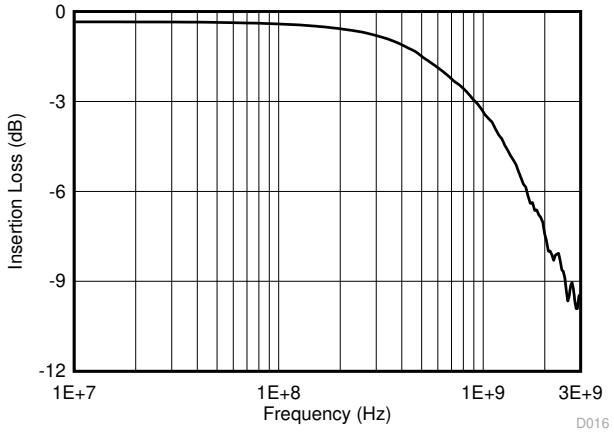


Figure 6-18. Data Switch Single-Ended Bandwidth

7 Parameter Measurement Information

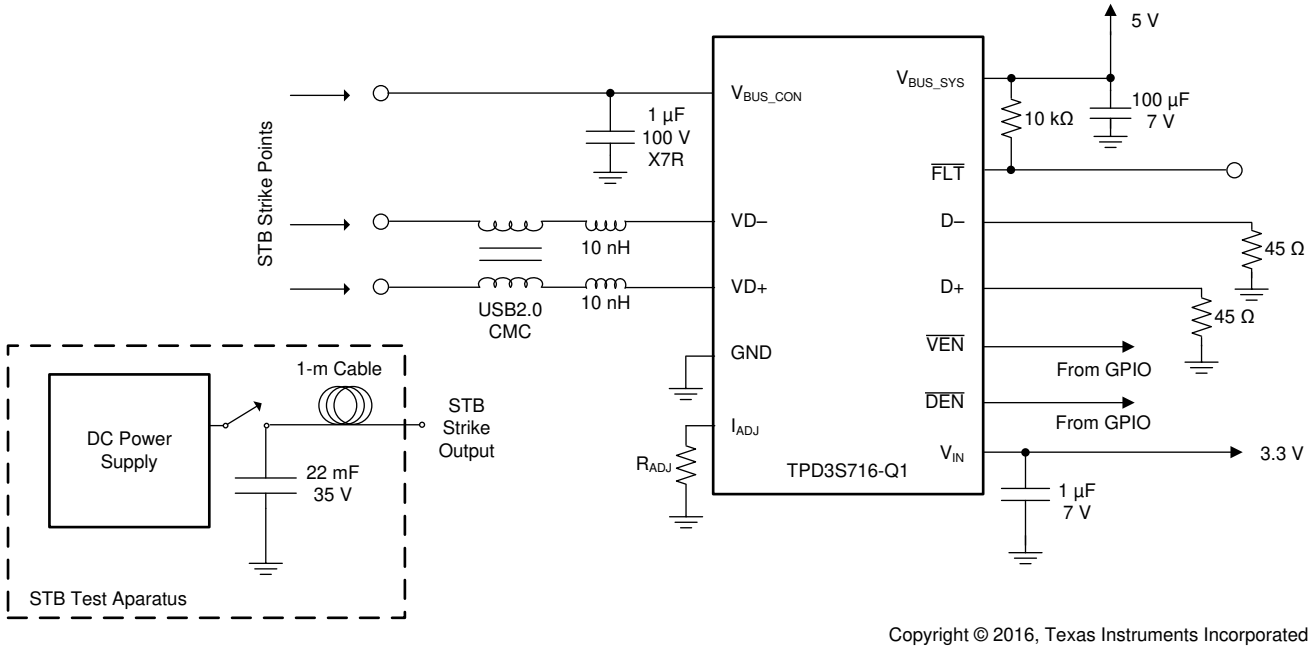


Figure 7-1. Short-to-Battery System Test Setup

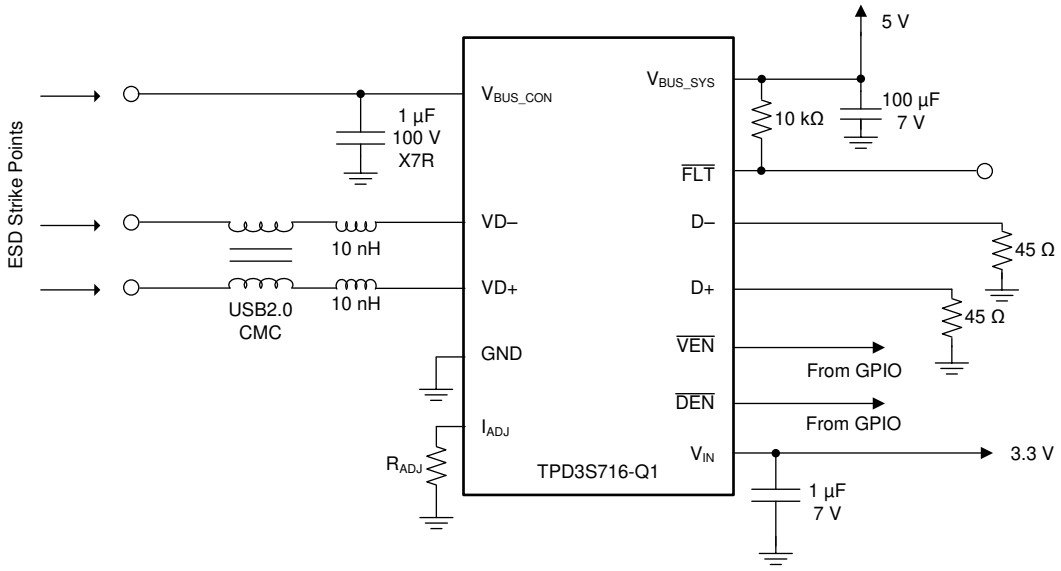


Figure 7-2. ESD System Test Setup

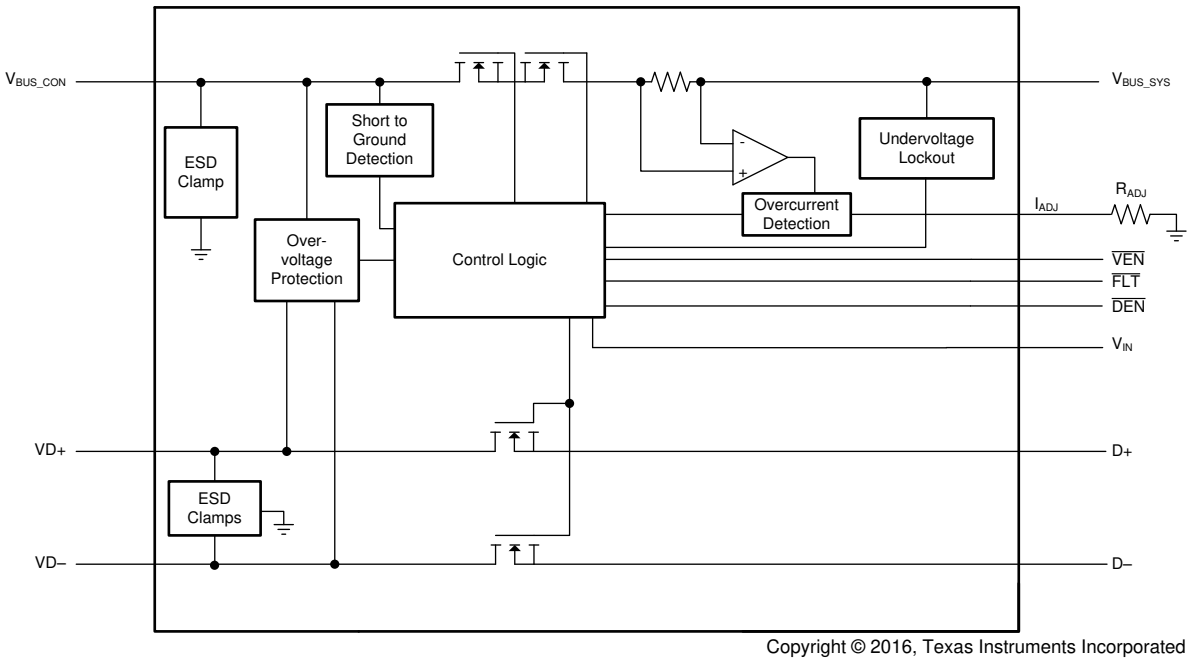
8 Detailed Description

8.1 Overview

The TPD3S716-Q1 provides a single-chip ESD protection and over voltage protection solution for automotive USB interfaces. It offers short to battery protection up to 18 V and short to ground protection on V_{BUS_CON}. The TPD3S716-Q1 also provides a $\overline{FLT}$ pin that indicates to the system if a fault condition has occurred. The TPD3S716-Q1 offers ESD clamps on the V_{BUS_CON}, VD+, and VD– pins, therefore eliminating the need for external TVS clamp circuits in the application.

The TPD3S716-Q1 has internal circuitry that controls the turnon of the internal nFET switches. An internal oscillator controls the timers that enable the switches and resets the open-drain $\overline{FLT}$ output. If V_{BUS_CON} and VD+/VD– are less than V_{OVP}, the switches are enabled. After an internal delay the charge-pump starts-up and turns on the internal nFET switches through a soft start. At any time, if any of the external USB pins rise above their respective V_{OVP} thresholds, the nFET switches are turned OFF and the $\overline{FLT}$ pin is pulled LOW.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 AEC-Q100 Qualified

The TPD3S716-Q1 is an automotive qualified device according to the AEC-Q100 standards. The TPD3S716-Q1 is qualified to operate from –40 to +125°C ambient temperature.

8.3.2 Short-to-Battery and Short-to-Ground Protection on V_{BUS_CON}

The V_{BUS_CON} pin is protected against shorts to battery and shorts to ground.

If a voltage on V_{BUS_CON} is detected as too low (below the V_{SHRT} threshold) after the device is enabled, the device enters short-circuit protection mode and asserts $\overline{FLT}$. It sources the I_{SHRT} current until it detects the voltage rising above the V_{SHRT} threshold, where it resumes standard operating mode and deasserts $\overline{FLT}$.

If a voltage above the V_{OVP} threshold is detected by the device, it shuts off all FETs and assert a fault on the $\overline{FLT}$ pin. When the excessive voltage is removed, the device automatically re-enables and $\overline{FLT}$ deasserts.

8.3.3 Short-to-Battery and Short-to-V_{BUS} Protection on VD+, VD–

The VD+ and VD– pins are protected against shorts to battery and shorts to bus. The OVP threshold on the VD+ and VD– pins is low enough that it protects against shorts to V_{BUS}.

When a voltage above the V_{OVP} threshold is detected by the device, it shuts off all FETs and asserts a fault on the $\overline{FLT}$ pin. When the excessive voltage is removed, the device automatically re-enables and $\overline{FLT}$ deasserts.

8.3.4 ESD Protection on V_{BUS_CON}, VD+, VD–

The protected pins (V_{BUS_CON}, VD+, VD–) are tested to pass the IEC 61000-4-2 ESD standard up to Level 4 ESD protection. Additionally, these pins are tested against ISO 10605 with the 330-pF, 330- Ω equivalent network. This guarantees passing of at least ±8-kV contact discharge and ±15-kV air gap discharge according to both standards. See Figure 7-2 for the test set-up used for testing IEC 61000-4-2 and ISO 10605.

8.3.5 Low R_{ON} nFET V_{BUS} Switch

The V_{BUS} switch has a low R_{ON} that provides minimal voltage droop from system to connector. Typical resistance is 63 mΩ and is specified for 135 mΩ at 150°C junction temperature.

8.3.6 High Speed Data Switches

The D+ and D– switches have a very low capacitance and a high bandwidth (1-GHz typical), allowing for a clean USB 2.0 eye diagram.

8.3.7 Adjustable Hiccup Current Limit up to 2.4-A

The V_{BUS} path of this device has an integrated overcurrent protection circuit. The current limit threshold for the overcurrent protection is adjustable via an external resistor R_{ADJ} to GND on the I_{ADJ} pin. Equation 1 to Equation 3 approximate the minimum, nominal, and maximum current limit values for TPD3S716-Q1 assuming a 1% tolerant resistor:

$$I_{LIM(TYP)} = 143 \times R_{ADJ}^{(-0.983)} \quad (1)$$

$$I_{LIM(MIN)} = 129 \times R_{ADJ}^{(-0.981)} - 0.02 \quad (2)$$

$$I_{LIM(MAX)} = 141.5 \times R_{ADJ}^{(-0.962)} + 0.015 \quad (3)$$

where

- $I_{LIM(TYP)}$ is the nominal current limit value in (A)
- $I_{LIM(MIN)}$ is the minimum current limit value in (A)
- $I_{LIM(MAX)}$ is the maximum current limit value in (A)
- R_{ADJ} is the nominal resistor to GND on the I_{ADJ} pin in (Ω)

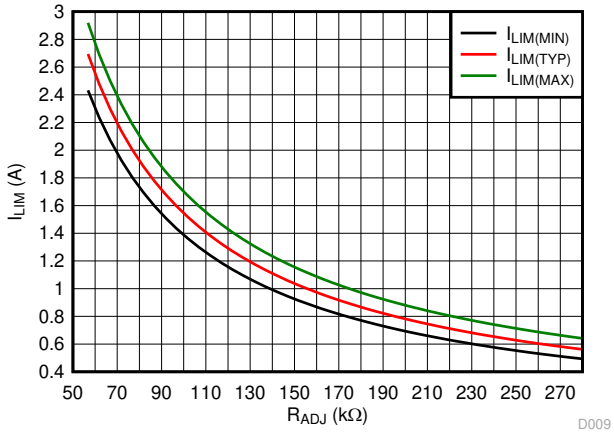


Figure 8-1. TPD3S716-Q1 Current Limit Thresholds vs. R_{ADJ}

Equation 1, Equation 2 and Equation 3 are useful for approximating the current limit threshold of TPD3S716-Q1; however, they do not constitute as part of TI's published device specifications for purposes of TI's product warranty. For the officially tested current limit threshold values, see the *Electrical Characteristics* table.

When the V_{BUS} current exceeds the overcurrent threshold, the device goes into a fault state where it limits the current to the overcurrent threshold value and asserts the $\overline{FLT}$ pin. After a short blanking time, the device cycles on and off to try to check if the connected device is still in overcurrent.

8.3.8 Fast Over-Voltage Response Time

The over-voltage FETs are designed to have a fast turnoff time to protect the upstream SoC as quickly as possible. Typical response time for complete turnoff is 2 µs for the V_{BUS} path and 200 ns for the data path.

8.3.9 Independent V_{BUS} and Data Enable Pins for Configuring both Host and Client/OTG Mode

The TPD3S716-Q1 has two enable inputs to turn on and off the device's internal FETs. The $\overline{VEN}$ pin disables and enables the V_{BUS} path. The $\overline{DEN}$ pin disables and enables the data path. Independent control of the V_{BUS} and data paths enables the TPD3S716-Q1 to be configured for both USB Host and Client/OTG mode. See Table 8-1.

8.3.10 Fault Output Signal

The TPD3S716-Q1 has a fault pin , $\overline{FLT}$ that indicates when there is any sort of fault condition because of an OVP, OCP, short-circuit, reverse-current, or thermal shutdown event occurring.

8.3.11 Thermal Shutdown Feature

In the event that the device exceeds the maximum allowable junction temperature, the thermal shutdown circuit disables the V_{BUS} and data switches and assert the fault pin low.

8.3.12 16-Pin SSOP Package

The TPD3S716-Q1 is packaged in a standard 16-pin SSOP leaded package.

8.3.13 Reverse Current Detection

If V_{BUS_CON} exceeds V_{BUS_SYS} by a voltage greater than $V_{REV\_SUPPLY(RISING)}$ for $t_{REV\_SUPPLY\_BLANK}$, then TPD3S716-Q1 detects this reverse current condition and asserts the fault pin. When $V_{BUS\_CON} - V_{BUS\_SYS}$ falls below $V_{REV\_SUPPLY(FALLING)}$, the fault pin is be deasserted and TPD3S716-Q1 enters back into its normal operating mode.

8.4 Device Functional Modes

8.4.1 Normal Operation

The TPD3S716-Q1 operates in normal operation modes when enabled, both V_{BUS_SYS} and V_{IN} are above their UVLO thresholds, and the device is not in any fault conditions. Table 8-1 shows the normal operating modes of the TPD3S716-Q1.

Table 8-1. Device Normal Operating Mode Table

MODE	$\overline{VEN}$	$\overline{DEN}$	V_{BUS} PATH	DATA PATH
USB Host	0	0	ON	ON
Power Only	0	1	ON	OFF
USB Client/OTG	1	0	OFF	ON
Disabled	1	1	OFF	OFF

8.4.2 Overvoltage Condition

When the VD+, VD–, or V_{BUS_CON} pins exceed their OVP threshold, the device enters the overvoltage state. All FETs are disabled and the $\overline{FLT}$ pin is asserted. When the protected pins drop below their OVP threshold, the device automatically turns back on and deasserts the $\overline{FLT}$ pin. An overvoltage condition is only detected on an enabled path. For example, if the data path is enabled and the V_{BUS} path is disabled (USB Client/OTG mode), if an overvoltage condition occurs on V_{BUS_CON}, the fault pin is not be asserted. However, because the FETs of disabled paths are already turned off, proper protection from overvoltage conditions are still guaranteed by the device on disabled paths.

8.4.3 Overcurrent Condition

When the current through the V_{BUS} path exceeds the I_{LIM} current threshold, the device enters into the overcurrent state. The TPD3S716-Q1 limits current to the I_{LIM} threshold by dropping voltage across the V_{BUS} FET to maintain constant current. When it continues to sense an overcurrent condition for the blanking time (t_{BLANK}), the device disables itself for the retry time (t_{RETRY}) and then retry automatically for the retry time (t_{BLANK_RETRY}). In the event that the current is below the overcurrent threshold, the device deasserts fault and resumes normal operation.

8.4.4 Short-Circuit Condition

If the voltage on the V_{BUS_CON} side is pulled below the V_{SHRT} threshold while the device is enabled, the TPD3S716-Q1 enters the short-circuit mode. It sources a constant current of I_{SHRT} until it rises above the V_{SHRT} threshold. When that occurs, the device automatically re-enters normal operation and deasserts the fault pin.

8.4.5 Device Logic Table

Table 8-2 shows the TPD3S716-Q1 logic table.

Table 8-2. TPD3S716-Q1 Logic Table

Mode	$\overline{VEN}$	$\overline{DEN}$	V_{BUS_CON}	VDx	I_{VBUS}	V_{BUS_SYS}, V_{IN}	T_J	$\overline{FLT}$	V_{BUS} PATH	DATA PATH
Unpowered	X	X	X	X	None	< UVLO	X	H	OFF	OFF
Disabled	H	H	X	X	None	> UVLO	< TSD	H	OFF	OFF
Host	L	L	< OVP & < V_{BUS_SYS} + 200 mV(typical) & > V_{SHRT}	< OVP	< OCP	> UVLO	< TSD	H	ON	ON
Client/OTG	H	L	X	< OVP	None	> UVLO	< TSD	H	OFF	ON
Power Only	L	H	< OVP & < V_{BUS_SYS} + 200 mV(typical) & > V_{SHRT}	X	< OCP	> UVLO	< TSD	H	ON	OFF
Thermal Shutdown	X	X	X	X	None	> UVLO	> TSD	L	OFF	OFF
Host: V_{BUS} OVP Fault	L	L	> OVP	X	None	> UVLO	< TSD	L	OFF	OFF
Host: Data OVP Fault	L	L	X	> OVP	None	> UVLO	< TSD	L	OFF	OFF
Host: OCP Fault	L	L	< OVP & < V_{BUS_SYS} + 200 mV(typical) & > V_{SHRT}	X	> OCP	> UVLO	< TSD	L	CURRENT LIMITED, AUTO-RETRY	AUTO-RETRY
Host: Short-Circuit Fault	L	L	< V_{SHRT}	X	X	> UVLO	< TSD	L	CURRENT LIMITED 250 mA (typical)	OFF
Host: RCP Fault	L	L	< OVP & > V_{BUS_SYS} + 200 mV (typical)	X	X	> UVLO	< TSD	L	ON	ON
OTG: Data OVP Fault	H	L	X	> OVP	None	> UVLO	< TSD	L	OFF	OFF
Power Only: V_{BUS} OVP Fault	L	H	> OVP	X	None	> UVLO	< TSD	L	OFF	OFF
Power Only: OCP Fault	L	H	X	X	> OCP	> UVLO	< TSD	L	CURRENT LIMITED, AUTO-RETRY	OFF
Power Only: Short-Circuit Fault	L	H	< V_{SHRT}	X	X	> UVLO	< TSD	L	CURRENT LIMITED 250 mA (typical)	OFF
Power Only: RCP Fault	L	H	< OVP & > V_{BUS_SYS} + 200 mV (typical)	X	X	> UVLO	< TSD	L	ON	OFF

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPD3S716-Q1 offers fully featured automotive USB2.0 protection including short-to-battery, overcurrent, and ESD protection. Care must be taken during the implementation to make sure the device provides adequate protection to the system.

9.2 Typical Application

Figure 9-1 shows a fully featured USB2.0 high speed port, with an 18-V short-to-battery requirement on the connector side.

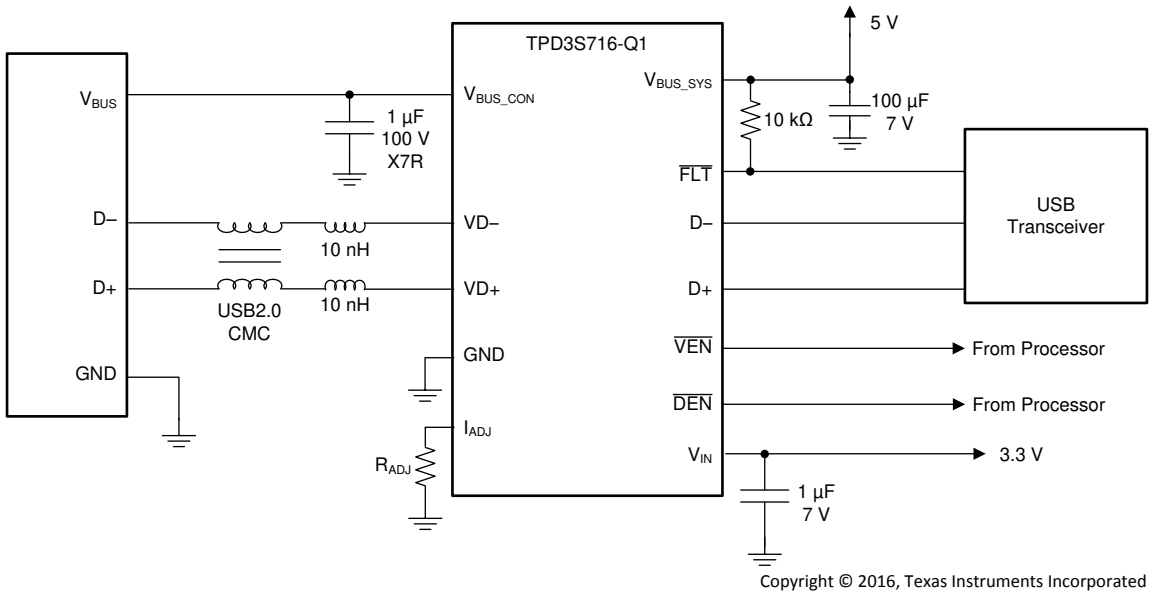


Figure 9-1. Typical Application Configuration for TPD3S716-Q1

9.2.1 Design Requirements

Table 9-1 shows the TPD3S716-Q1 input parameters for this application example.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Short-to-battery tolerance on VD+, VD–, V_{BUS_CON}	18 V
Max current in normal operation on V_{BUS}	1.5 A
Current Limit Setting on V_{BUS}	1.505 A (minimum)
Maximum Ambient Temperature Requirement	105°C
USB Data Rate	480 Mbps

9.2.2 Detailed Design Procedure

The following parameters must be known to the designer to begin the design process:

- Short-to-battery tolerance on connector pins
- Maximum current in normal operation on V_{BUS}
- Maximum operating ambient temperature
- USB Data Rate

9.2.2.1 Short-to-Battery Tolerance

The TPD3S716-Q1 is capable of handling up to 18 V DC on the VD+, VD–, and V_{BUS_CON} pins. In the event of a short-to-battery on V_{BUS_CON}, significant ringing would be expected because of the hot plug-like nature of the short-to-battery event. In typical ceramic capacitor configurations, a standard RLC response is expected which results in a ringing of nearly two times the applied DC voltage. The TPD3S716-Q1 is capable of withstanding the transient ringing from hot plug-like events, assuming some precautions are taken.

Careful capacitor selection on the V_{BUS_CON} pin must be observed. A capacitor with a low derating percentage under the applied voltages must be used to prevent excess ringing. In the example, a 1-µF, 100-V tolerant ceramic X7R capacitor is used. It is best practice to carefully select the capacitors used in this circuit to prevent derating-based voltage spikes under hot plug events. See Figure 9-4 and Figure 9-5 to compare ringing of a 50-V capacitor to a 100-V capacitor. Figure 9-6 shows the 100-V capacitor with the TPD3S716-Q1 installed.

Another alternative to a high rated ceramic capacitor is to implement either a standard R-C snubber circuit, or a small external TVS diode. Depending on the short-to-battery tolerance needed, no special precautions may be needed.

9.2.2.2 Maximum Current on V_{BUS}

The TPD3S716-Q1 is capable of operating up to 2.4 A maximum DC current. In this example, the maximum current for USB2.0 BC1.2 of 1.5 A has been chosen.

9.2.2.3 Power Dissipation and Junction Temperature

This section demonstrates how to analyze the power dissipation and junction temperature of the TPD3S716-Q1 to validate that the application requirements of an I_{VBUS} operating current level of 1.5 A and a maximum operating ambient temperature of 105 °C can be met.

It is good design practice to estimate power dissipation and maximum expected junction temperature of TPD3S716-Q1. This is important to insure the device does not go into thermal shutdown in normal operation and that the long term reliability of the device is maintained. Using Equation 4 to Equation 6, the system designer can control choices of the device's proximity to other power dissipating devices and the design of the printed circuit board (PCB). These have a direct influence on maximum junction temperature. Other factors, such as airflow and maximum ambient temperature, are often determined by system considerations. It is important to remember that these calculations do not include the effects of adjacent heat sources, and enhanced or restricted air flow. Addition of extra PCB copper area around these devices is recommended to reduce the thermal impedance and maintain the junction temperature as low as practical.

For TPD3S716-Q1, the operating junction temperature must be kept below 150°C in order to prevent the device from going into thermal shutdown. Equation 4 is used to calculate the junction temperature of the device:

$$T_J = T_A + [(I_{OUT}{}^2 \times R_{ON}) \times R_{\theta JA}] \quad (4)$$

where

- I_{OUT} = Rated OUT pin current (A)
- R_{ON} = Power path on-resistance at an assumed T_J (Ω)
- T_A = Maximum ambient temperature (°C)
- T_J = Maximum junction temperature (°C)
- $R_{\theta JA}$ = Thermal resistance (°C/W)

This application example requires an I_{VBUS} operating current level of 1.5 A. TPD3S716-Q1 has maximum junction temperature derating requirements depending on the maximum operating current of the device according to Equation 5:

$$T_{J(MAX)} = –15.6 × (I_{VBUS(MAX\ OPERATING)}) + 161.5\ (°C) \quad (5)$$

where

- $T_{J(MAX)}$ = Maximum allowed junction temperature (°C)
- $I_{VBUS(MAX\ OPERATING)}$ = Maximum I_{VBUS} operating current (A)

See Figure 9-7 for a plot of the reliability curve equation. Using this equation, 138.1°C is the maximum allowed junction temperature in this application.

This example requires a maximum operating ambient temperature of 105°C. To determine if this can be supported using Equation 4, the maximum V_{BUS} path R_{ON} must be determined. Equation 6 calculates the maximum V_{BUS} path R_{ON} possible for TPD3S716-Q1 for a given junction temperature:

$$R_{ON(MAX)} = (T_J + 183.15) / 2726.7\ (Ω) \quad (6)$$

where

- $R_{ON(MAX)}$ = Maximum V_{BUS} R_{ON} at a given junction temperature (Ω)
- T_J = Device junction temperature (°C)

See Figure 9-8 for a plot of the maximum V_{BUS} path R_{ON} vs. Junction Temperature curve. Using the above equation, the maximum V_{BUS} R_{ON} possible for TPD3S716-Q1 at 138.1°C is $R_{ON(MAX)}$ = 0.118 Ω.

Using the calculated parameters for this example and the standard datasheet $R_{θJA}$ for TPD3S716-Q1, the maximum operating ambient temperature possible in this example is T_A = 111°C. Because this is greater than the application requirement of 105°C, TPD3S716-Q1 can safely be operated at 1.5 A with $R_{θJA}$ = 98.8 (°C/W). If the resulting ambient temperature in the above calculations resulted in a T_A < 105 °C, methods for improving $R_{θJA}$ would need to be taken. See the *Layout Optimized for Thermal Performance* section for guidelines on improving $R_{θJA}$ for TPD3S716-Q1. The example given in the *Layout Optimized for Thermal Performance* yields an $R_{θJA}$ = 57 (°C/W). Excellent thermal performance of TPD3S716-Q1 can be achieved with the proper PCB layout.

9.2.2.4 USB Data Rate

The TPD3S716-Q1 is capable of operating at the maximum USB2.0 High Speed data rate of 480-Mbps because of the high data switch bandwidth of 1-GHz (typical). In this design example the maximum data rate of 480-Mbps has been chosen.

9.2.3 Application Curves

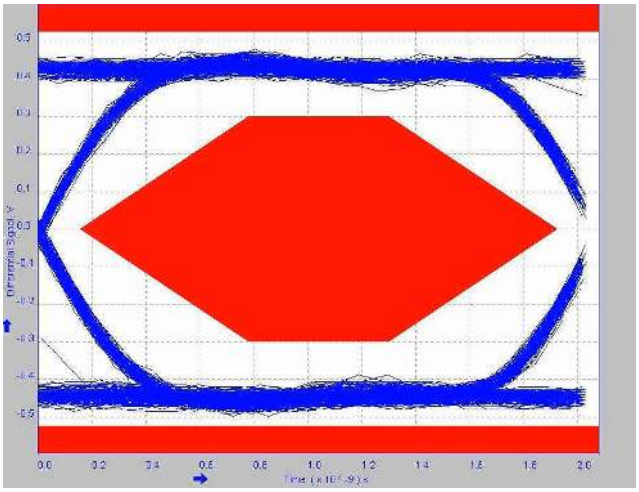


Figure 9-2. USB2.0 Eye Diagram (Board only, Through Path)

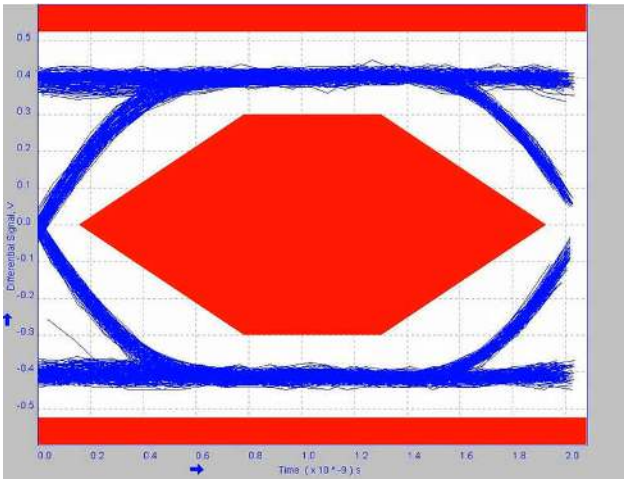


Figure 9-3. USB2.0 Eye Diagram (System from Typical Application Schematic)

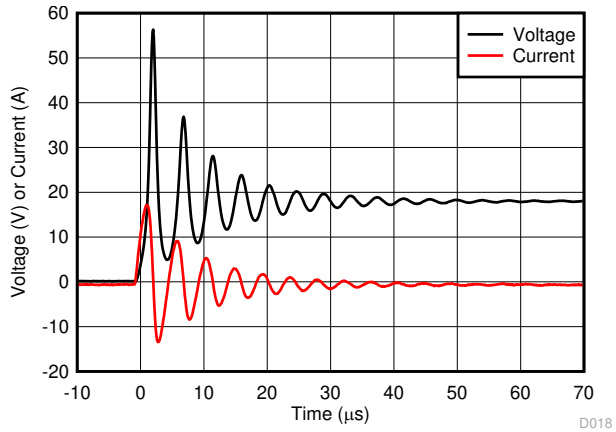


Figure 9-4. 50-V, 1-µF X7R Ceramic Shorted to 18-V (Not Recommended)

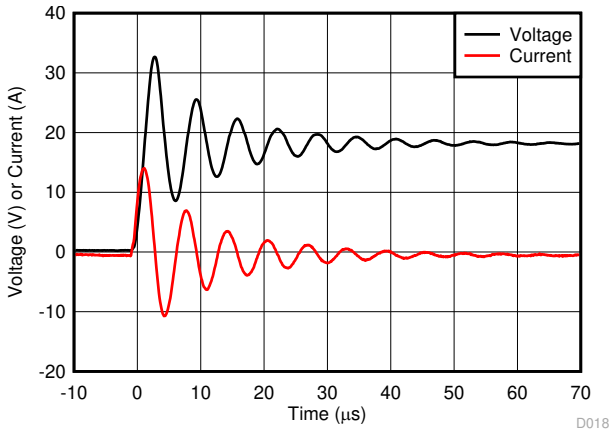


Figure 9-5. 100-V, 1-µF X7R Ceramic Shorted to 18 V

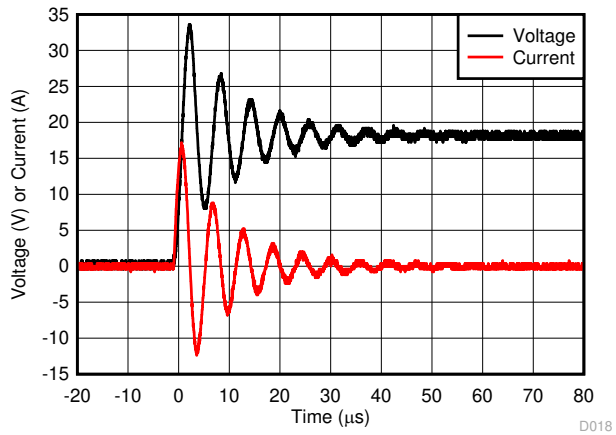


Figure 9-6. TPD3S716-Q1 and 100-V, 1-µF X7R Shorted to 18 V (Powered Off)

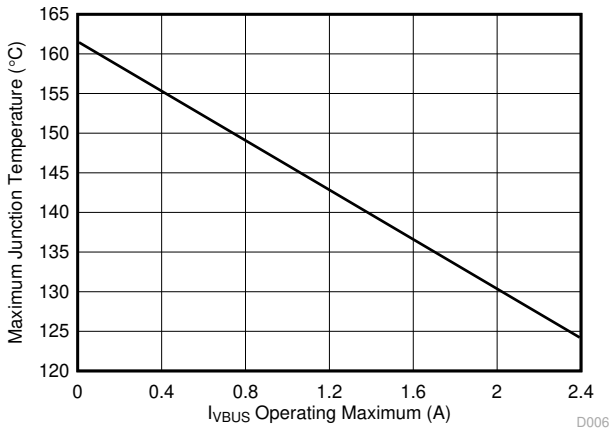


Figure 9-7. TPD3S716-Q1 I_{VBUS} Temperature Derating Curve

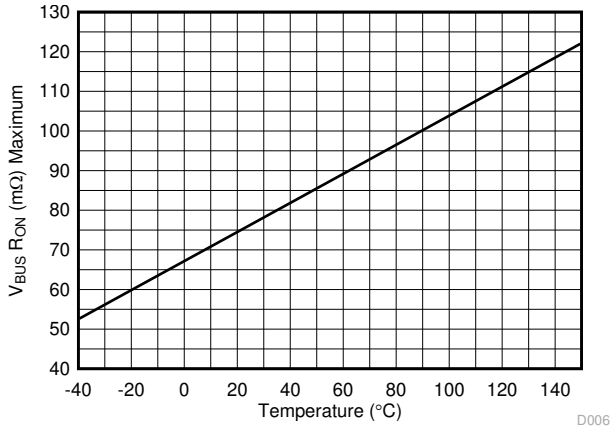


Figure 9-8. TPD3S716-Q1 Maximum V_{BUS} R_{ON} vs. Junction Temperature

10 Power Supply Recommendations

10.1 V_{BUS} Path

The V_{BUS_SYS} pins provide power to the chip and supply current through the load switch to V_{BUS_CON}. A 100-µF bulk capacitor is recommended on V_{BUS_SYS} to supply the USB port and maintain compliance. A 1-µF capacitor is recommended on the V_{BUS_CON} pin with adequate voltage rating to tolerate short-to-battery conditions. A supply voltage above the UVLO threshold for V_{BUS_SYS} must be supplied for the device to power on.

10.2 V_{IN} Pin

The V_{IN} pin provides a voltage reference for the data switch OVP level as well as a bypass for ESD clamping. A 1-µF capacitor must be placed as close to the pin as possible and the supply must be set to be above the UVLO threshold for V_{IN}.

11 Layout

11.1 Layout Guidelines

Proper routing and placement maintains signal integrity for high-speed signals. The following guidelines apply to the TPD3S716-Q1:

- Place the bypass capacitors as close as possible to the V_{IN}, V_{BUS_SYS}, and V_{BUS_CON} pins. Capacitors must be attached to a solid ground. This minimizes voltage disturbances during transient events such as short-to-battery, ESD, or overcurrent conditions.
- High speed traces (data switch path) must be routed as straight as possible and any sharp bends must be minimized.

Standard ESD recommendations apply to the VD+, VD–, and V_{BUS_CON} pins as well:

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Example

Figure 11-1 shows a full layout for a standard USB2.0 port. A common mode choke and inductors are used on the high speed data lines, and the requisite bypassing caps are placed on V_{BUS_CON}, V_{BUS_SYS}, and V_{IN}.

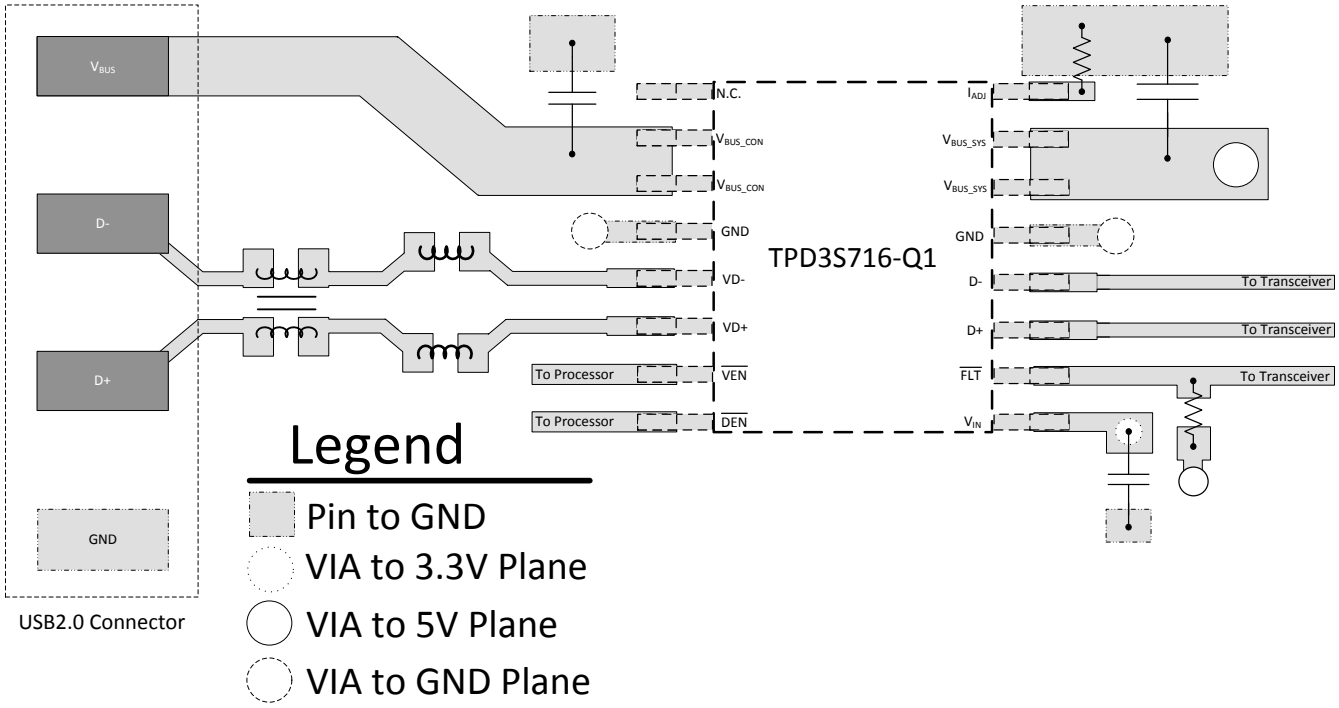


Figure 11-1. Typical Layout Example for TPD3S716-Q1

11.3 Layout Optimized for Thermal Performance

Figure 11-2 and Figure 11-3 show images from a real PCB design optimized for the best thermal performance for TPD3S716-Q1. This PCB layout has 6 layers (2 signal and 4 plane layers). The 2 signal layers are the outer layers of the PCB and constructed with 2-oz copper, and the 4 internal plane layers are constructed with 1-oz copper. Using this PCB layout yielded an $R_{\theta JA(CUSTOM)}$ = 57 (°C/W). The images contain rough dimensions of the copper traces and pours used around the device. One key strategy to optimize thermal performance of the device is to maximize the area of the copper pours and traces used to route the device power, GND, and signal pins when possible. Another key strategy is to maximize the copper weight of the PCB metal layers. This example demonstrates that excellent thermal performance can be achieved with TPD3S716-Q1 with the proper PCB layout.

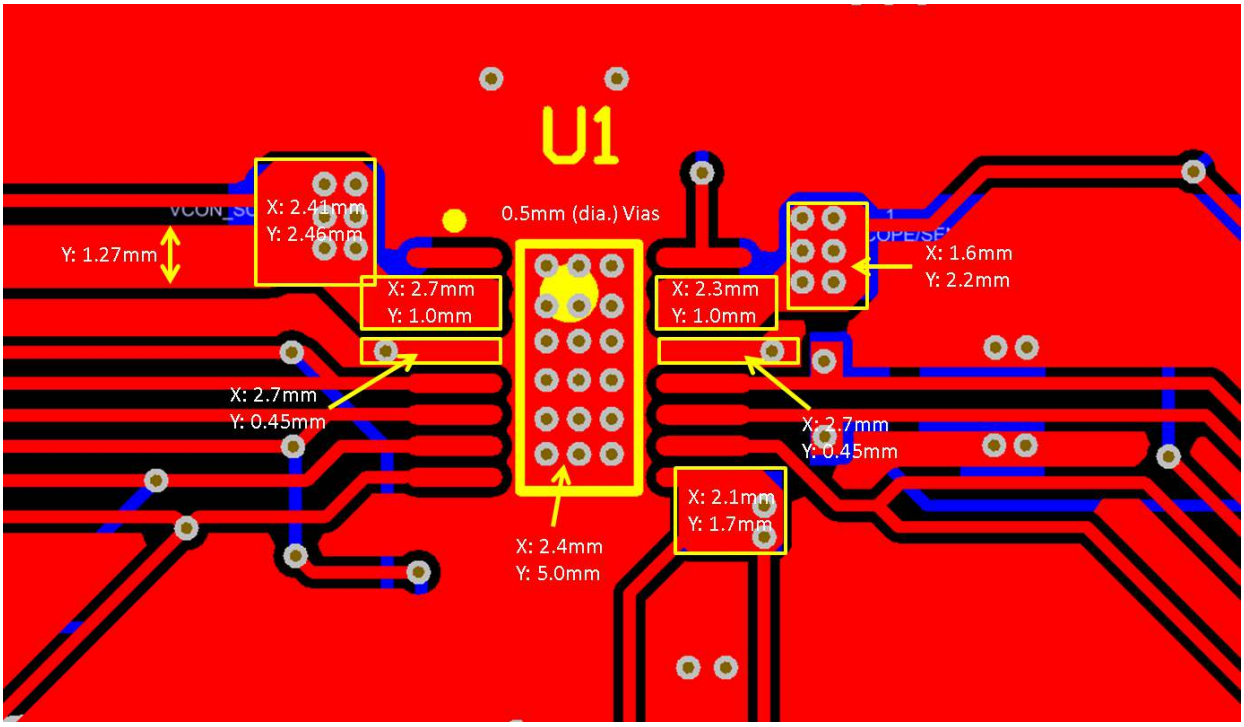


Figure 11-2. Thermally Optimized PCB Layout Top Layer

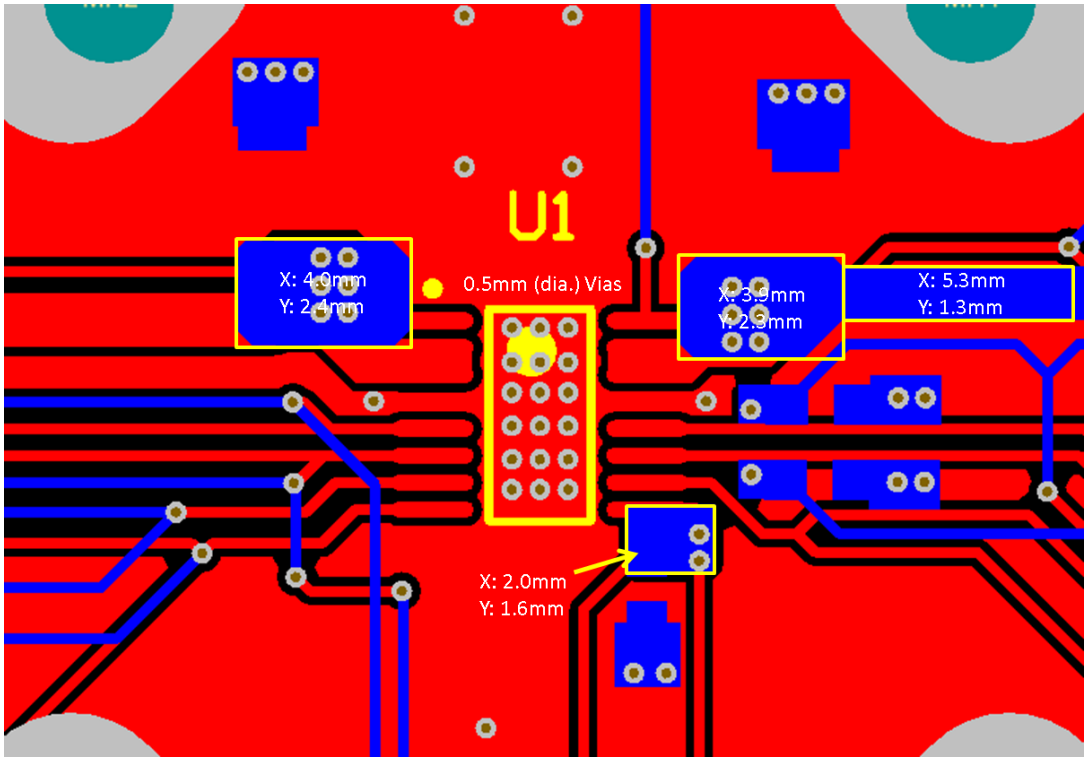


Figure 11-3. Thermally Optimized PCB Layout Bottom Layer

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

TPD3S716-Q1 Evaluation Module, SLVUAL9

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD3S716QDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RJ716Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

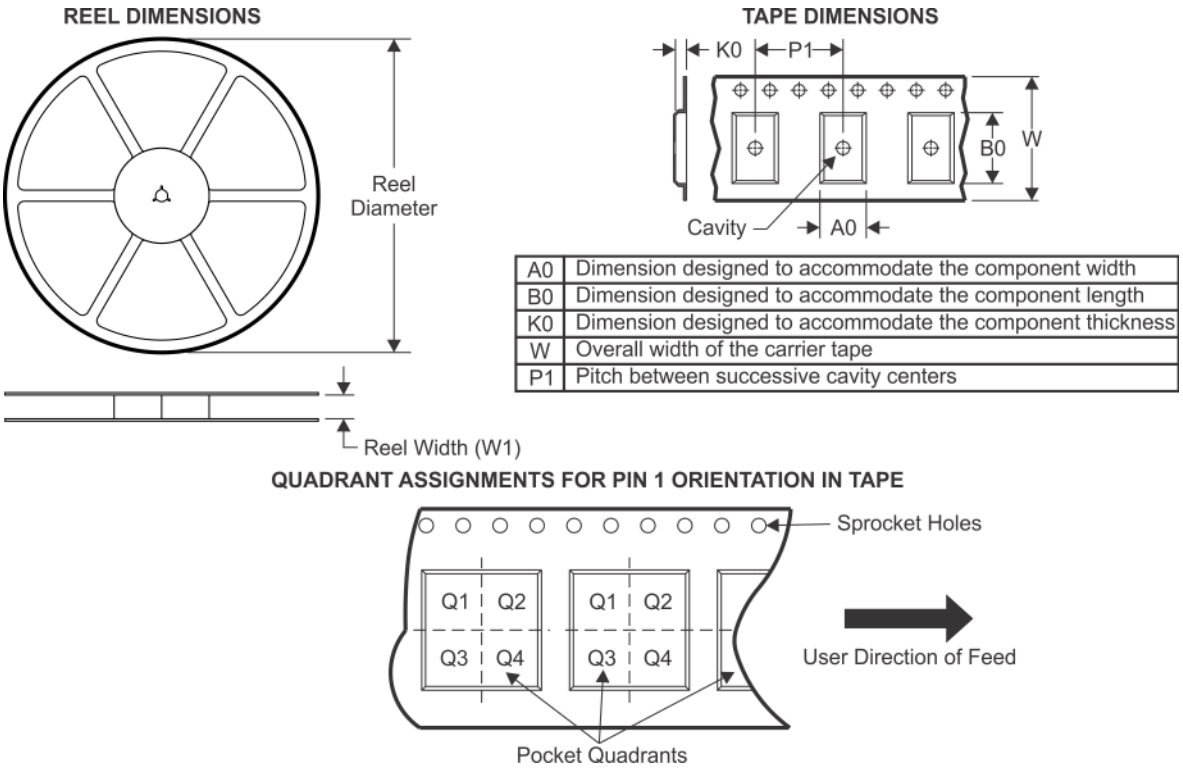
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

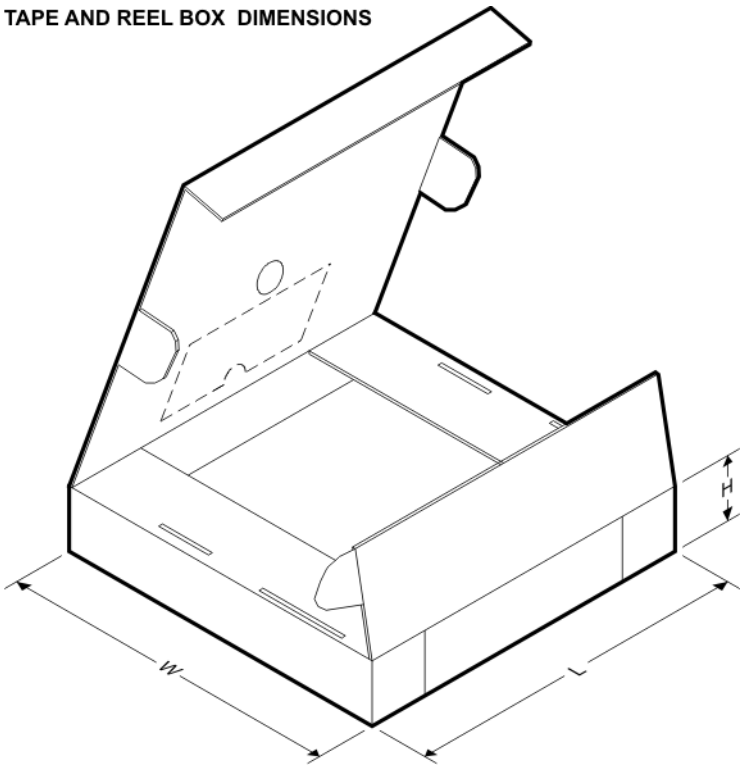


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD3S716QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

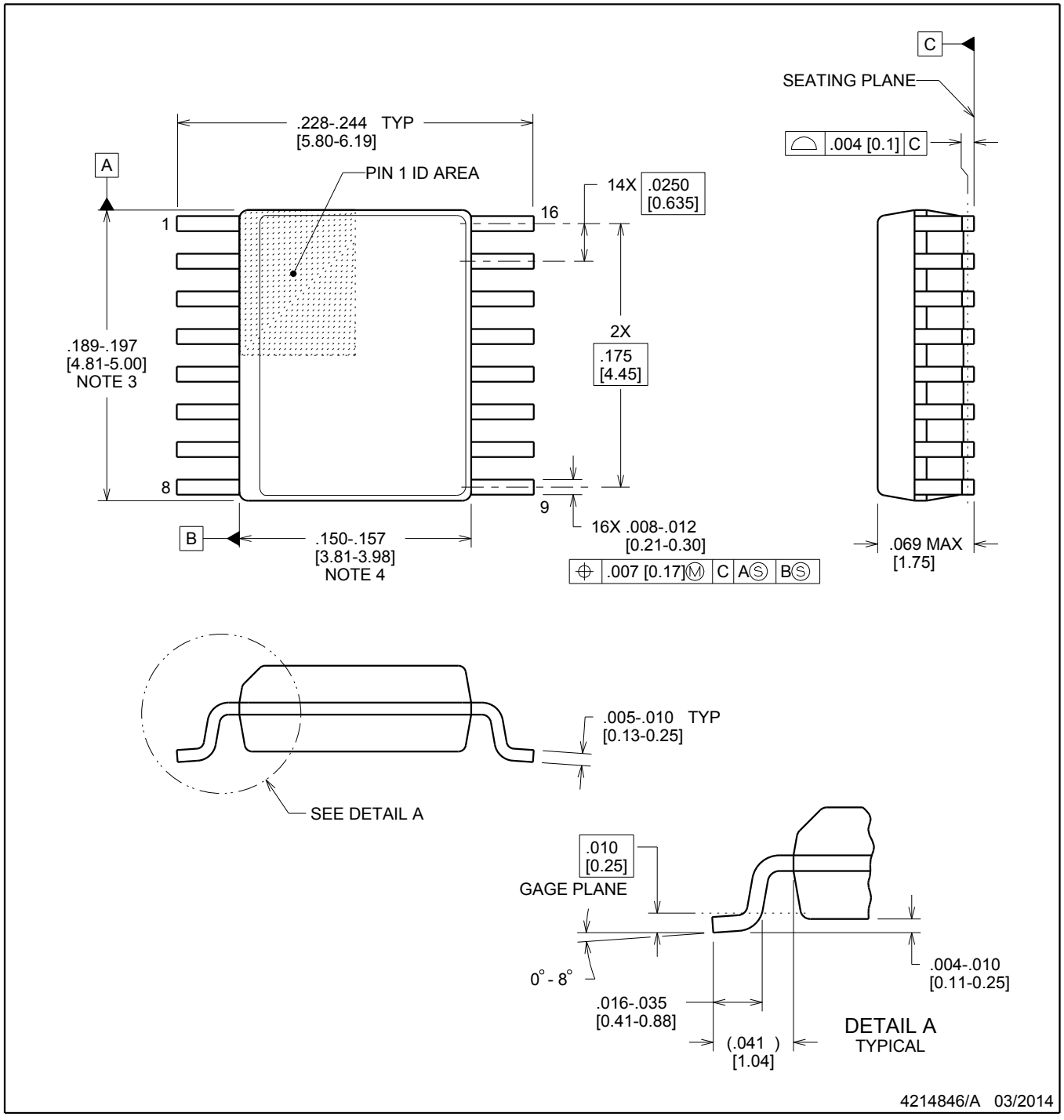
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD3S716QDBQRQ1	SSOP	DBQ	16	2500	367.0	367.0	35.0

PACKAGE OUTLINE

DBQ0016A

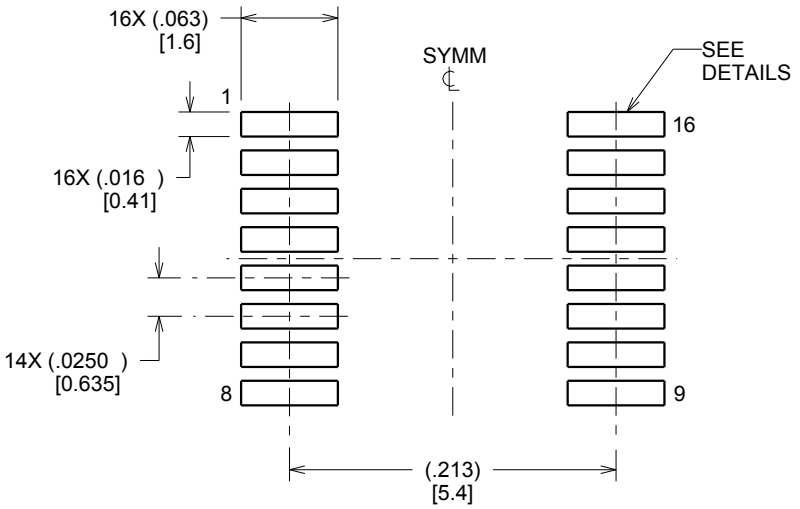
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

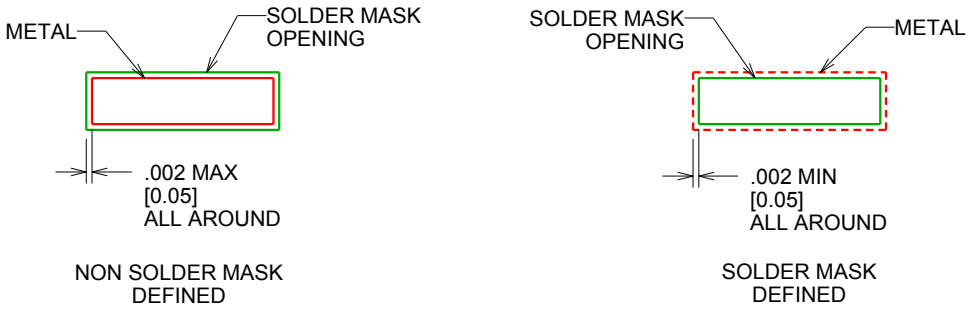


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

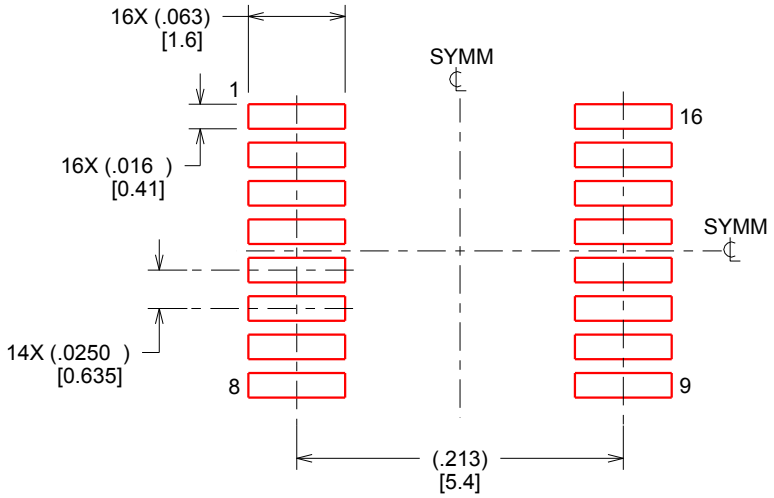


SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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