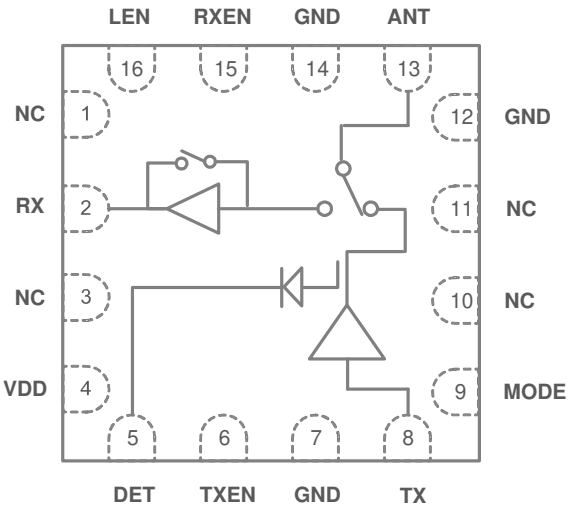
CMOS 5GHz WLAN 802.11ac RFeIC WITH PA, LNA AND SPDT



Description

RFX8050 is a highly integrated, single-chip, single-die RFeIC (RF Front-end Integrated Circuit) which incorporates key RF functionality needed for IEEE 802.11a/n/ac WLAN system operating in the 4.9-5.85GHz range. The RFX8050 architecture integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network, LO rejection, and harmonic filters all in a CMOS single-chip device.

RFX8050 has simple and low-voltage CMOS control logic, and requires minimal external components. A directional coupler based power detect circuit is also integrated for accurate monitoring of output power from the PA.

RFX8050 is assembled in an ultra-compact low-profile 2.5x2.5x0.45 mm 16-lead QFN package. With support to direct battery operation, the RFX8050 is ideal RF front-end solution for implementing 5GHz WLAN in smartphones and other mobile platforms.

Applications

- 802.11a/n/ac
- Smartphones
- Tablets/MIDs
- Gaming
- Notebook/Netbook/Ultrabooks
- Mobile/Portable Devices
- Consumer Electronics
- Other 5GHz ISM Platforms

FEATURES

- 5GHz WLAN Single Chip, Single-Die RF Front-End IC
- High Transmit Signal Linearity Meeting Standards for 802.11ac OFDM /MCS9 Modulation
- Separate TX and RX Transceiver Port and Single Antenna Port
- 5GHz Power Amplifier with Low-Pass Harmonic Filter
- Low Noise Amplifier with Bypass Mode
- Transmit/Receive Switch Circuitry
- Integrated Power Detector for Transmit Power Monitor and Control
- Low Voltage (1.2V) CMOS Control Logic
- Low-Current Mode in TX for Battery Current Savings
- ESD Protection Circuitry on All Pins
- DC Decoupled RF Ports
- Internal RF Decoupling on All VDD Bias Pins
- Low Noise Figure for the Receive Chain
- High Power Capability for Received Signals in Bypass Mode
- Very Low DC Power Consumption
- Full On-chip Matching Circuitry
- Minimal External Components Required
- 50-Ohm Input / Output Matching
- Market Proven CMOS Technology
- 2.5mm x 2.5mm x 0.45mm Small Outline 16L QFN Package with Exposed Ground Pad

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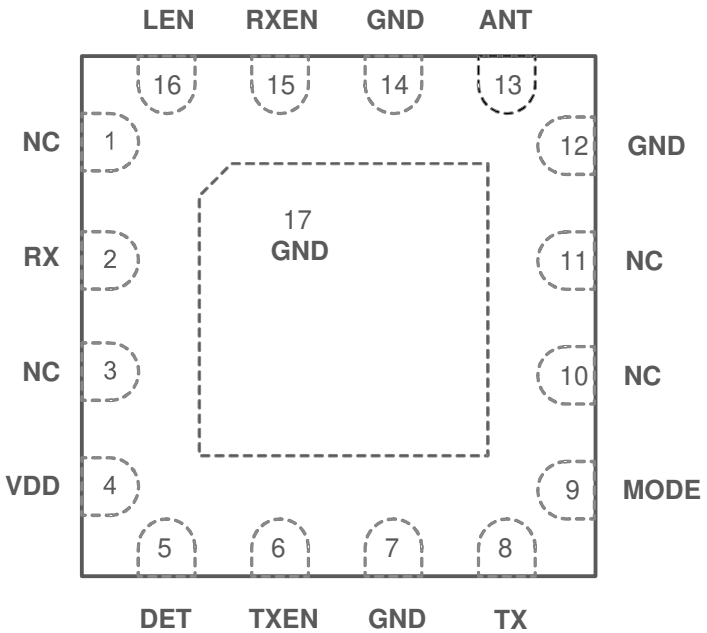
PIN ASSIGNMENTS:

Pin Number	Pin Name	Description
1, 3, 10, 11	NC	Internally Not Connected
2	RX	RF Output Port from LNA or Bypass – DC Shorted to GND
4	VDD	DC Supply Voltage
5	DET	Analog Voltage Proportional to the PA Power Output
6	TXEN	CMOS Input to Control TX Enable
8	TX	RF Input Port from the Transceiver – DC Shorted to GND
9	MODE	CMOS Input to Control High-Linearity/Low-Current Mode
13	ANT	Antenna Port RF Signal from the PA or RF Signal Applied to the LNA; DC Shorted to GND
15	RXEN	CMOS Input to Control RX Enable
16	LEN	CMOS Input to Control LNA Enable or Bypass Mode
7, 12, 14	GND	Ground – Must Be Connected to GND in the Application Circuit

PIN-OUT DIAGRAM:



(Top "See-Through" View)

ABSOLUTE MAXIMUM RATINGS:

Parameters	Units	Min	Max	Conditions
DC VDD Voltage Supply	V	0	5.0	All VDD Pins
DC Control Pin Voltage	V	0	3.6	All Control Pins
DC VDD Current Consumption	mA		400	Through VDD Pins when TX is "ON"
TX RF Input Power	dBm		+7	
ANT RF Input Power	dBm		+10	Bypass Mode
Junction Temperature	°C		135	
Storage Ambient Temperature	°C	-40	+125	Appropriate care required according to JEDEC Standards
Operating Ambient Temperature	°C	-40	+85	

Note: Sustained operation at or above the Absolute Maximum Ratings for any one or combinations of the above parameters may result in permanent damage to the device and is not recommended.

All Maximum RF Input Power Ratings assume 50-Ohm terminal impedance.

NOMINAL OPERATING CONDITIONS:

Parameters	Units	Min	Typ	Max	Conditions
DC VDD Voltage Supply *(Note 1)*	V	3.0	3.6	4.8	All VDD Pins
Control Voltage "High" *(Note 2)*	V	1.2		*	* 3.6V or VDD Whichever is Lower
Control Voltage "Low"	V	0		0.3	
DC Control Pin Current Consumption	µA		1		
DC Shutdown Current	µA		3		All Control Lines "Low"
PA Turn On/Off Time	µsec		0.5	1	
LNA Turn On/Off Time	µsec		0.5	1	
Shut-Down and "ON" State Switching Time	µsec		0.5	1	

Note 1: For normal operation of the RFX8050, VDD must be continuously applied to all VDD supply pins.
Note 2: If control voltage can exceed 1.8V, a 1KΩ – 10KΩ series resistor is recommended for the application circuit on each control line.

TRANSMIT PATH CHARACTERISTICS (VDD=3.6V; T=+25 °C)

Parameters	Units	Min	Typ	Max	Conditions
Operating Frequency Band	GHz	4.9		5.85	
Linear Output Power for 802.11ac	dBm		+16		High Linearity Mode, For EVM<1.8%, MCS9/256QAM/80MHz
Linear Output Power for 802.11a	dBm		+17		High Linearity Mode, EVM<3%, 64QAM/54Mbps/20MHz
			+15.5		Low Current Mode, EVM<3%, 64QAM/54Mbps/20MHz
Small-Signal Power Gain	dB		28		High Linearity Mode, Between TX and ANT pins
			27		Low Current Mode, Between TX and ANT Pins
TX Quiescent Current	mA		145		High Linearity Mode
			100		Low Current Mode
TX Linear Current	mA		205		P_{OUT} = +17dBm, High Linearity Mode, 20 MHz
			155		P_{OUT} = +17dBm, Low Current Mode, 20MHz
Power Detector Voltage Output	mV		200 - 1000		P_{OUT} = +5 to +20dBm, 10kΩ Load
Second Harmonic	dBm/MHz		-30		P_{OUT}=+20dBm HT20/MCS0
Third Harmonic	dBm/MHz		-35		P_{OUT}=+20dBm HT20/MCS0
Input Return Loss	dB		-12		At TX Port
Output Return Loss	dB		-12		At ANT Port
Load VSWR for Stability (CW, Fix Pin for Pout=+20dBm with 50Ω load)	N/A	4:1	6:1		All non-harmonically related spurs less than -43dBm/MHz
Load VSWR for Ruggedness (CW, Fix Pin for Pout=+20dBm with 50 Ohm Load)	N/A	8:1	10:1		No Damage

RECEIVE PATH CHARACTERISTICS (VDD=3.6V; T=+25 °C)

Parameters	Units	Min	Typ	Max	Conditions
Operating Frequency Band	GHz	4.9		5.85	All RF Pins are Loaded by 50-Ohm
Gain	dB		12		High Gain Mode, Between ANT and RX pins; RXEN=LEN="High"
Noise Figure	dB		3.6		High Gain Mode, At ANT Pin
Insertion Loss for LNA Bypass Mode	dB		6		Between ANT and RX Pins; RXEN="High", LEN="Low"
Input Return Loss	dB		-10		At ANT Port, High Gain Mode
			-10		Bypass Mode
Output Return Loss	dB		-10		At RX Port, High Gain Mode
			-10		Bypass Mode
RF Port Impedance	Ohm		50		
DC Quiescent Current	mA		13		No RF Applied, Through VDD, High Gain Mode
			1.2		No RF Applied, Through VDD, Bypass Mode
Input P_{1dB}	dBm		-5		At ANT Pin, High-Gain Mode
			+10		At ANT Pin, Bypass Mode

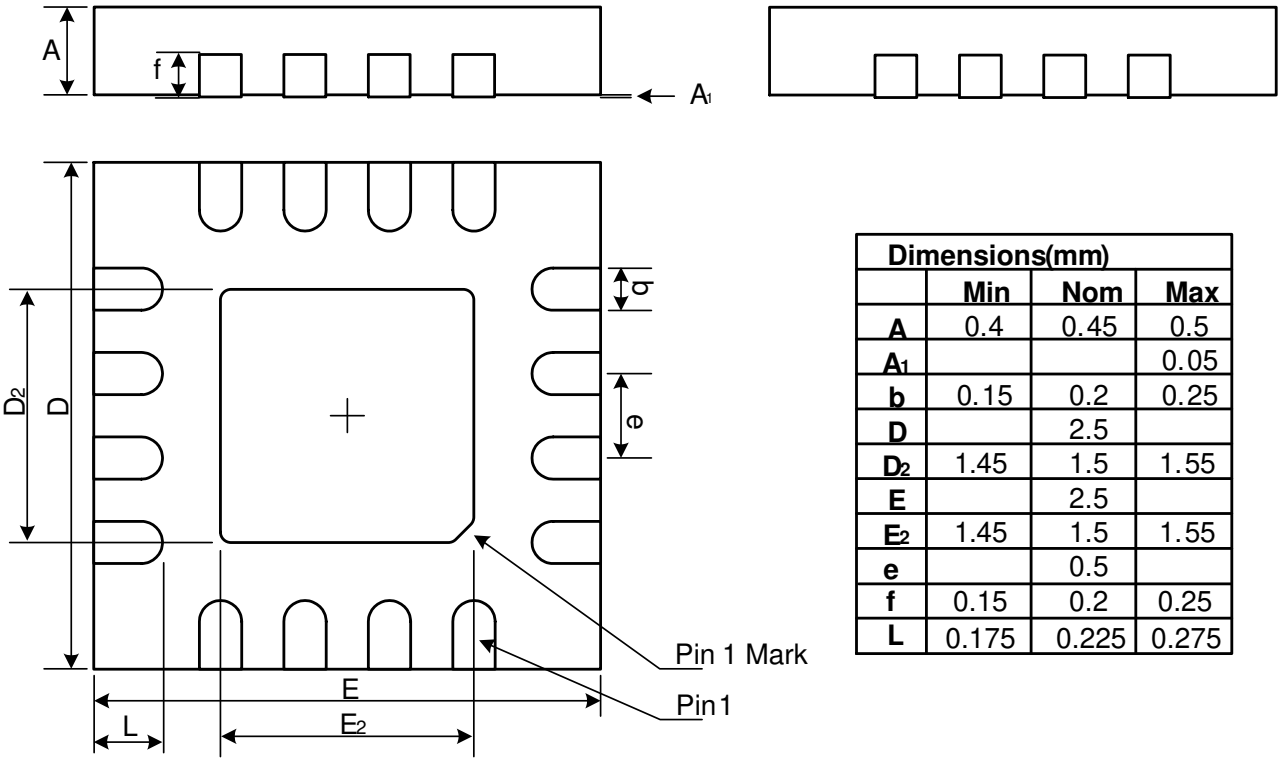
CONTROL LOGIC TRUTH TABLE

TXEN	LEN	RXEN	MODE	Mode Of Operation
0	0	0	0	Shutdown Mode
1	X	X	0	Transmit Mode, High-Linearity
1	X	X	1	Transmit Mode, Low-Current
0	1	1	X	Receive Mode, High-Gain
0	0	1	X	Receive Mode, Bypass
All Others				Unsupported (No Damage)

Note: "1" denotes high voltage state (> 1.2V)
"0" denotes low voltage state (<0.3V) at Control Pins

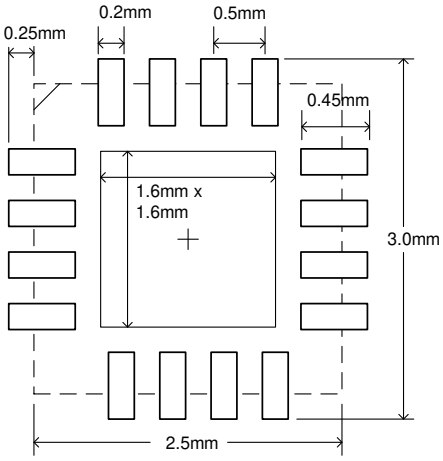
"X" denotes the don't care state
1KΩ – 10KΩ series resistor may be required for each control line

PACKAGE DIMENSIONS (All Dimensions in mm):

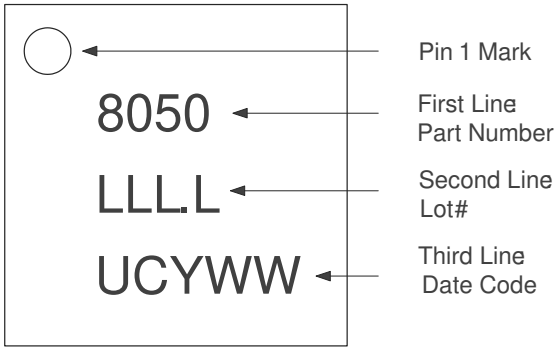


Dimensions(mm)			
	Min	Nom	Max
A	0.4	0.45	0.5
A_1			0.05
b	0.15	0.2	0.25
D		2.5	
D_2	1.45	1.5	1.55
E		2.5	
E_2	1.45	1.5	1.55
e		0.5	
f	0.15	0.2	0.25
L	0.175	0.225	0.275

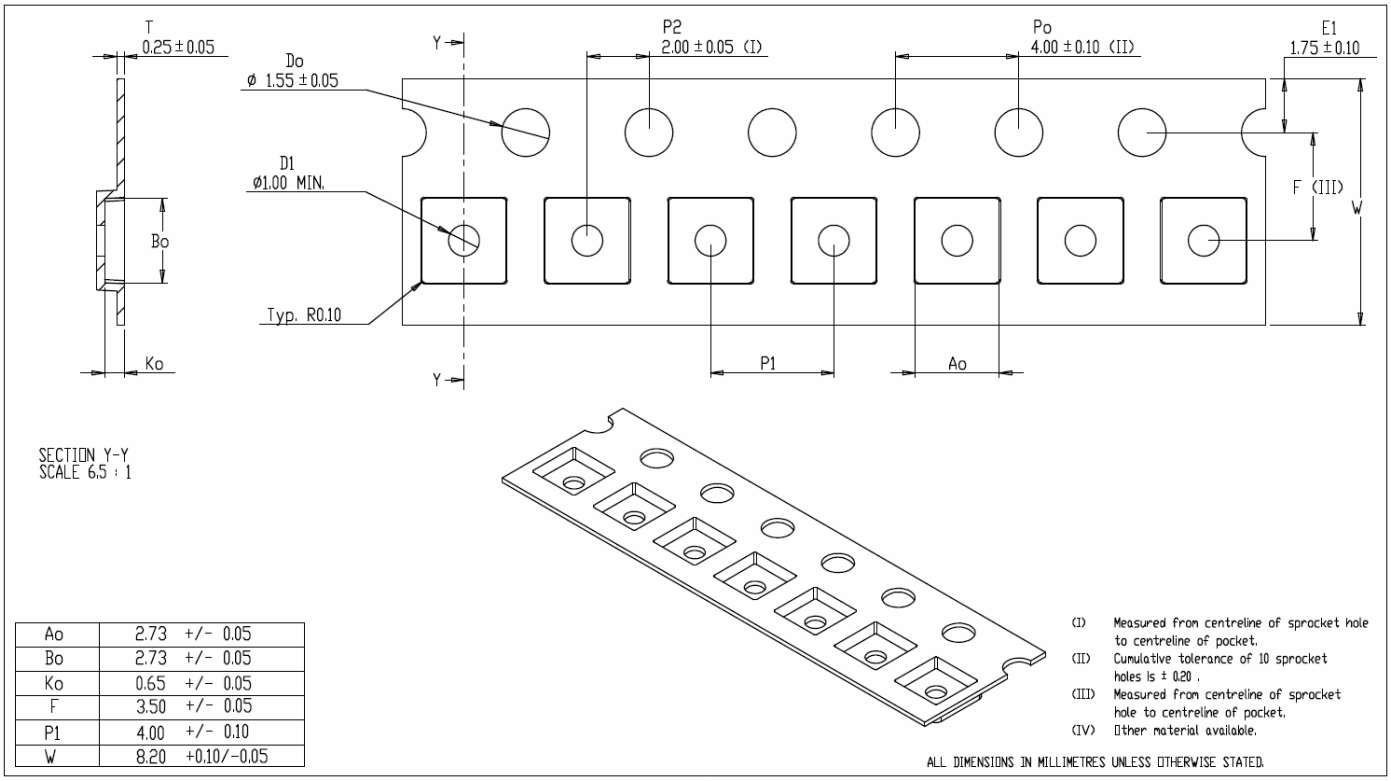
PCB LAND PATTERN



PACKAGE MARKING



TAPE SPECIFICATION



Ao	2.73	+/- 0.05
Bo	2.73	+/- 0.05
Ko	0.65	+/- 0.05
F	3.50	+/- 0.05
P1	4.00	+/- 0.10
W	8.20	+0.10/-0.05

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.