

## N-channel 400 V, 3 Ω typ., 1.8 A SuperMESH3™ Power MOSFET in a SOT-223 package

Datasheet - production data

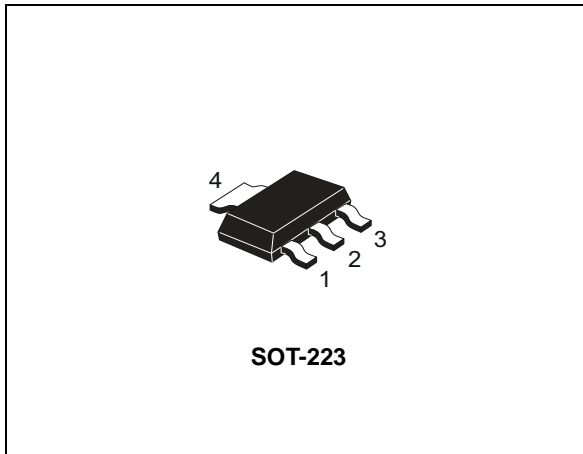
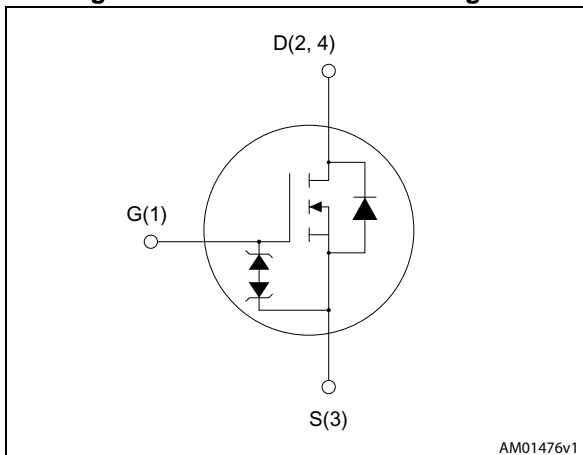


Figure 1. Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>TOT</sub>
STN3N40K3	400V	3.4 Ω	1.8 A	3.3W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

### Application

- Switching applications

### Description

This SuperMESH3™ Power MOSFET is the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Table 1. Device summary

Order code	Marking	Package	Packaging
STN3N40K3	3N40K3	SOT-223	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain source voltage	400	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current continuous $T_C = 25\text{ }^\circ\text{C}$	1.8 <sup>(1)</sup>	A
$I_D$	Drain current continuous $T_C = 100\text{ }^\circ\text{C}$	1 <sup>(1)</sup>	A
$I_{DM}$ <sup>(2)</sup>	Drain current pulsed	7.2	A
$I_{AR}$ <sup>(3)</sup>	Avalanche current, repetitive or not repetitive	0.6	A
$E_{AS}$ <sup>(4)</sup>	Single pulse avalanche energy	45	mJ
$P_{TOT}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	3.3	W
$dv/dt$ <sup>(5)</sup>	Peak diode recovery voltage slope	12	V/ns
$E_{SD}$	Gate-source human body model ( $R = 1.5\text{ k}\Omega$ , $C = 100\text{ pF}$ )	1	kV
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Drain current limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. Pulse width limited by  $T_{Jmax}$ .
4. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .
5.  $I_{sd} \leq 1.8\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 80\% V_{(BR)DSS}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-amb}$ <sup>(1)</sup>	Thermal resistance junction-amb max.	37.9	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 30\text{ s}$

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	400			V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0, V <sub>DS</sub> = 400 V			1	μA
		V <sub>GS</sub> = 0, V <sub>DS</sub> = 400 V, T <sub>C</sub> = 125 °C			50	μA
I <sub>GSS</sub>	Gate-body leakage current	V <sub>DS</sub> = 0, V <sub>GS</sub> = ± 20 V			±10	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 50 μA	3	3.75	4.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.6 A		3.1	3.4	Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 50 V, f = 1 MHz, V <sub>GS</sub> = 0	-	165	-	pF
C <sub>oss</sub>	Output capacitance		-	17	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	3	-	pF
C <sub>oss(er)</sub> <sup>(1)</sup>	Equivalent output capacitance energy related	V <sub>DS</sub> = 0 to 320 V, V <sub>GS</sub> = 0	-	9	-	pF
C <sub>oss(tr)</sub> <sup>(2)</sup>	Equivalent output capacitance time related		-	14	-	pF
R <sub>g</sub>	Intrinsic gate resistance	f=1 MHz open drain	-	10	-	Ω
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 320 V, I <sub>D</sub> = 1.8 A, V <sub>GS</sub> = 10 V (see <a href="#">Figure 18</a> )	-	11	-	nC
Q <sub>gs</sub>	Gate-source charge		-	2	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	7	-	nC

1. Is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>
2. Is defined as a constant equivalent capacitance giving the same storage energy as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn on delay time	$V_{DD} = 200\text{ V}$ , $I_D = 0.6$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17</a> )	-	7	-	ns
$t_r$	Rise time		-	8	-	ns
$t_{d(off)}$	Turn off delay time		-	18	-	ns
$t_f$	Fall time		-	14	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		1.8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		7.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 0.6\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 1.8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 20</a> )	-	145		ns
$Q_r$	Reverse recovery charge		-	490		nC
$I_{RRM}$	Reverse recovery current		-	7		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 1.8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 20</a> )	-	166		ns
$Q_{rr}$	Reverse recovery charge		-	580		nC
$I_{RRM}$	Reverse recovery current		-	7		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics

Figure 2. Safe operating area

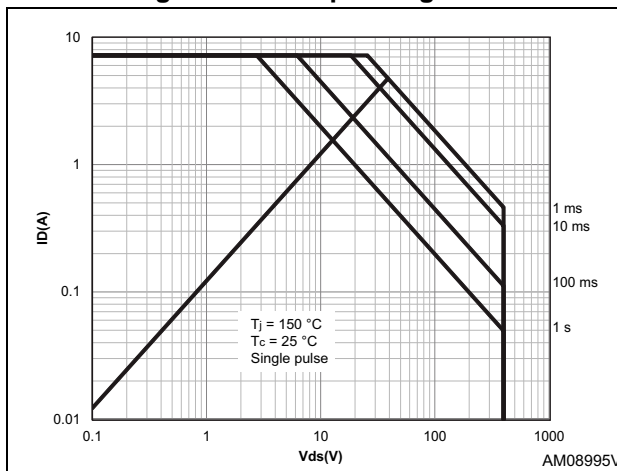


Figure 3. Thermal impedance

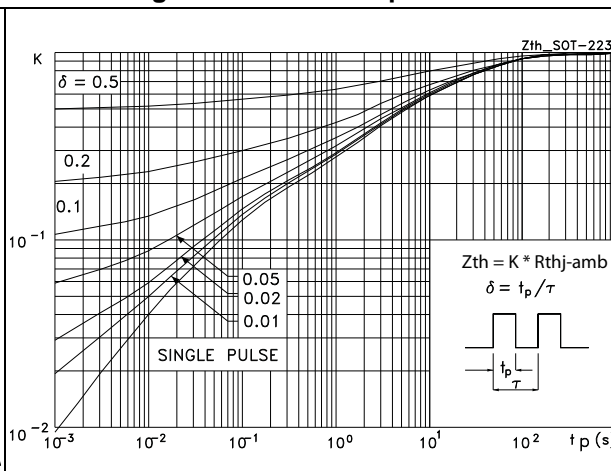


Figure 4. Output characteristics

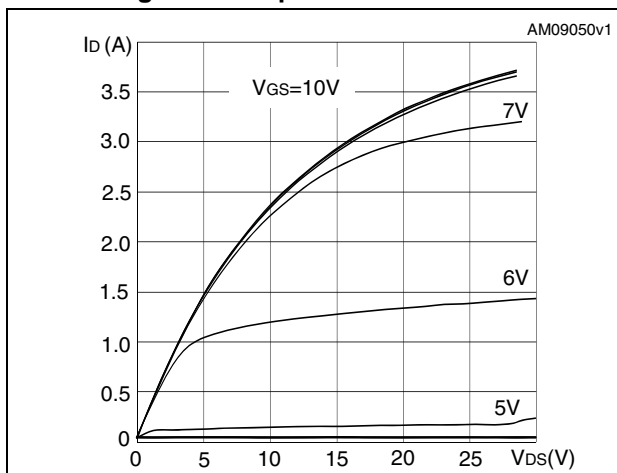


Figure 5. Transfer characteristics

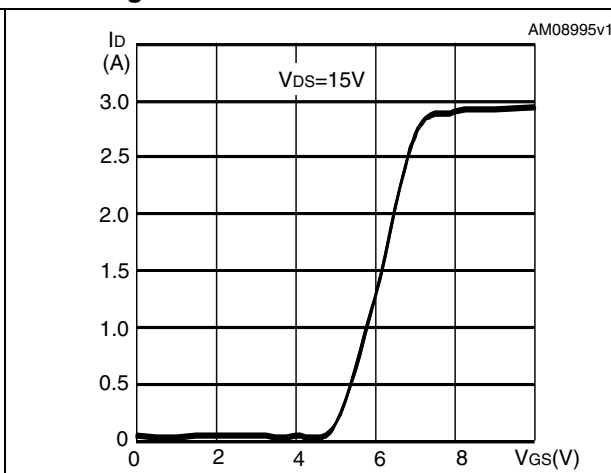


Figure 6. Gate charge vs gate-source voltage

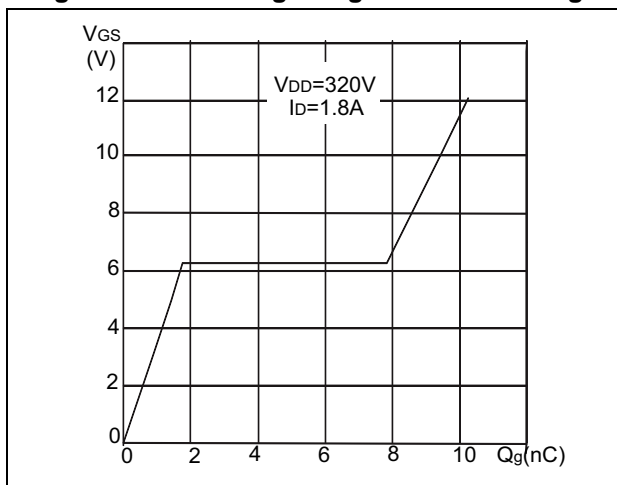


Figure 7. Static drain-source on resistance

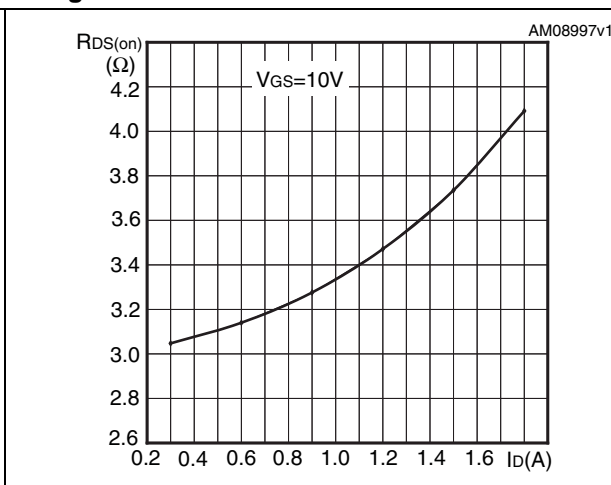


Figure 8. Capacitance variations

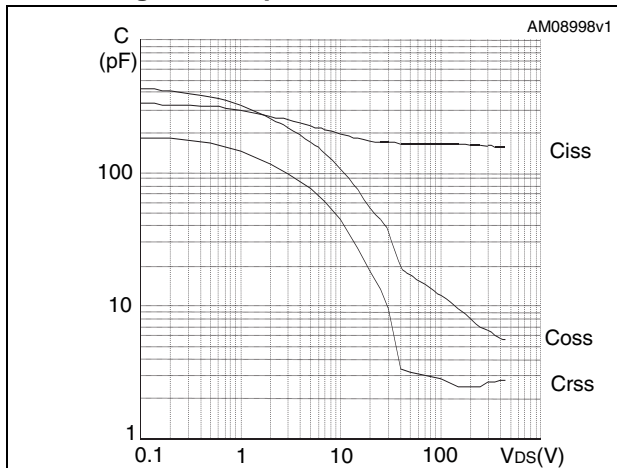


Figure 9. Output capacitance stored energy

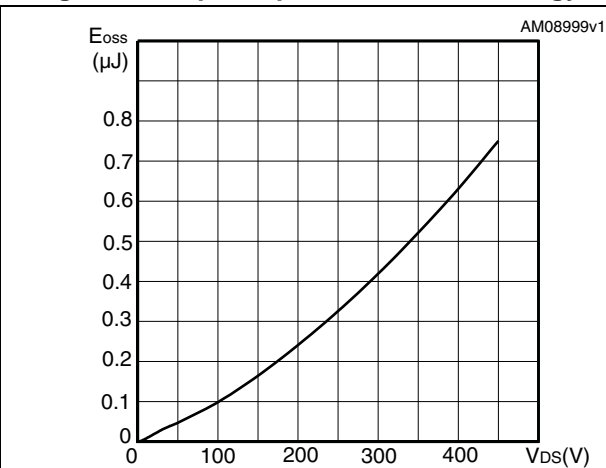


Figure 10. Normalized gate threshold voltage vs. temperature

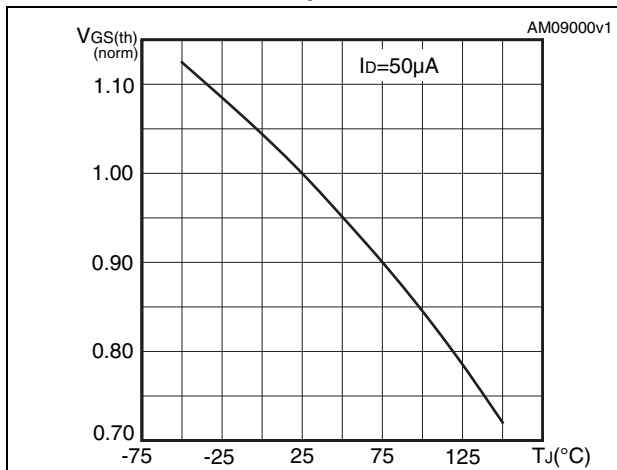


Figure 11. Normalized on resistance vs. temperature

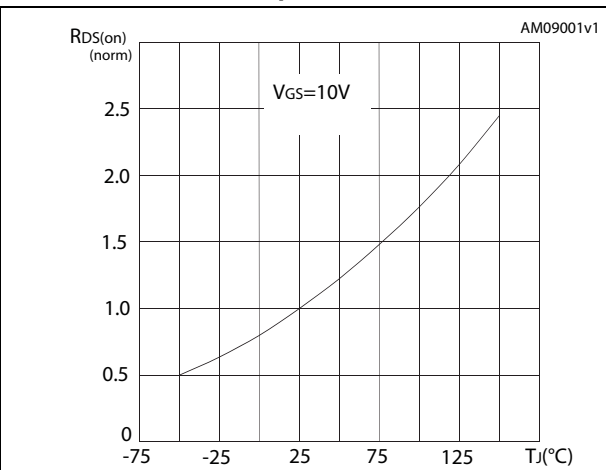


Figure 12. Source-drain diode forward characteristics

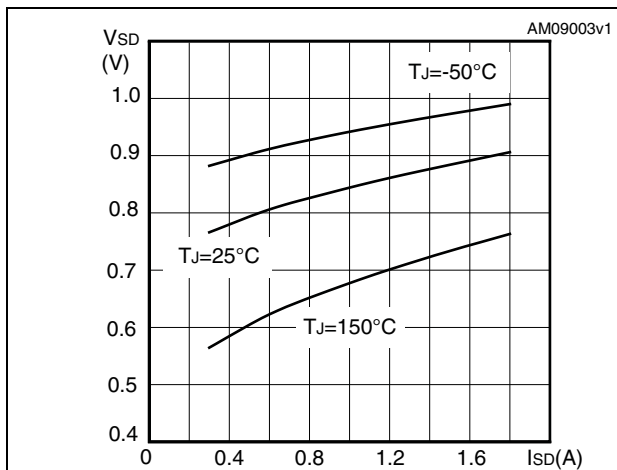


Figure 13. Normalized V(BR)DSS vs. temperature

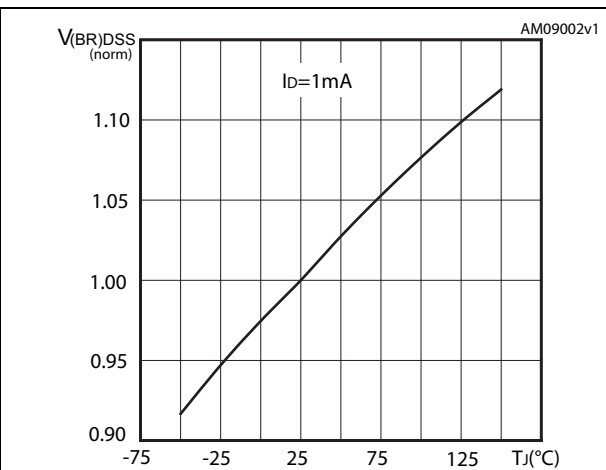
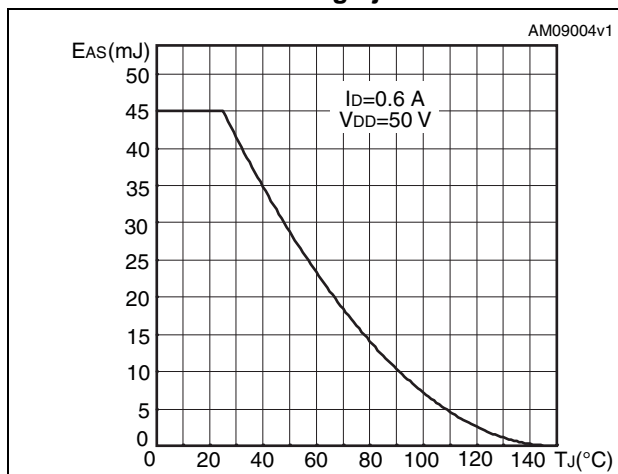


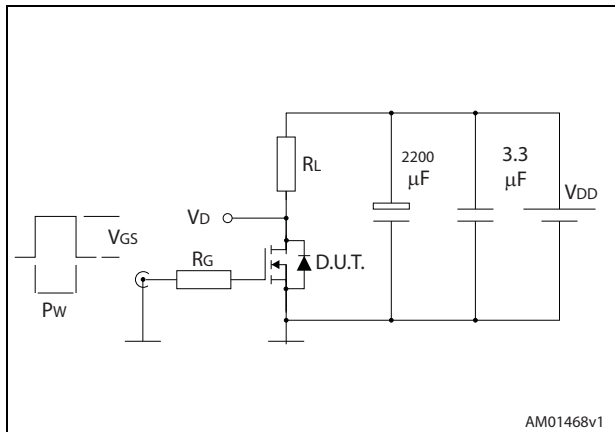
Figure 14. Maximum avalanche energy vs. starting Tj





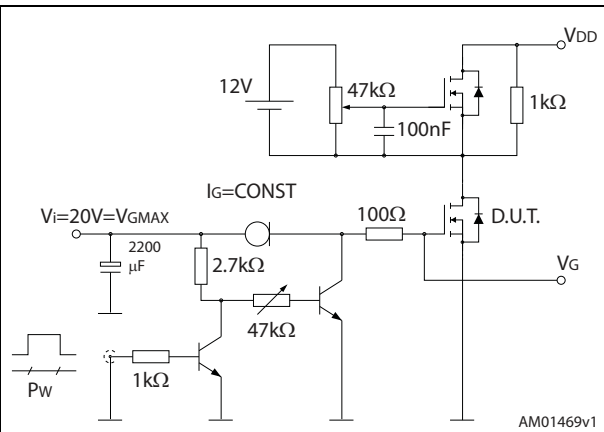
### 3 Test circuits

Figure 15. Switching times test circuit for resistive load



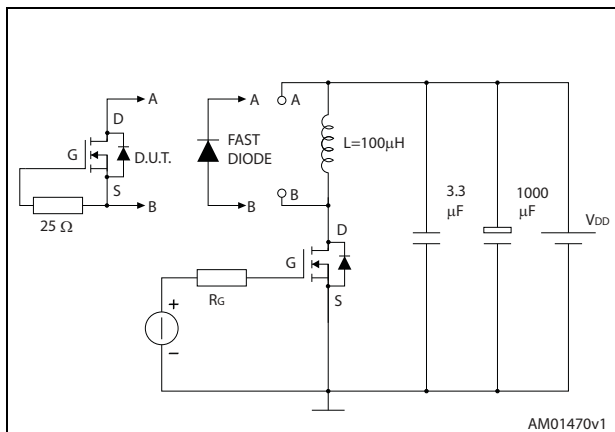
AM01468v1

Figure 16. Gate charge test circuit



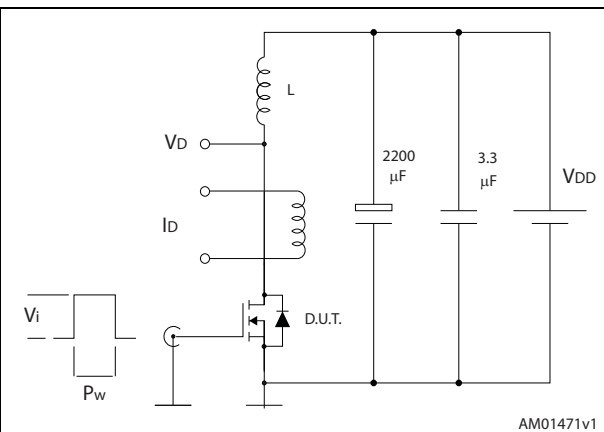
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Figure 17. Switching times test circuit for resistive load



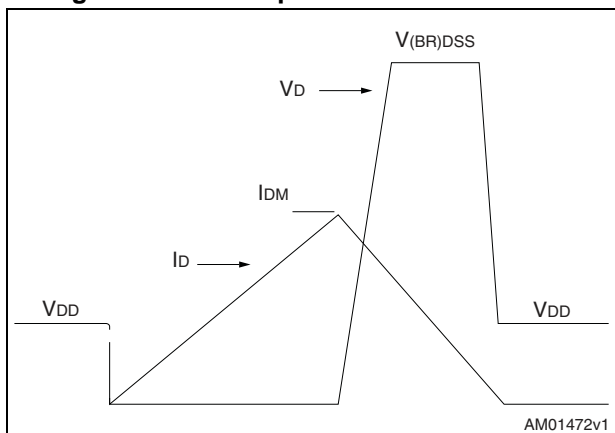
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Figure 18. Gate charge test circuit



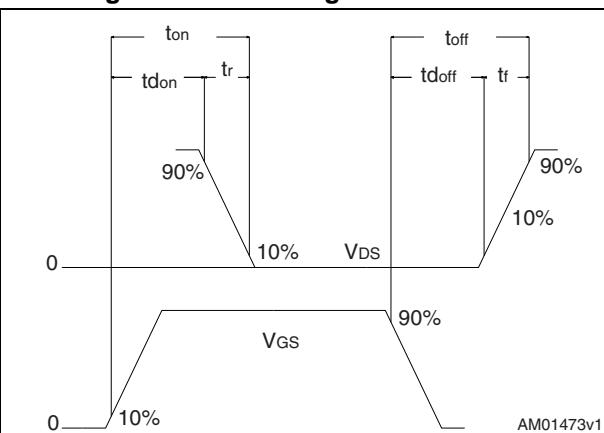
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Figure 19. Unclamped inductive waveform



AM01472v1

Figure 20. Switching time waveform

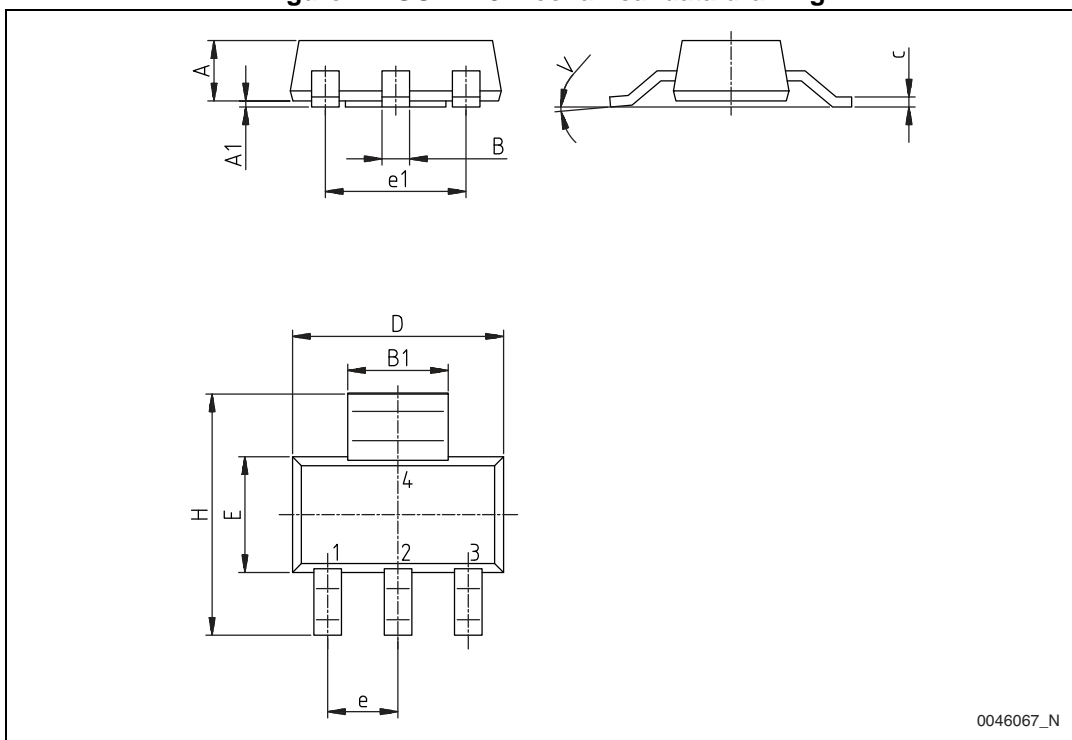


AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Figure 21. SOT-223 mechanical data drawing

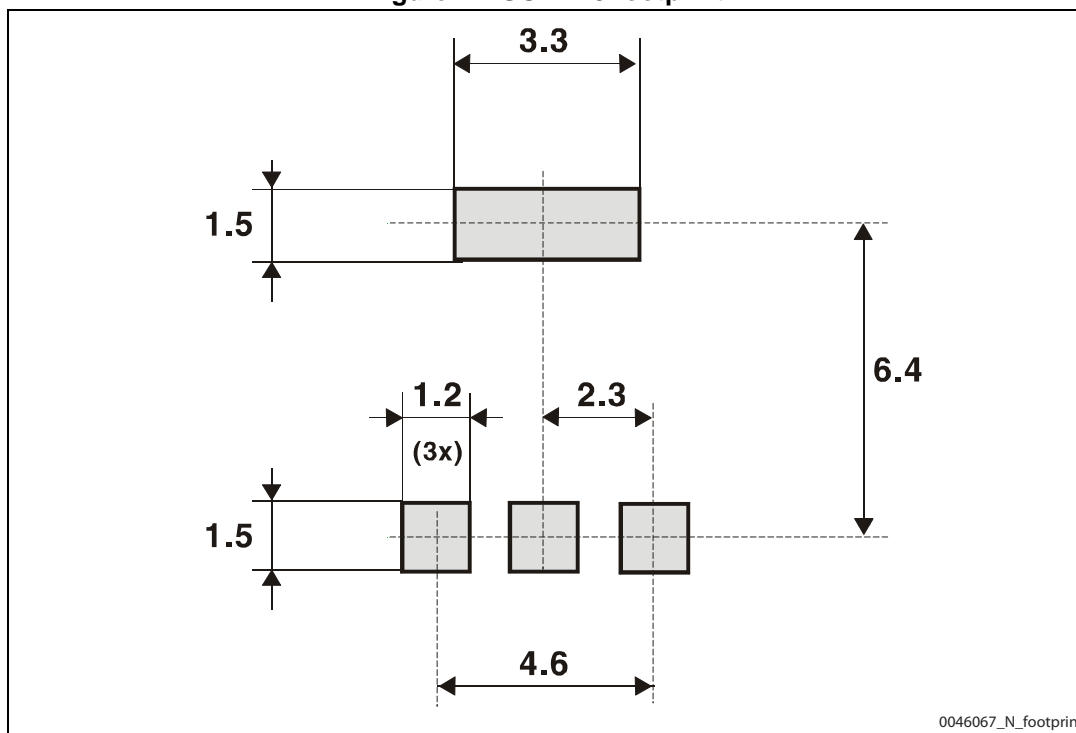


0046067\_N

Table 8. SOT-223 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.80
A1	0.02		0.10
B	0.60	0.70	0.85
B1	2.9	3.0	3.15
c	0.24	0.26	0.35
D	6.30	6.50	6.70
e		2.30	6.70
e1		4.60	
E	3.30	3.50	3.70
H	6.70	7.0	7.30
V			10°

Figure 22. SOT-223 footprint



## 5 Revision history

Table 9. Document revision history

Date	Revision	Changes
29-Jun-2010	1	First release.
08-Apr-2011	2	Document status promoted from preliminary data to datasheet.
06-Jun-2014	3	Updated silhouette, features and <i>Figure 1: Internal schematic diagram</i> in cover page. Updated <i>Table 2: Absolute maximum ratings</i> , <i>Table 3: Thermal data</i> , and <i>Table 4: On /off states</i> . Updated <i>Figure 2: Safe operating area</i> and <i>Figure 6: Gate charge vs gate-source voltage</i> . Updated <i>Section 4: Package mechanical data</i> . Minor text changes.

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