

## **PI74LVC4245A**

## 8-Bit Dual Supply Bus Transceiver with 3-State Outputs

## **Product Features**

- 4.5V to 5.5V on A-port and 2.7V to 3.6V on B-port
- Latch-up performance exceeds 200mA Per JESD78
- ESD protection exceeds JESD 22
  - 2000V Human-Body Model (A114-B)
  - 200V Machine Model (A115-A)
- Industrial Temperature: -40°C to +85°C
- Packaging (Pb-free & Green available):
  - 24-pin 173-mil wide plastic TSSOP (L)
  - 24-pin 150-mil wide plastic QSOP (Q)
  - 24-pin 300-mil wide plastic SOIC (S)

## Logic Block Diagram

## 

## Truth Table<sup>(1)</sup>

Inputs		Outputs
OEDIR		
L	L	Bus B Data to Bus A
L	Н	Bus A Data to Bus B
Н	Х	Z (Isolation)

#### Note:

1. H = High Signal LevelX = Don't Care or Irreleva

X = Don't Care or Irrelevant Z

L = Low Signal Level

Z = High Impedance

### **Product Description** The PI74LVC4245A is a n

The PI74LVC4245A is a non-inverting 8-bit Bidirectional Transceiver that uses two separate power supply rails. A-port ( $V_{CCA}$ ) is set to operate at 5V and B-port ( $V_{CCB}$ ) is set to operate at 3.3V. This allows for translation from a 3.3V to a 5V environment and vice-versa. This tranceiver is designed for asynchronous two-way communication between data buses. The direction control input pin (DIR) determines the dataflow from the A bus to the B bus or from the B bus to the A bus. The output enable ( $\overline{OE}$ ) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

## **Product Pin Configuration**

(5V) V <sub>CCA</sub>		24	VCCB (3.3V)
DIR 🛛	2	23	VCCB (3.3V)
A1 🗖	3	22	
A2 🛛	4	21	<b>D</b> B1
A3 🗖	5	20	<b>D</b> B2
A4 🗖	6	19	🛛 ВЗ
A5 🗖	7	18	<b>D</b> B4
A6 🗖	8	17	<b>D</b> B5
A7 🗖	9	16	🛛 В6
A8 🗖	10	15	🛿 В7
GND	11	14	<b>B</b> 8
GND	12	13	GND
ı			1

## **Product Pin Description**

Pin Name	Description
ŌĒ	3-State Output Enable Inputs (Active LOW)
DIR	Direction Control Input
Ax	Side A Inputs or 3-State Outputs
Bx	Side B Inputs or 3-State Outputs
GND	Ground
V <sub>CCA</sub> ,V <sub>CCB</sub>	Power



## **Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply voltage range, $V_{CCA}$ and $V_{CCB}$ 0.5V to +7V
Input voltage range, $V_{I}^{(1)}$ : I/O ports (A-port)0.5V to V <sub>CCA</sub> +0.5V
I/O ports (B-port)
Control Pins
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> <0)50mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> <0)50mA
Continous Output Current IO±50mA
Continous Current through each VCC or GND pin
Package thermal impedance, $\theta_{JA}^{(2)}$ : package L
package Q 98°C/W
package S 79°C/W
Storage Temperature range, $T_{stg}$ 65°C to 150°C

### Notes:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1. This value is limited to 7V maximum.

2. The package thermal impedance is calculated in accordance with JESD 51.

## **Recommended Operating Conditions for** $V_{CCA}$ = 4.5V to 5.5V<sup>(1)</sup>

Parameter	Description	Min.	Max.	Units
V <sub>CCA</sub>	Supply Voltage	4.5	5.5	
V <sub>IH</sub>	High-Level Input Voltage	2		
V <sub>IL</sub>	Low-Level Input Voltage		0.8	V
VI	Input Voltage	0	V <sub>CCA</sub>	
Vo	Output Voltage	0	V <sub>CCA</sub>	
I <sub>OH</sub>	High-Level Output Current		-24	A
I <sub>OL</sub>	I <sub>OL</sub> Low-Level Output Current		24	mA
TA	Operating Free-Air Temperature	-40	85	°C

Notes:

1. All unused inputs of the device must be held at the associated V<sub>CC</sub> or GND to ensure proper device operation.

## **Recommended Operating Conditions for** $V_{CCB} = 2.7V$ to $3.6V^{(1)}$

Parameter	Description			Max.	Units
V <sub>CCB</sub>	Supply Voltage		2.7	3.6	
V <sub>IH</sub>	High-Level Input Voltage	$V_{CCB} = 2.7V$ to 3.6V	2		
V <sub>IL</sub>	Low-Level Input Voltage $V_{CCB} = 2.7V$ to $3.6V$			0.8	V
VI	Input Voltage		0	V <sub>CCB</sub>	
Vo	Output Voltage		0	V <sub>CCB</sub>	
I.e.e.	High I aval Output Current	$V_{CCB} = 2.7V$		-12	
I <sub>OH</sub>	High-Level Output Current	$V_{\rm CCB} = 3V$		-24	110 Å
т	$V_{\rm CCB} = 2.7 V$	$V_{\rm CCB} = 2.7 V$		12	mA
I <sub>OL</sub>	Low-Level Output Current	$V_{CCB} = 3V$		24	
TA	Operating Free-Air Temperature		-40	85	°C

#### Notes:

1. All unused inputs of the device must be held at the associated V<sub>CC</sub> or GND to ensure proper device operation.



DC Electrical Characteristics (Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified)
A-Port (5V)

Param- eters	Description	Test Conditions	VCCA	V <sub>CCB</sub>	Min.	Typ. <sup>(1)</sup>	Max.	Units
		I — 100A	4.5V	2.7V to 3.6V	4.4	4.5		
N/	Minimum High Level	$I_{OH} = -100 \mu A$	5.5V	2.7V to 3.6V	5.4	5.5		
V <sub>OH</sub> Output Voltage	I	4.5V	2.7V to 3.6V	3.7	4.17			
		$I_{OH} = -24mA$	5.5V	2.7V to 3.6V	4.7	5.2		v
		I = 100 A	4.5V	2.7V to 3.6V			0.1	
V	Maximum Low Level	$I_{OL} = 100 \mu A$	5.5V	2.7V to 3.6V			0.1	
VOL	V <sub>OL</sub> Output Voltage	$I_{} = 24m \Lambda$	4.5V	2.7V to 3.6V		0.19	0.5	
	$I_{OL} = 24 mA$	5.5V	2.7V to 3.6V		0.19	0.5		
II	Maximum Input Leak- age Current (Control Inputs)	$V_I = V_{CCA}$ or GND	5.5V	2.7V to 3.6V			±1	
I <sub>OZ</sub> <sup>(2)</sup>	Maximum 3-State Output Leakage Current (A port)	$V_{\rm O} = V_{\rm CCA}$ or GND	5.5V	2.7V to 3.6V			±5	μA
I <sub>CCA</sub>	Quiescent V <sub>CCA</sub> Supply Current	$V_{I} = V_{CCA}$ or GND, $I_{O} = 0$	5.5V	2.7V to 3.6V			10	
$\Delta I_{CCA}^{(3)}$	I <sub>CCA</sub> per input (A port and Control Inputs)	One Input at 3.4V, other inputs at $V_{CCA}$ or GND	5.5V	2.7V to 3.6V		0.65	1.5	mA
CI	Input Capacitance (Con- trol Inputs)	$V_{I} = V_{CCA}$ or GND	Open	2.7V to 3.6V		2.4		nE
C <sub>IO</sub>	Input/Output Capaci- tance (A port)	$V_{O} = V_{CCA}$ or GND	5V	2.7V to 3.6V		9.5		pF

Notes:

5. All typical values are measured at  $V_{CCA} = 5V$ ,  $T_A = 25^{\circ}C$ 

6. For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

7. This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0V or the associated  $V_{CC}$ .

DC Electrical Characteristics (Over Supply Vo	ge and Operating Temperature Ranges, unless otherwise specified	1)
B-Port (3.3V)		

Parameters	Description	Test Conditions	V <sub>CCA</sub>	V <sub>CCB</sub>	Min.	Typ. <sup>(1)</sup>	Max.	Units
	Minimum High	$I_{OH} = -100 \mu A$	4.5V to 5.5V	2.7V to 3.6V	V <sub>CC</sub> -0.1			
V <sub>OH</sub>	Level Output Volt-	I _ 12mA	4.5V to 5.5V	2.7V	2.2	2.56		
	age	$I_{OH} = -12mA$	4.5V to 5.5V	3V	2.4	2.85		
		$I_{OH} = -24mA$	4.5V to 5.5V	3V	2	2.70		V
	Maximum Low	$I_{OL} = 100 \mu A$	4.5V to 5.5V	2.7V to 3.6V			0.1	
V <sub>OL</sub>		$I_{OL} = 12mA$	4.5V to 5.5V	2.7V		0.09	0.4	
		$I_{OL} = 24 \text{mA}$	4.5V to 5.5V	3V		0.18	0.5	
I <sub>OZ</sub> <sup>(2)</sup>	Maximum 3-State Output Leakage Current (B port)	$V_{O} = V_{CCB}$ or GND	4.5V to 5.5V	3.6V			±5	
I <sub>CCB</sub>	Quiescent V <sub>CCB</sub> Supply Current	$V_{I} = V_{CCB}$ or GND, $I_{O} = 0$	4.5V to 5.5V	3.6V			10	μΑ
$\Delta I_{CCB}^{(3)}$	I <sub>CCB</sub> per input	One Input at $V_{CCB}$ -0.6V, other inputs at $V_{CCB}$ or GND	4.5V to 5.5V	2.7V to 3.6V			50	
C <sub>IO</sub>	Input/Output Ca- pacitance (B port)	$V_{\rm O} = V_{\rm CCB}$ or GND	4.5V to 5.5V	3.3V		9.7		pF

Notes:

1. All typical values are measured at  $V_{CCB} = 3.3V$ ,  $T_A = 25^{\circ}C$ 

2. For I/O ports, the parameter  $I_{\mbox{\scriptsize OZ}}$  includes the input leakage current.

3. This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0V or the associated  $V_{CC}$ .

## **Capacitance** ( $V_{CCA} = 4.5V$ to 5.5V, $V_{CCB} = 2.7V$ to 3.6V, $T_A = 25^{\circ}C$ )

Parameters	Description	Test C	Тур.	Units	
C	Power Dissipation Capaci-	Outputs Enabled	$C_{-} = 0$ mE f = 10 MHz	20	ъE
C <sub>PD</sub>	tance <sup>(1)</sup>	Outputs Disabled	$C_L = 0 pF, f = 10 MHz$	2.3	pF

Notes:

1.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle,  $C_{PD}$  is related to I<sub>CCD</sub> dynamic operating current by the expression: I<sub>CCD</sub> = ( $C_{PD}$ )( $V_{CC}$ )( $f_{IN}$ ) +(I<sub>CC</sub> static)



## **AC Electrical Characteristics**

(Over Recommended Operating Free-Air Temperature Range unless otherwise noted, See Figure 1 and 2)

		To (Output)	$V_{CCA} = 5V \pm 0.5V, V_{CCA} = 5V \pm 0.5V, V_{CCA}$	Units	
Parameters	From (Input)		$C_L = 50 pF$ ,		
	(input)	(Output)	Min.	Max.	
t <sub>PHL</sub>	A	В	1	5.7	
t <sub>PLH</sub>	А	D	1	5.5	
t <sub>PHL</sub>	В	٨	1	6.1	
t <sub>PLH</sub>		А	1	5.9	
t <sub>PZL</sub>	ŌĒ		1	8	
t <sub>PZH</sub>	UE	А	1	7.6	
t <sub>PZL</sub>	- <del>OE</del>	D	1	8	ns
t <sub>PZH</sub>	OE	В	1	7.7	1
t <sub>PLZ</sub>			1	6.2	1
t <sub>PHZ</sub>	ŌĒ	А	1	5.8	
t <sub>PLZ</sub>		D	1	7	]
t <sub>PHZ</sub>	OE	В	1	6.8	]
t <sub>SK(O)</sub>	Output-to-Output Skew <sup>(1)</sup>			1.5	]

Notes:

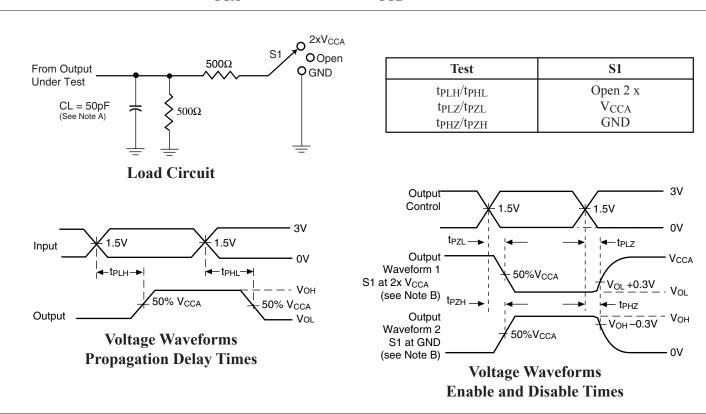
1. Skew between any two outputs of the same device, switching in the same direction. Parameter guaranteed by design.

## **Power- Up Considerations**

To avoid excessive supply current, bus contention or oscillation during power-up, the following guidelines should be followed:

- 1. Connect ground first before any supply voltage is applied.
- 2. Then Power up  $V_{CCA}$ , which is the control side of the device.
- 3. Ramp  $\overline{\text{OE}}$  ahead of or with  $V_{\text{CCA}}$  to help prevent bus contention
- 4. Ramp DIR with V<sub>CCA</sub> if DIR HIGH is needed (A bus to B bus). Otherwise keep DIR LOW.





# PARAMETER MEASUREMENT INFORMATION FOR B TO A PORT $V_{CCA} = 5V \pm 0.5V$ and $V_{CCB} = 2.7V$ to 3.6V

Figure 1. Load Circuit and Voltage Waveforms

## Notes:

- A. C<sub>L</sub> includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50 $\Omega$ , t<sub>R</sub>  $\leq$  2.5ns, t<sub>F</sub>  $\leq$  2.5ns.
- The outputs are measured one at a time with one transition per measurement.



#### 7V **O**Open Test **S1** 500Ω From Output **Q**GND Under Test t<sub>PLH</sub>/t<sub>PHL</sub> Open 7V tpLZ/tpZL CL = 50 pF500Ω GND t<sub>PHZ</sub>/t<sub>PZH</sub> (See Note A) **Load Circuit** ЗV Output Control 1.5V 1.5V 0V ЗV t<sub>PZL</sub> --t<sub>PLZ</sub> . 1.5V 1.5V Input Output 3.5V οv Waveform 1 <-t<sub>PLH</sub>-► . I ← t<sub>PHL</sub> → S1 at 7V Vol +0.3\ (see Note B) t<sub>PZH -</sub> Voi Vон – t<sub>PHZ</sub> Output 1.5V .5V Output V<sub>OH</sub>-0.3V VOH Vol Waveform 2 1.5V S1 at GND Voltage Waveforms ٥V (see Note B) **Propagation Delay Times Voltage Waveforms Enable and Disable Times**

# PARAMETER MEASUREMENT INFORMATION FOR A TO B PORT $V_{CCA}$ = 4.5V to 5.5V and $V_{CCB}$ = 2.7V to 3.6V

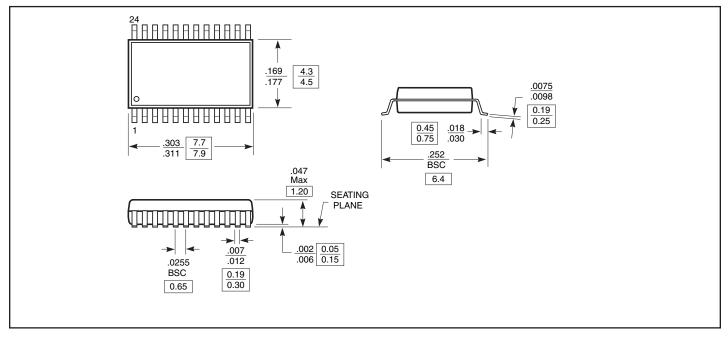
Figure 2. Load Circuit and Voltage Waveforms

## Notes:

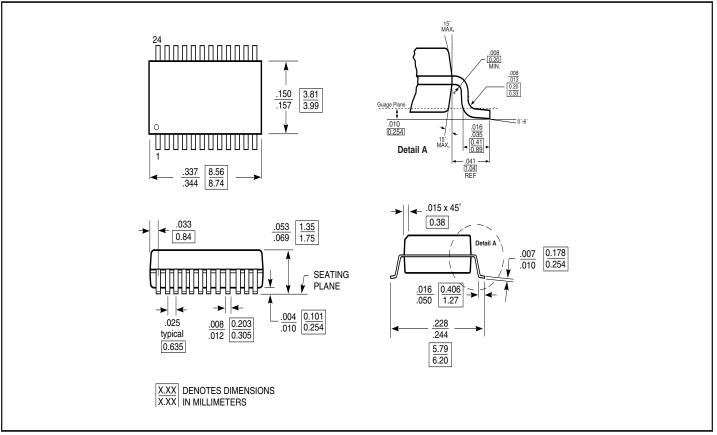
- A. C<sub>L</sub> includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics:  $PRR \le 10$  MHz,  $Z_0 = 50\Omega$ ,  $t_R \le 2.5$ ns,  $t_F \le 2.5$ ns.
- The outputs are measured one at a time with one transition per measurement.



Packaging Mechanical: 24-pin TSSOP (L)

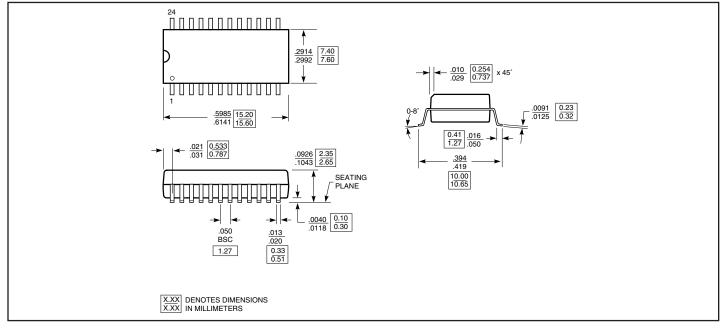


## Packaging Mechanical: 24-pin QSOP (Q)





## Packaging Mechanical: 24-pin SOIC (S)



## **Ordering Information**

Ordering Code	Package Code	Package Type
PI74LVC4245AL	L	24-pin, 173-mil wide plastic TSSOP
PI74LVC4245ALE	L	Pb-free, 24-pin, 173-mil wide plastic TSSOP
PI74LVC4245AQ	Q	24-pin, 150-mil wide plastic QSOP
PI74LVC4245AS	S	24-pin, 300-mil wide plastic SOIC
PI74LVC4245ASE	S	Pb-free & Green, 24-pin, 300-mil wide plastic SOIC

Notes:

• Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

• E = Pb-free & Green

• Adding an X suffix = Tape/Reel