High-Speed CMOS Bus Exchange Switches with Extended Voltage Range

QS3386

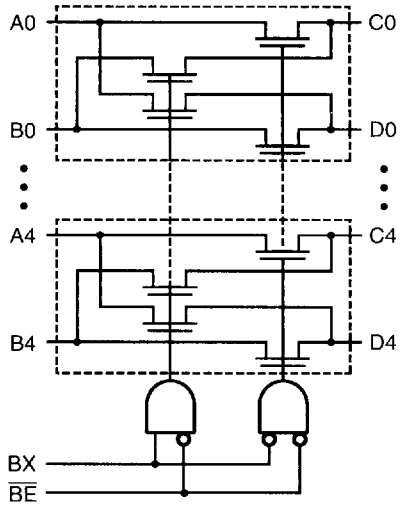
FEATURES/BENEFITS

- 7Ω switches connect inputs to outputs
- Uses Vcc of +5V and GND of –2V
- Zero propagation delay
- Low power CMOS proprietary technology
- Provides routing of ECL signals
- Bus exchange allows nibble swap
- Zero ground bounce
- Available in 24-pin DIP, SOIC, and QSOP

DESCRIPTION

The QS3386 each provide two sets of ten high-speed CMOS bus switches with a signal range of +5 to –2V, allowing routing of ECL signals. These devices can also be used to route video and RF signals with voltage ranges of ±2V (4V peak to peak). The low ON resistance (7Ω) of the 3386 allows inputs to be connected to outputs without adding propagation delay and without generating additional noise. Control inputs operate at TTL levels. The Bus Enable ($\overline{BE}$) signal turns the switches on. The Bus Exchange (BX) signal provides nibble swap of the AB and CD pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a five 2-to-1 multiplexer and to create low delay barrel shifters, etc.

FUNCTIONAL BLOCK DIAGRAM



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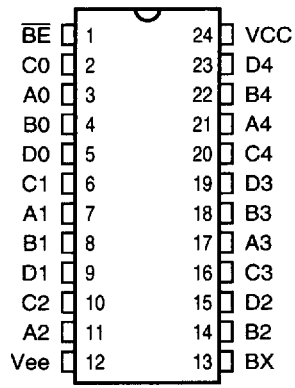
PIN DESCRIPTION

Name	I/O	Function
A4-A0, B4-B0	I/O	Buses A, B
C4-C0, D4-D0	I/O	Buses C, D
$\overline{BE}$	I	Bus Switch Enable
BX	I	Bus Exchange

PIN CONFIGURATION (All Pins Top View)

PDIP, SOIC, QSOP



FUNCTION TABLE

$\overline{BE}$	BX	A4-A0	B4-B0	Function
H	X	Hi-Z	Hi-Z	Disconnect
L	L	C4-C0	D4-D0	Connect
L	H	D4-D0	C4-C0	Exchange

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to +7.5V
DC Switch Voltage Vs	Vee –0.5V to Vee
DC Input Voltage V_{IN}	Vee –0.5V to Vee +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	–3.0V
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	SOIC Typ	SOIC Max	QSOP Typ	QSOP Max	PDIP Typ	PDIP Max	Unit
Control Pins	3	4	3	4	4	5	pF
QuickSwitch Channels	7	8	7	8	8	9	pF

Note: Capacitance is characterized but not tested.

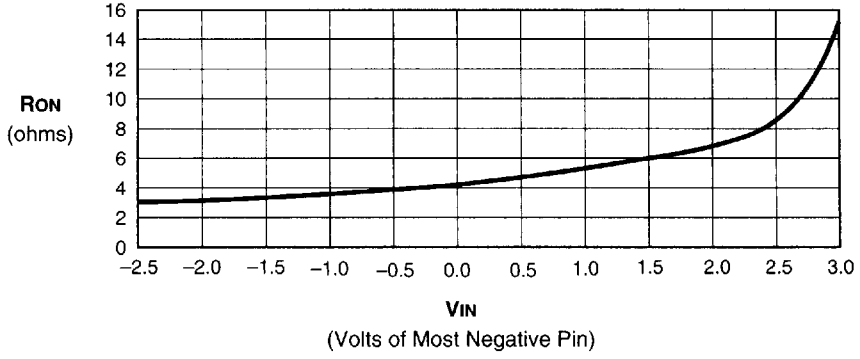
DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial: T_A = 0°C to 70°C, Vcc = Vee +(7.5 ± 5%)

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs, Vee = –2V	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs, Vee = –2V	—	—	0.8	V
$\lvert I_{IN} \rvert$	Input Leakage Current(2)	Vee ≤ V_{IN} ≤ Vcc	—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Current (Hi-Z)	Vee ≤ AB, CD ≤ Vcc	—	—	5	µA
R_{ON}	Switch ON Resistance(4,5)	Vcc = Min., V_{IN} = 0.0V I_{ON} = 30 mA	—	8	10	Ω
R_{ON}	Switch ON Resistance(4,5)	Vcc = Min., V_{IN} = 2.4V I_{ON} = 15 mA	—	12	17	Ω

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. During input/output leakage, testing all pins are at a HIGH or LOW state, and the $\overline{BE}$ control is HIGH.
3. Not more than one output should be used to test this high power condition and the duration is ≤1 second.
4. Measured by voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A or B, C or D) pins.
5. Max. value R_{ON} guaranteed but not tested.

Typical ON Resistance vs V_{IN} at 4.75 Vcc



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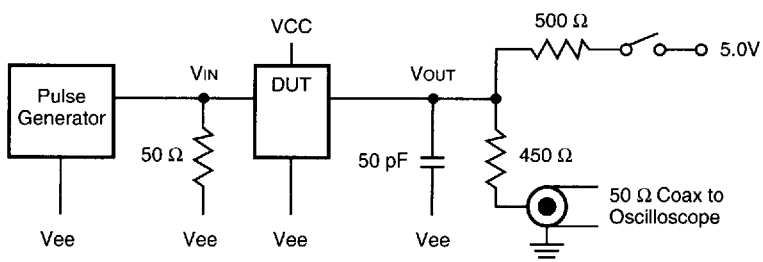
POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	Vcc = Max., V_{IN} = GND or Vcc, f = 0	3.0	mA
ΔI_{CC}	Power Supply Current per Input HIGH[2]	Vcc = Max., V_{IN} = 3.4V, f = 0 per Control Input	5.0	mA
Q_{CCD}	Dynamic Power Supply Current per MHz[3]	Vcc = Max., ABCD Pins Open, Control Inputs Toggling @ 50% Duty Cycle	0.5	mA/ MHz
Ic	Total Power Supply Current[4,5]	Vcc = Max., ABCD Pins at 0.0V, Control Inputs Toggling @ 50% Duty Cycle Vih = 3.4V, f Clock + MHz	18	mA

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V, control inputs only). A, B, C, D pins do not contribute to Icc.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A, B, C, D inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed by design, but not tested.
4. Ic = I Quiescent + I Inputs + I Dynamic.
   Ic = Icc + $\Delta I_{CC} D_H N_T$ + Qccd (fiNi).
   Icc = Power Supply Current for each TTL HIGH input (V_{IN} = 3.4V, control inputs only).
   D_H = Duty Cycle for each TTL input that is HIGH (control inputs only).
   N_T = Number of TTL inputs that are at D_H (control inputs only).
   fi = frequency that the inputs are toggled (control inputs only).
5. Note that activity on A, B, C, D inputs do not contribute to Ic if A, B, C, D inputs are between Vee and Vcc. The switches merely connect and pass through activity on these pins. For example: If the control inputs are at 0V and the switches are on, Ic will be equal to Icc only regardless of activity on the A, B, C, D pins.

Parameter Tested	Switch Position
t_{PLZ}, t_{PLZ}	Closed
All Others	Open



SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial: T_A = 0°C to 70°C, V_{CC} = Vee +(7.5 ± 5%)
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]	QS3386 Min	QS3386 Typ	QS3386 Max	Unit
t_{PLH} t_{PHL}	Data Propagation Delay[2,3] AiBi to CiDi, CiDi to AiBi	—	0.25	—	ns
t_{PZL} t_{PZH}	Switch Turn-on Delay[1] $\overline{BE}$ to Ai, Bi, Ci, Di	1.5	—	6.5	ns
t_{PLZ} t_{PHZ}	Switch Turn-off Delay[1,2] $\overline{BE}$ to Ai, Bi, Ci, Di	1.5	—	5.5	ns
t_{BX}	Switch Multiplex Delay[1] BX to Ai, Bi, Ci, Di[1]	1.5	—	6.5	ns
$\lvert Q_{CI} \rvert$	Charge Injection, Typical[2,4]	—	—	2.0	pC
$\lvert Q_{DCI} \rvert$	Differential Charge Injection, Typical[2,5]	—	<0.5	—	pC

Notes:

1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe, V_{IN} at A = 0.0V.
5. Measured at switch turn off through bus multiplex, A to C ≥ A to D, B connected to C, load = 50 pF in parallel with 10 meg scope probe, V_{IN} at A = 0.0V. Charge injection is reduced because the injection from the turn off of the A to C switch is compensated by the turn on of the B to C switch.

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