# LMC6442 Dual Micropower Rail-to-Rail Output Single Supply Operational Amplifier

**Check for Samples: LMC6442**

## FEATURES

- **(Typical, $V_S$ = 2.2V)**
- **Output Swing to Within 30 mV of Supply Rail**
- **High Voltage Gain 103 dB**
- **Gain Bandwidth Product 9.5 KHz**
- **Ensured for: 2.2V, 5V, 10V**
- **Low Supply Current 0.95 µA/Amplifier**
- **Input Voltage Range −0.3V to $V^+$ -0.9V**
- **2.1 µW/Amplifier Power Consumption**
- **Stable for $A_V \geq +2$ or $A_V \leq -1$**

## APPLICATIONS

- **Portable Instruments**
- **Smoke/Gas/CO/Fire Detectors**
- **Pagers/Cell Phones**
- **Instrumentation**
- **Thermostats**
- **Occupancy Sensors**
- **Cameras**
- **Active Badges**

## DESCRIPTION

The LMC6442 is ideal for battery powered systems, where very low supply current (less than one microamp per amplifier) and Rail-to-Rail output swing is required. It is characterized for 2.2V to 10V operation, and at 2.2V supply, the LMC6442 is ideal for single (Li-Ion) or two cell (NiCad or alkaline) battery systems.

The LMC6442 is designed for battery powered systems that require long service life through low supply current, such as smoke and gas detectors, and pager or personal communications systems.

Operation from single supply is enhanced by the wide common mode input voltage range which includes the ground (or negative supply) for ground sensing applications. Very low (5 fA, typical) input bias current and near constant supply current over supply voltage enhance the LMC6442's performance near the end-of-life battery voltage.

Designed for closed loop gains of greater than plus two (or minus one), the amplifier has typically 9.5 KHz GBWP (Gain Bandwidth Product). Unity gain can be used with a simple compensation circuit, which also allows capacitive loads of up to 300 pF to be driven, as described in the Application Information section.

### Connection Diagram

**Top View**

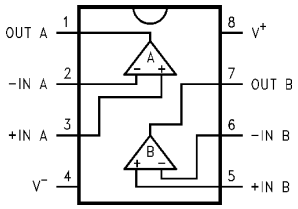



**Figure 1. 8-Pin SOIC / PDIP Package**
**See Package Numbers D0008A, P0008E**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings (1)(2)

| | |
|---|---|
| ESD Tolerance (3) | 2 kV |
| Differential Input Voltage | ±Supply Voltages |
| Voltage at Input/Output Pin | $(V^+)$ + 0.3V, $(V^-)$ − 0.3V |
| Supply Voltage $(V^+ - V^-)$: | 16V |
| Current at Input Pin (4) | ±5 mA |
| Current at Output Pin (5) (6) | ±30 mA |
| Lead Temp. (soldering 10 sec) | 260°C |
| Storage Temp. Range: | −65°C to +150°C |
| Junction Temp. (7) | 150°C |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5 kΩ in series with 100 pF.
(4) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(6) Do not short circuit output to $V^+$, when $V^+$ is greater than 13V or reliability will be adversely affected.
(7) The maximum power dissipation is a function of $T_{J(MAX)}$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

## Operating Ratings (1)

| | | |
|---|---|---|
| Supply Voltage | | $1.8V \le V_S \le 11V$ |
| Junction Temperature Range: LMC6442AI, LMC6442I | | $-40°C < T_J < +85°C$ |
| Thermal Resistance ($\theta_{JA}$) | D0008A Package, 8-pin Surface Mount | 193°C/W |
| | P0008E Package, 8-pin Molded DIP | 115°C/W |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

## 2.2V Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J$ = 25°C, $V^+$ = 2.2V, $V^-$ = 0V, $V_{CM} = V_O = V^+/2$, and $R_L$ = 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

| Parameter | | Test Conditions | Typ (1) | LMC6442AI Limit (2) | LMC6442I Limit (2) | Units |
|---|---|---|---|---|---|---|
| **DC Electrical Characteristics** | | | | | | |
| $V_{OS}$ | Input Offset Voltage | | −0.75 | ±3<br>**±4** | ±7<br>**±8** | mV<br>max |
| $TCV_{OS}$ | Temp. coefficient of input offset voltage | | 0.4 | | | µV/°C |
| $I_B$ | Input Bias Current | See (3) | 0.005 | **4** | **4** | pA<br>max |
| $I_{OS}$ | Input Offset Current | See (3) | 0.0025 | **2** | **2** | pA<br>max |
| CMRR | Common Mode Rejection Ratio | $-0.1V \le V_{CM} \le 0.5V$ | 92 | 67<br>**67** | 67<br>**67** | dB min |
| $C_{IN}$ | Common Mode Input Capacitance | | 4.7 | | | pF |
| PSRR | Power Supply Rejection Ratio | $V_S$ = 2.5 V to 10V | 95 | 75<br>**75** | 75<br>**75** | dB<br>min |

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis unless otherwise specified.
(3) Limits specified by design.

## 2.2V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_J$ = 25°C, $V^+$ = 2.2V, $V^-$ = 0V, $V_{CM}$ = $V_O$ = $V^+$/2, and $R_L$ = 1 MΩ to $V^+$/2. **Boldface** limits apply at the temperature extremes.

| Parameter | | Test Conditions | Typ (1) | LMC6442AI Limit (2) | LMC6442I Limit (2) | Units |
|---|---|---|---|---|---|---|
| $V_{CM}$ | Input Common-Mode Voltage Range | CMRR ≥ 50 dB | 1.3 | 1.05<br>**0.95** | 1.05<br>**0.95** | V min |
| | | | −0.3 | −0.2<br>**0** | −0.2<br>**0** | V max |
| $A_V$ | Large Signal Voltage Gain | Sourcing (4) | 100 | | | dB min |
| | | Sinking (4) | 94 | | | |
| | | $V_O$ = 0.22V to 2V | 103 | 80 | 80 | |
| $V_O$ | Output Swing | $V_{ID}$ = 100 mV (5) | 2.18 | 2.15<br>**2.15** | 2.15<br>**2.15** | V min |
| | | $V_{ID}$ = −100 mV (5) | 22 | 60<br>**60** | 60<br>**60** | mV max |
| $I_{SC}$ | Output Short Circuit Current | Sourcing, $V_{ID}$ = 100 mV (6) (5) | 50 | 18<br>**17** | 18<br>**17** | µA min |
| | | Sinking, $V_{ID}$ = −100 mV (6) (5) | 50 | 20<br>**19** | 20<br>**19** | |
| $I_S$ | Supply Current (2 amplifiers) | $R_L$ = open | 1.90 | 2.4<br>**3.0** | 2.6<br>**3.2** | µA max |
| | | $V^+$ = 1.8V, $R_L$ = open | 2.10 | | | |
| **AC Electrical Characteristics** | | | | | | |
| SR | Slew Rate (7) | | 2.2 | | | V/ms |
| GBWP | Gain-Bandwidth Product | | 9.5 | | | KHz |
| $\varphi_m$ | Phase Margin | See (8) | 63 | | | deg |

(4) $R_L$ connected to $V^+$/2. For Sourcing Test, $V_O$ > $V^+$/2. For Sinking tests, $V_O$ < $V^+$/2.
(5) $V_{ID}$ is differential input voltage referenced to inverting input.
(6) Output shorted to ground for sourcing, and shorted to V+ for sinking short circuit current test.
(7) Slew rate is the slower of the rising and falling slew rates.
(8) See the Typical Performance Characteristics and Applications Information sections for more details.

## 5V Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J$ = 25°C, $V^+$ = 5V, $V^-$ = 0V, $V_{CM}$ = $V_O$ = $V^+$/2, and $R_L$ = 1 MΩ to $V^+$/2. **Boldface** limits apply at the temperature extremes.

| Parameter | | Test Conditions | Typ (1) | LMC6442AI Limit (2) | LMC6442I Limit (2) | Units |
|---|---|---|---|---|---|---|
| **DC Electrical Characteristics** | | | | | | |
| $V_{OS}$ | Input Offset Voltage | | −0.75 | ±3<br>**±4** | ±7<br>**±8** | mV max |
| $TCV_{OS}$ | Temp. coefficient of input offset voltage | | 0.4 | | | µV/°C |
| $I_B$ | Input Bias Current | See (3) | 0.005 | **4** | **4** | pA max |
| $I_{OS}$ | Input Offset Current | See (3) | 0.0025 | **2** | **2** | pA max |
| CMRR | Common Mode Rejection Ratio | −0.1V ≤ $V_{CM}$ ≤3.5V | 102 | 70<br>**70** | 70<br>**70** | dB min |
| $C_{IN}$ | Common Mode Input Capacitance | | 4.1 | | | pF |
| PSRR | Power Supply Rejection Ratio | $V_S$ = 2.5 V to 10V | 95 | 75<br>**75** | 75<br>**75** | dB min |

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis unless otherwise specified.
(3) Limits specified by design.

## 5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_J$ = 25°C, $V^+$ = 5V, $V^-$ = 0V, $V_{CM} = V_O = V^+/2$, and $R_L$ = 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

| Parameter | | Test Conditions | Typ (1) | LMC6442AI Limit (2) | LMC6442I Limit (2) | Units |
|---|---|---|---|---|---|---|
| $V_{CM}$ | Input Common-Mode Voltage Range | CMRR ≥ 50 dB | 4.1 | 3.85<br>**3.75** | 3.85<br>**3.75** | V min |
| | | | −0.4 | −0.2<br>**0** | −0.2<br>**0** | V max |
| $A_V$ | Large Signal Voltage Gain | Sourcing (4) | 100 | | | dB min |
| | | Sinking (4) | 94 | | | |
| | | $V_O$ = 0.5V to 4.5V | 103 | 80 | 80 | |
| $V_O$ | Output Swing | $V_{ID}$ = 100 mV (5) | 4.99 | 4.95<br>**4.95** | 4.95<br>**4.95** | V min |
| | | $V_{ID}$ = −100 mV (5) | 20 | 50<br>**50** | 50<br>**50** | mV max |
| $I_{SC}$ | Output Short Circuit Current | Sourcing, $V_{ID}$ = 100 mV (6) (5) | 500 | 300<br>**200** | 300<br>**200** | µA min |
| | | Sinking, $V_{ID}$ = −100 mV (6) (5) | 350 | 200<br>**150** | 200<br>**150** | |
| $I_S$ | Supply Current (2 amplifiers) | $R_L$ = open | 1.90 | 2.4<br>**3.0** | 2.6<br>**3.2** | µA max |
| **AC Electrical Characteristics** | | | | | | |
| SR | Slew Rate (7) | | 4.1 | 2.5 | 2.5 | V/ms |
| GBWP | Gain-Bandwidth Product | | 10 | | | KHz |
| $\varphi_m$ | Phase Margin | See (8) | 64 | | | deg |
| THD | Total Harmonic Distortion | $A_V$ = +2, f = 100 Hz,<br>$R_L$ = 10 MΩ, $V_{OUT}$ = 1 $V_{PP}$ | 0.08 | | | % |

(4) $R_L$ connected to $V^+/2$. For Sourcing Test, $V_O > V^+/2$. For Sinking tests, $V_O < V^+/2$.
(5) $V_{ID}$ is differential input voltage referenced to inverting input.
(6) Output shorted to ground for sourcing, and shorted to V+ for sinking short circuit current test.
(7) Slew rate is the slower of the rising and falling slew rates.
(8) See the Typical Performance Characteristics and Applications Information sections for more details.

## 10V Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_J$ = 25°C, $V^+$ = 10V, $V^-$ = 0V, $V_{CM} = V_O = V^+/2$, and $R_L$ = 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

| Parameter | | Test Conditions | Typ (1) | LMC6442AI Limit (2) | LMC6442I Limit (2) | Units |
|---|---|---|---|---|---|---|
| **DC Electrical Characteristics** | | | | | | |
| $V_{OS}$ | Input Offset Voltage | | −1.5 | ±3<br>**±4** | ±7<br>**±8** | mV max |
| $TCV_{OS}$ | Temp. coefficient of input offset voltage | | 0.4 | | | µV/°C |
| $I_B$ | Input Bias Current | See (3) | 0.005 | **4** | **4** | pA max |
| $I_{OS}$ | Input Offset Current | See (3) | 0.0025 | **2** | **2** | pA max |
| CMRR | Common Mode Rejection Ratio | −0.1V ≤ $V_{CM}$ ≤8.5V | 105 | 70<br>**70** | 70<br>**70** | dB min |
| $C_{IN}$ | Common Mode Input Capacitance | | 3.5 | | | pF |
| PSRR | Power Supply Rejection Ratio | $V_S$= 2.5 V to 10V | 95 | 75<br>**75** | 75<br>**75** | dB min |

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis unless otherwise specified.
(3) Limits specified by design.

## 10V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_J$ = 25°C, $V^+$ = 10V, $V^-$ = 0V, $V_{CM} = V_O = V^+/2$, and $R_L$ = 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

| Parameter | | Test Conditions | Typ (1) | LMC6442AI Limit (2) | LMC6442I Limit (2) | Units |
|---|---|---|---|---|---|---|
| $V_{CM}$ | Input Common-Mode Voltage Range | CMRR ≥ 50 dB | 9.1 | 8.85<br>**8.75** | 8.85<br>**8.75** | V<br>min |
| | | | −0.4 | −0.2<br>**0** | −0.2<br>**0** | V<br>max |
| $A_V$ | Large Signal Voltage Gain | Sourcing (4) | 120 | | | dB<br>min |
| | | Sinking (4) | 100 | | | |
| | | $V_O$ = 0.5V to 9.5V | 104 | 80 | 80 | |
| $V_O$ | Output Swing | $V_{ID}$ = 100 mV (5) | 9.99 | 9.97<br>**9.97** | 9.97<br>**9.97** | V<br>min |
| | | $V_{ID}$ = −100 mV (5) | 22 | 50<br>**50** | 50<br>**50** | mV<br>max |
| $I_{SC}$ | Output Short Circuit Current | Sourcing, $V_{ID}$ = 100 mV (6) (5) | 2100 | 1200<br>**1000** | 1200<br>**1000** | µA<br>min |
| | | Sinking, $V_{ID}$ = −100 mV (6) (5) | 900 | 600<br>**500** | 600<br>**500** | |
| $I_S$ | Supply Current (2 amplifiers) | $R_L$ = open | 1.90 | 2.4<br>**3.0** | 2.6<br>**3.2** | µA<br>max |
| **AC Electrical Characteristics** | | | | | | |
| SR | Slew Rate (7) | | 4.1 | 2.5 | 2.5 | V/ms |
| GBWP | Gain-Bandwidth Product | | 10.5 | | | KHz |
| $\varphi_m$ | Phase Margin | See (8) | 68 | | | deg |
| $e_n$ | Input-Referred Voltage Noise | $R_L$ = open<br>f = 10 Hz | 170 | | | nV/√Hz |
| $i_n$ | Input-Referred Current Noise | $R_L$ = open<br>f = 10 Hz | 0.0002 | | | pA/√Hz |
| | Crosstalk Rejection | See (9) | 85 | | | dB |

(4) $R_L$ connected to $V^+/2$. For Sourcing Test, $V_O > V^+/2$. For Sinking tests, $V_O < V^+/2$.
(5) $V_{ID}$ is differential input voltage referenced to inverting input.
(6) Output shorted to ground for sourcing, and shorted to V+ for sinking short circuit current test.
(7) Slew rate is the slower of the rising and falling slew rates.
(8) See the Typical Performance Characteristics and Applications Information sections for more details.
(9) Input referred, $V^+$ = 10V and $R_L$ = 10 MΩ connected to 5V. Each amp excited in turn with 1 KHz to produce about 10 $V_{PP}$ output.

## Typical Performance Characteristics

$V_S$ = 5V, Single Supply, $T_A$ = 25°C unless otherwise specified

**Total Supply Current vs. Supply Voltage**

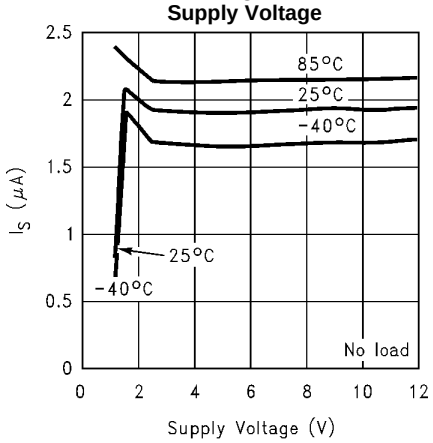



**Figure 2.**

**Total Supply Current vs. Supply Voltage (Negative Input Overdrive)**

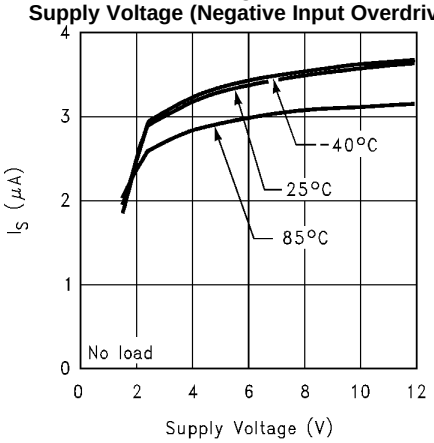



**Figure 3.**

**Total Supply Current vs. Supply Voltage (Positive Input Overdrive)**

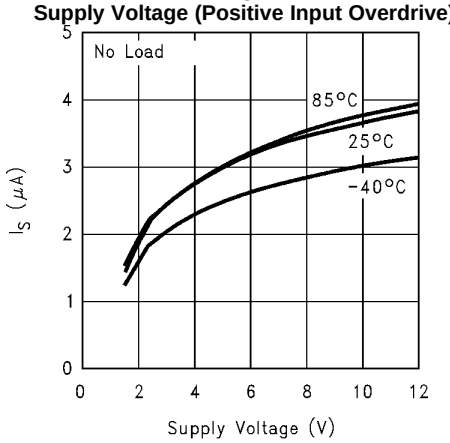



**Figure 4.**

**Input Bias Current vs. Temperature**

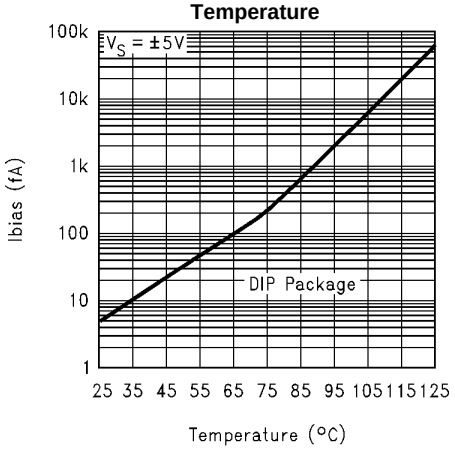



**Figure .**

**Offset Voltage vs. Common Mode Voltage ($V_S$ = 2.2V)**

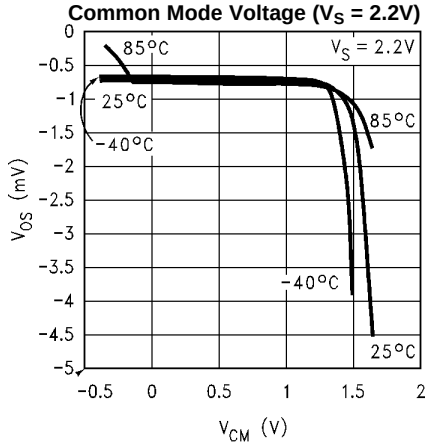



**Figure 5.**

**Offset Voltage vs. Common Mode Voltage ($V_S$ = 5V)**

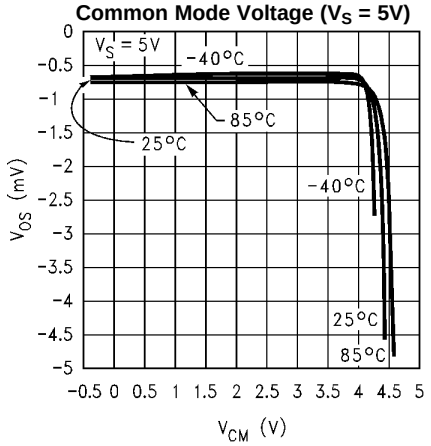



**Figure 6.**

## Typical Performance Characteristics (continued)

$V_S$ = 5V, Single Supply, $T_A$ = 25°C unless otherwise specified

**Offset Voltage vs. Common Mode Voltage ($V_S$ = 10V)**

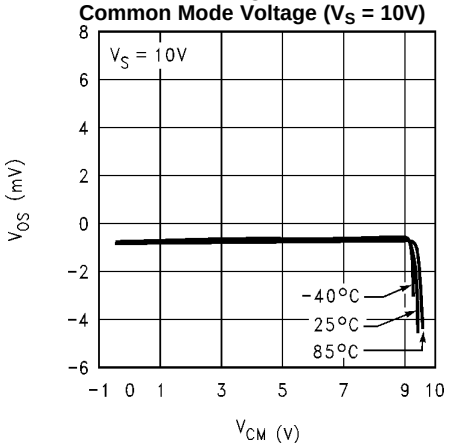



**Figure 7.**

**Swing Towards V⁻ vs. Supply Voltage**

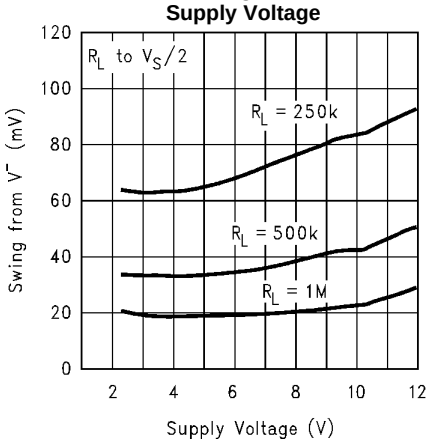



**Figure 8.**

**Swing Towards V⁺ vs. Supply Voltage**

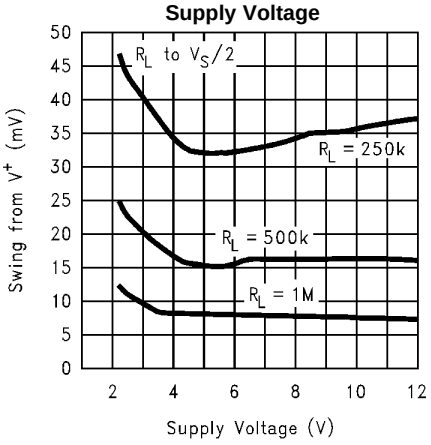



**Figure 9.**

**Swing From Rail(s) vs. Temperature**

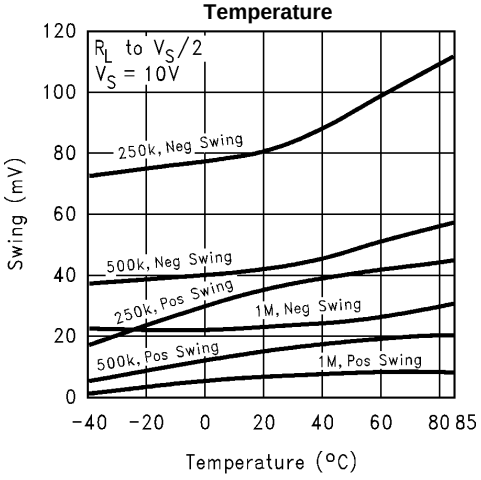



**Figure 10.**

**Output Source Current vs. Output Voltage**

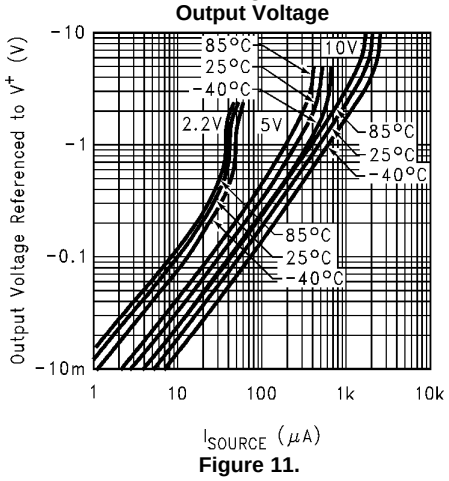



**Figure 11.**

**Output Sink Current vs. Output Voltage**

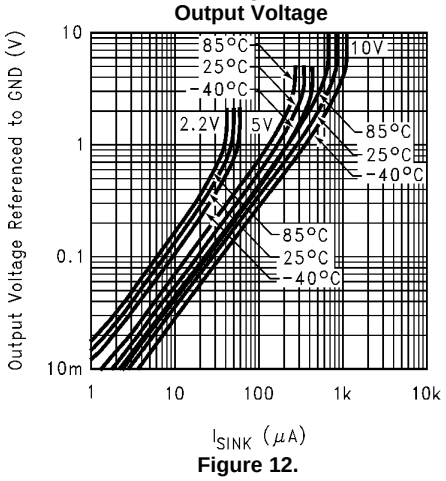



**Figure 12.**

## Typical Performance Characteristics (continued)

$V_S$ = 5V, Single Supply, $T_A$ = 25°C unless otherwise specified

**Maximum Output Voltage vs. Load Resistance**

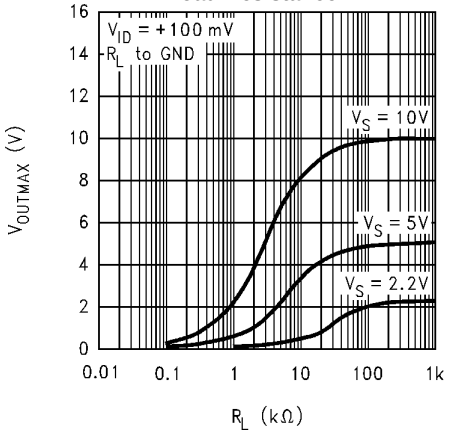



**Figure 13.**

**Large Signal Voltage Gain vs. Supply Voltage**

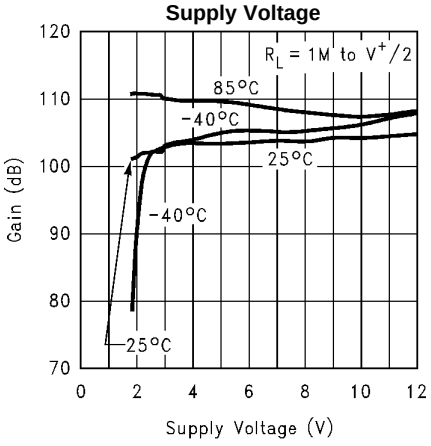



**Figure 14.**

**Open Loop Gain/Phase vs. Frequency**

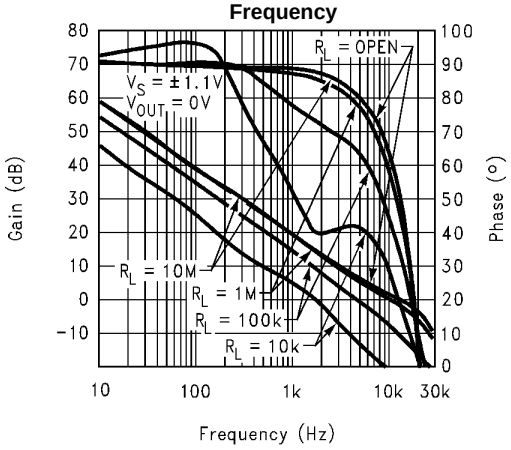



**Figure 15.**

**Open Loop Gain/Phase vs. Frequency For Various $C_L$ ($Z_L$ = 1 MΩ II $C_L$)**

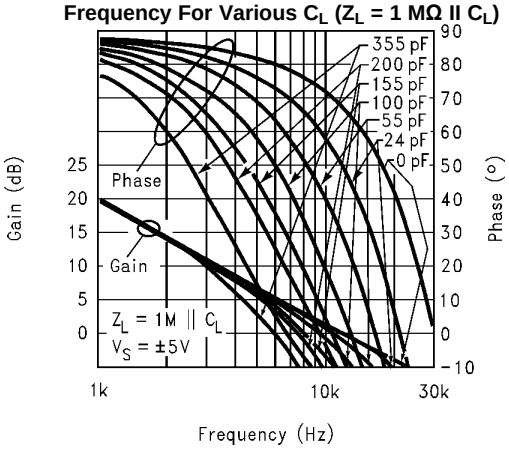



**Figure 16.**

**Open Loop Gain/Phase vs. Frequency For Various $C_L$ ($Z_L$ = 100 KΩ II $C_L$)**

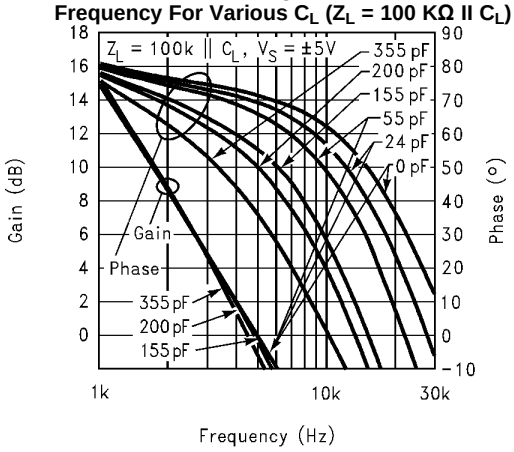



**Figure 17.**

**Gain Bandwidth Product vs. Supply Voltage**

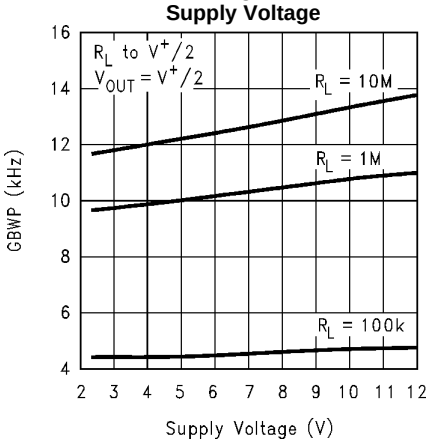



**Figure 18.**

## Typical Performance Characteristics (continued)

$V_S$ = 5V, Single Supply, $T_A$ = 25°C unless otherwise specified

**Phase Margin (Worst Case) vs. Supply Voltage**

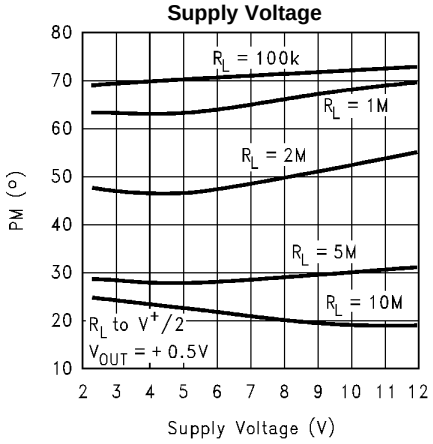



**Figure 19.**

**CMRR vs. Frequency**

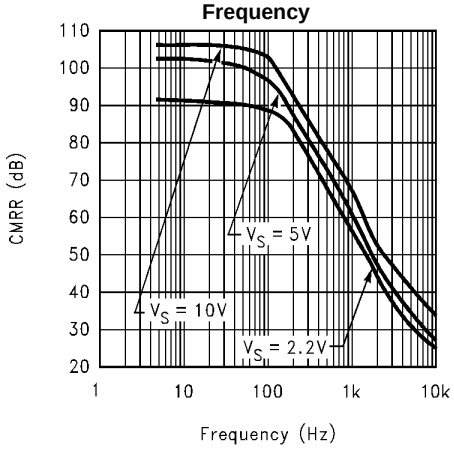



**Figure 20.**

**PSRR vs. Frequency**

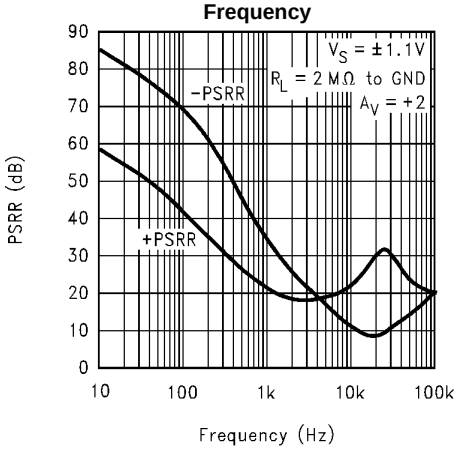



**Figure 21.**

**Positive Slew Rate vs. Supply Voltage**

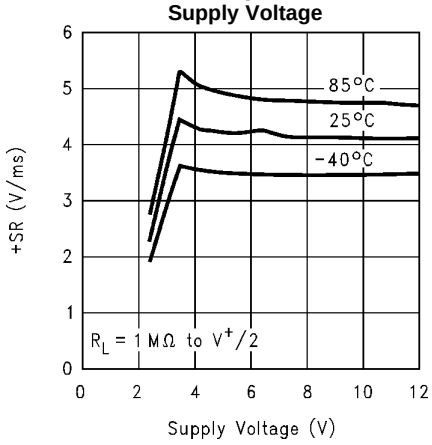



**Figure 22.**

**Negative Slew Rate vs. Supply Voltage**

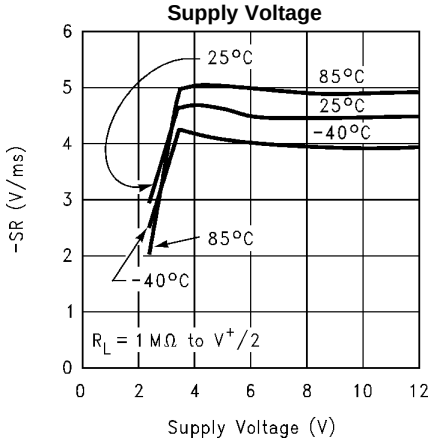



**Figure 23.**

**Cross-Talk Rejection vs. Frequency**

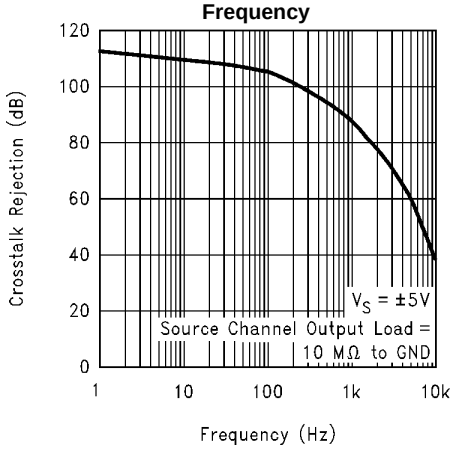



**Figure 24.**

## Typical Performance Characteristics (continued)

$V_S$ = 5V, Single Supply, $T_A$ = 25°C unless otherwise specified

**Input Voltage Noise vs. Frequency**

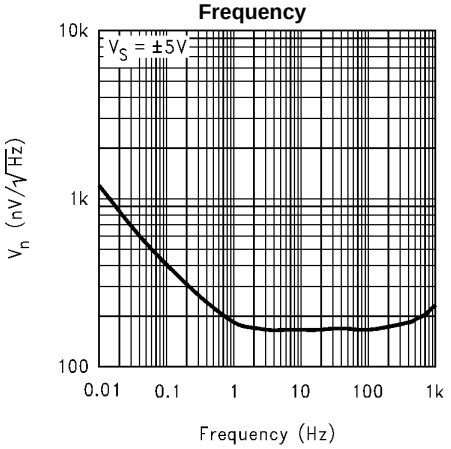



**Figure 25.**

**Output Impedance vs. Frequency**

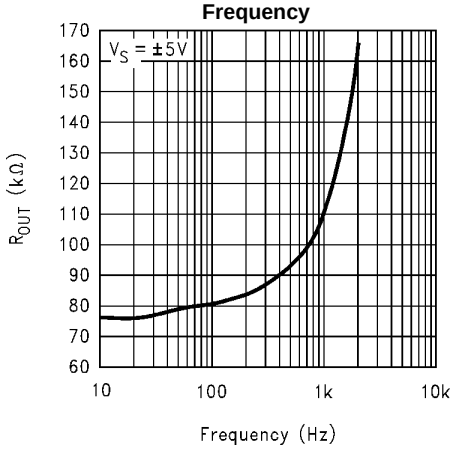



**Figure 26.**

**THD+N vs. Frequency**

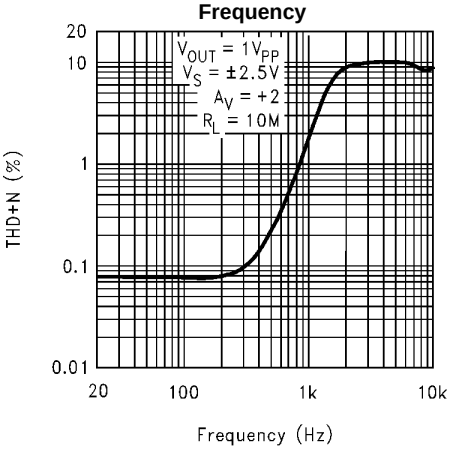



**Figure 27.**

**THD+N vs. Amplitude**

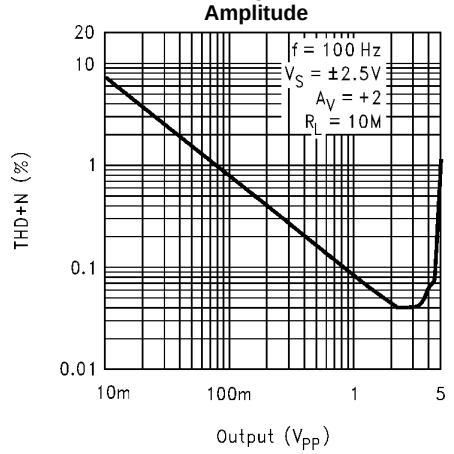



**Figure 28.**

**Maximum Output Swing vs. Frequency**

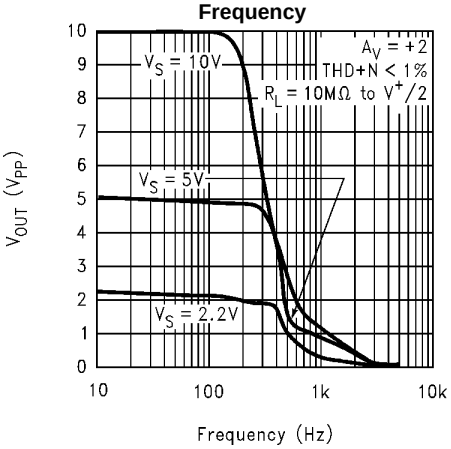



**Figure 29.**

**Small Signal Step Response ($A_V$ = +2) ($C_L$ = 12 pF, 100 pF)**

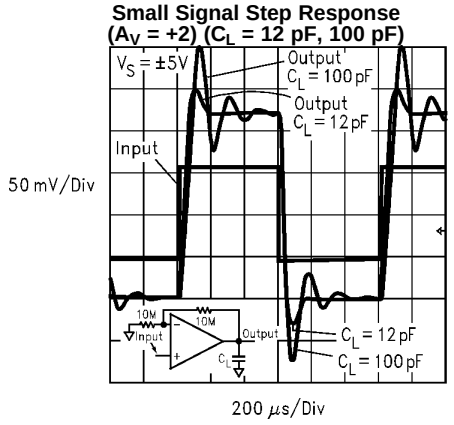



**Figure 30.**

## Typical Performance Characteristics (continued)

$V_S$ = 5V, Single Supply, $T_A$ = 25°C unless otherwise specified

**Large Signal Step Response ($A_V$ = +2) ($C_L$ = 100 pF)**

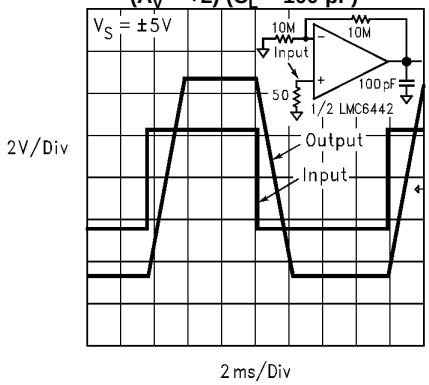



**Figure 31.**

**Small Signal Step Response ($A_V$ = −1) ($C_L$ = 1MΩ II 100 pF, 200 pF)**

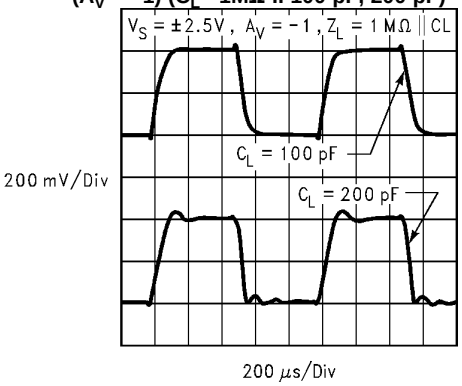



**Figure 32.**

**Small Signal Step Response ($A_V$ = +1) For Various $C_L$**

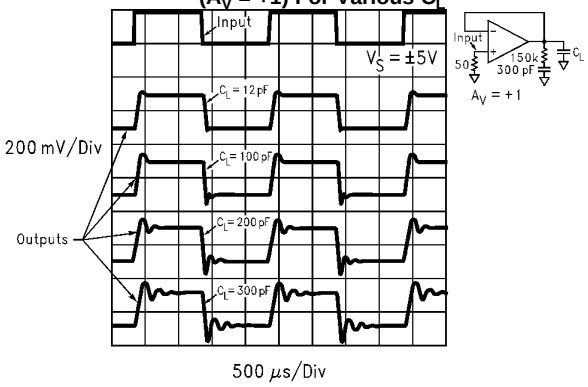



**Figure 33.**

**Large Signal Step Response ($A_V$ = +1) ($C_L$ = 200 pF)**

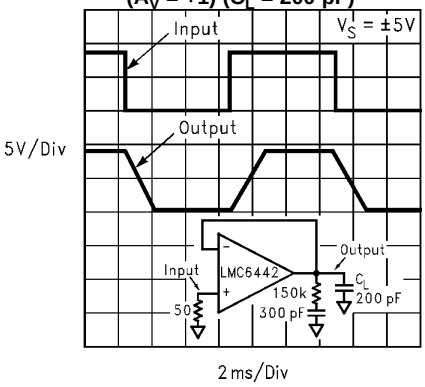



**Figure 34.**

## APPLICATIONS INFORMATION

### USING LMC6442 IN UNITY GAIN APPLICATIONS

LMC6442 is optimized for maximum bandwidth and minimal external components when operating at a minimum closed loop gain of +2 (or −1). However, it is also possible to operate the device in a unity gain configuration by adding external compensation as shown in Figure 35:

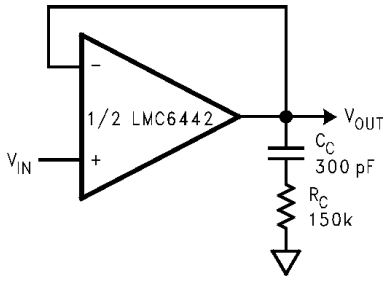



**Figure 35. $A_V$ = +1 Operation by adding $C_C$ and $R_C$**

Using this compensation technique it is possible to drive capacitive loads of up to 300 pF without causing oscillations (see the Typical Performance Characteristics for step response plots). This compensation can also be used with other gain settings in order to improve stability, especially when driving capacitive loads (for optimum performance, $R_C$ and $C_C$ may need to be adjusted).

### USING "T" NETWORK

Compromises need to be made whenever high gain inverting stages need to achieve a high input impedance as well. This is especially important in low current applications which tend to deal with high resistance values. Using a traditional inverting amplifier, gain is inversely proportional to the resistor value tied between the inverting terminal and input while the input impedance is equal to this value. For example, in order to build an inverting amplifier with an input impedance of 10MΩ and a gain of 100, one needs to come up with a feedback resistor of 1000 MΩ -an expensive task.

An alternate solution is to use a "T" Network in the feedback path, as shown in Figure 36.

Closed loop gain, $A_V$ is given by:

$$A_V = -\frac{R^2}{R2} \bullet \left(\frac{2}{R} + \frac{1}{R1}\right) \quad (1)$$

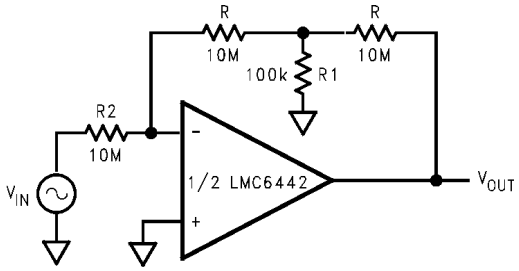



**Figure 36. "T" Network Used to Replace High Value Resistor**

It must be noted, however, that using this scheme, the realizable bandwidth would be less than the theoretical maximum. With feedback factor, β, defined as:

$$\beta \cong \frac{R2}{R2 + R} \bullet \frac{R1}{R1 + R} \quad \text{for } R2 \gg R1 \quad (2)$$

$$BW(-3\ dB) \approx GBWP \bullet \beta \quad (3)$$

In this case, assuming a GBWP of about 10 KHz, the expected BW would be around 50 Hz (vs. 100 Hz with the conventional inverting amplifier).

Looking at the problem from a different view, with $R_F$ defined by $A_V$•Rin, one could select a value for R in the "T" Network and then determine R1 based on this selection:

$$R1 = \frac{R^2}{R_F - 2R} \tag{4}$$

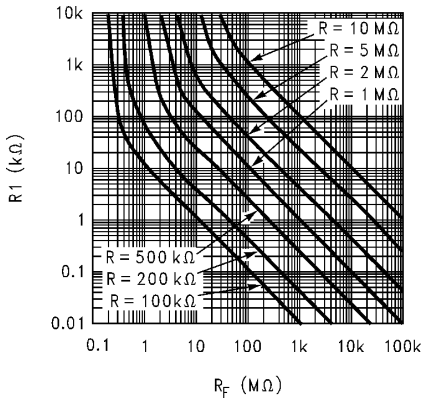



**Figure 37. "T" Network Values for Various Values of R**

For convenience, Figure 37 shows R1 vs. $R_F$ for different values of R.

## DESIGN CONSIDERATIONS FOR CAPACITIVE LOADS

As with many other opamps, the LMC6442 is more stable at higher closed loop gains when driving a capacitive load. Figure 38 shows minimum closed loop gain versus load capacitance, to achieve less than 10% overshoot in the output small signal response. In addition, the LMC6442 is more stable when it provides more output current to the load and when its output voltage does not swing close to $V^-$.

The LMC6442 is more tolerant to capacitive loads when the equivalent output load resistance is lowered or when output voltage is 1V or greater from the $V^-$ supply. The capacitive load drive capability is also improved by adding an isolating resistor in series with the load and the output of the device. Figure 39 shows the value of this resistor for various capacitive loads ($A_V$ = −1), while limiting the output to less than 10 % overshoot.

Referring to the Typical Performance Characteristics plot of Phase Margin (Worst Case) vs. Supply Voltage, note that Phase Margin increases as the equivalent output load resistance is lowered. This plot shows the expected Phase Margin when the device output is very close to $V^-$, which is the least stable condition of operation. Comparing this Phase Margin value to the one read off the Open Loop Gain/Phase vs. Frequency plot, one can predict the improvement in Phase Margin if the output does not swing close to $V^-$. This dependence of Phase Margin on output voltage is minimized as long as the output load, $R_L$, is about 1MΩ or less.

**Output Phase Reversal:** The LMC6442 is immune against this behavior even when the input voltages exceed the common mode voltage range.

**Output Time Delay:** Due to the ultra low power consumption of the device, there could be as long as 2.5 ms of time delay from when power is applied to when the device output reaches its final value.

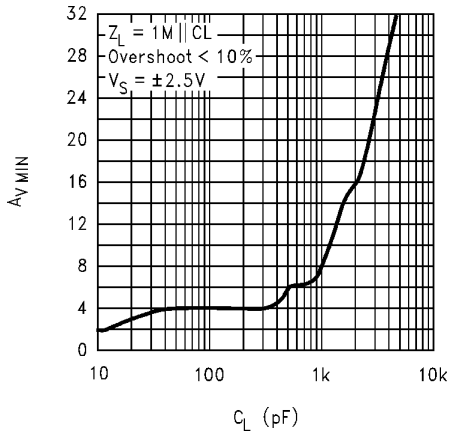



**Figure 38. Minimum Operating Gain vs. Capacitive Load**

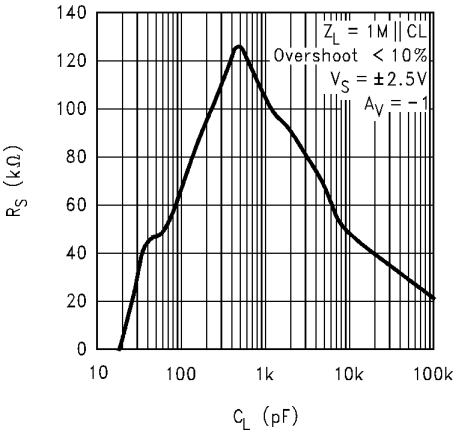
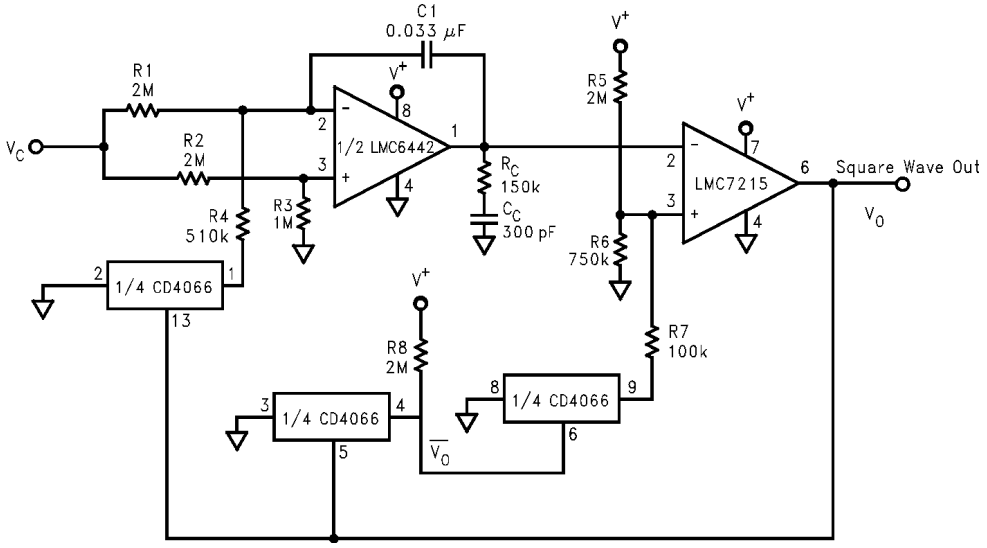



**Figure 39. Isolating Resistor Value vs Capacitive Load**

## Application Circuits




$V^+ = 5V$: $I_S < 10\ \mu A$, $f/V_C = 4.3\ (Hz/V)$

$$R1 \cong 4R4$$

$$R2 = 2R3$$

$$f(Hz) = \frac{V_C}{3R_1C_1V^+\left[\frac{R6}{R5+R6} - \frac{(R6 \parallel R7)}{(R6 \parallel R7)+R5}\right]} \cong \frac{V_C(R5+R6)}{3R_1C_1V^+(R6-R7)} \quad \text{for } R5 >> R6 \text{ and } R6 >> R7$$

**Figure 40. Micropower Single Supply Voltage to Frequency Converter**

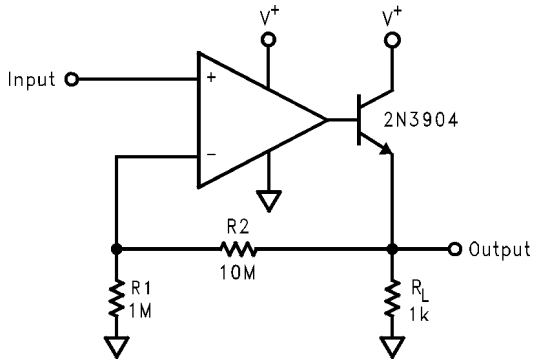



**Figure 41. Gain Stage with Current Boosting**

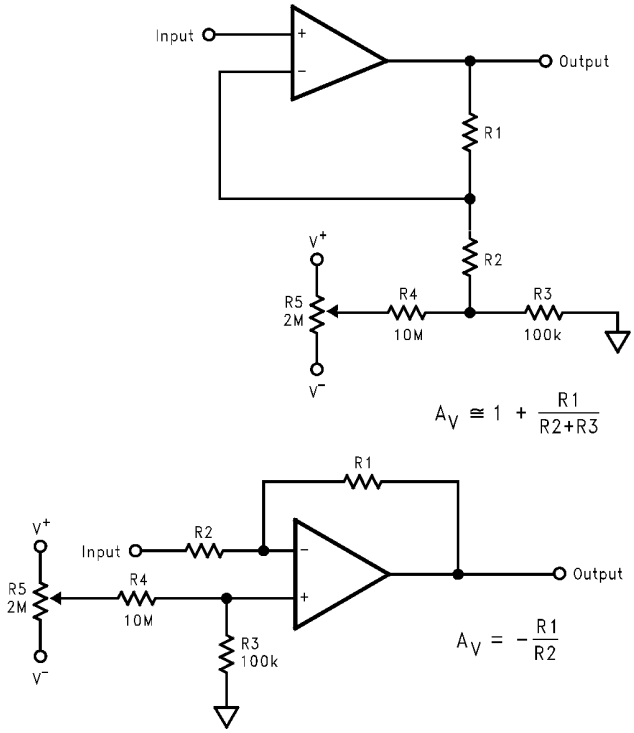



**Figure 42. Offset Nulling Schemes**

## REVISION HISTORY

| Changes from Revision D (March 2013) to Revision E | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 16 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMC6442AIM/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LMC64 42AIM | Samples |
| LMC6442AIMX | NRND | SOIC | D | 8 | | TBD | Call TI | Call TI | -40 to 85 | LMC64 42AIM | |
| LMC6442AIMX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LMC64 42AIM | Samples |
| LMC6442IM/NOPB | ACTIVE | SOIC | D | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | LMC64 42IM | Samples |
| LMC6442IMX/NOPB | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN \| Call TI | Level-1-260C-UNLIM | -40 to 85 | LMC64 42IM | Samples |
| LMC6442IN/NOPB | ACTIVE | PDIP | P | 8 | 40 | Green (RoHS & no Sb/Br) | CU SN | Level-1-NA-UNLIM | -40 to 85 | LMC6442 IN | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

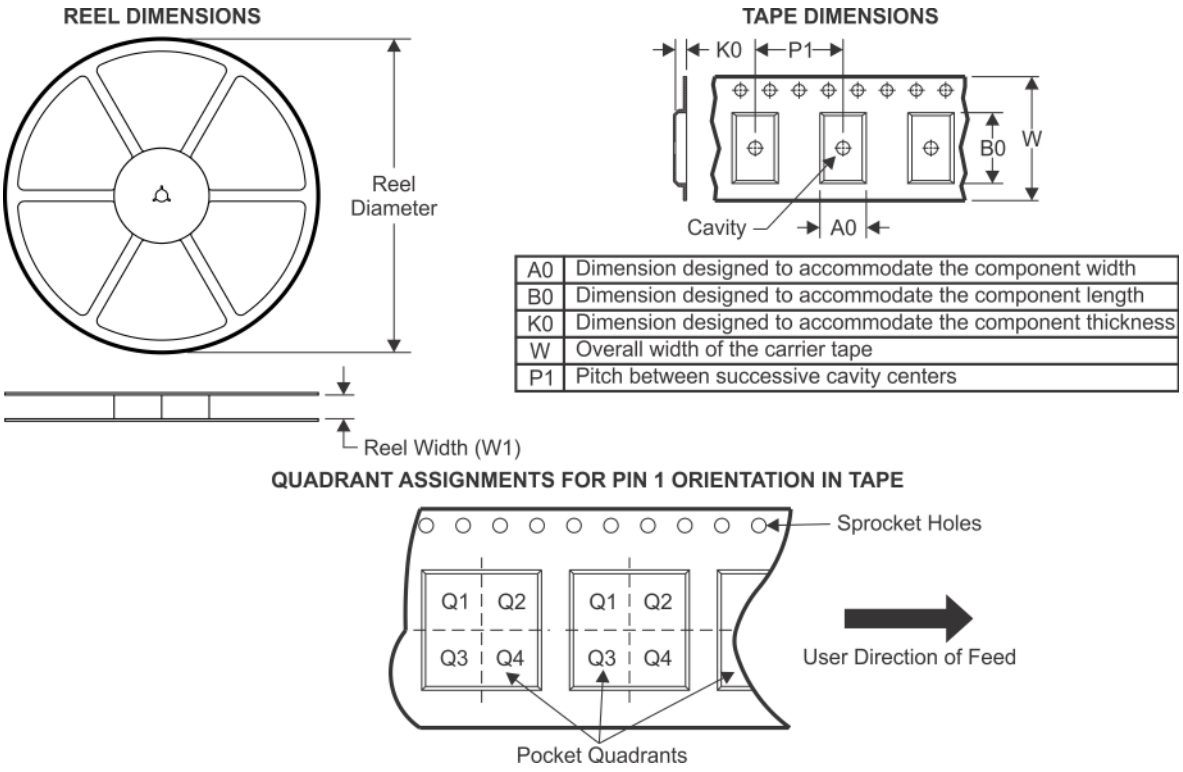
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

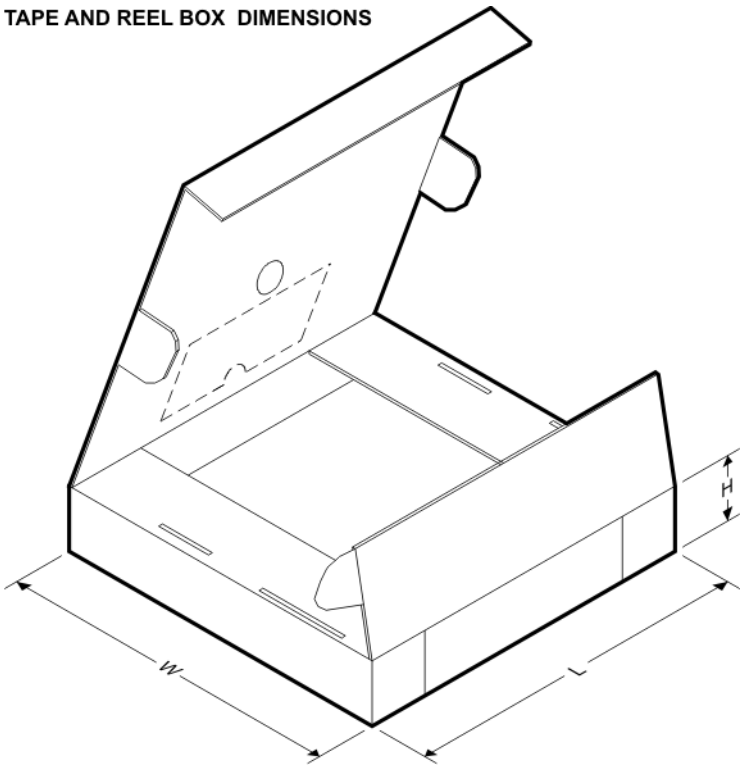



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMC6442AIMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LMC6442IMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |

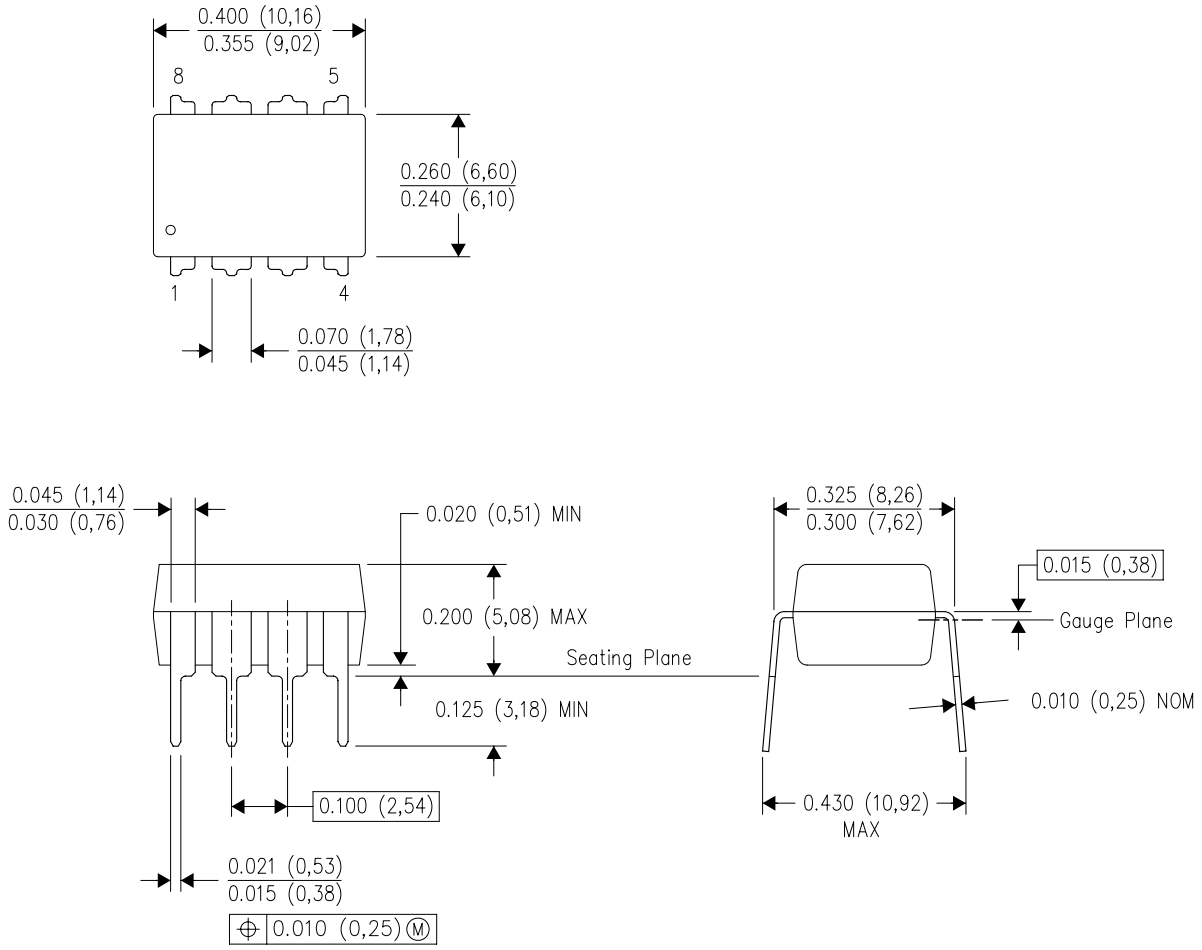
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

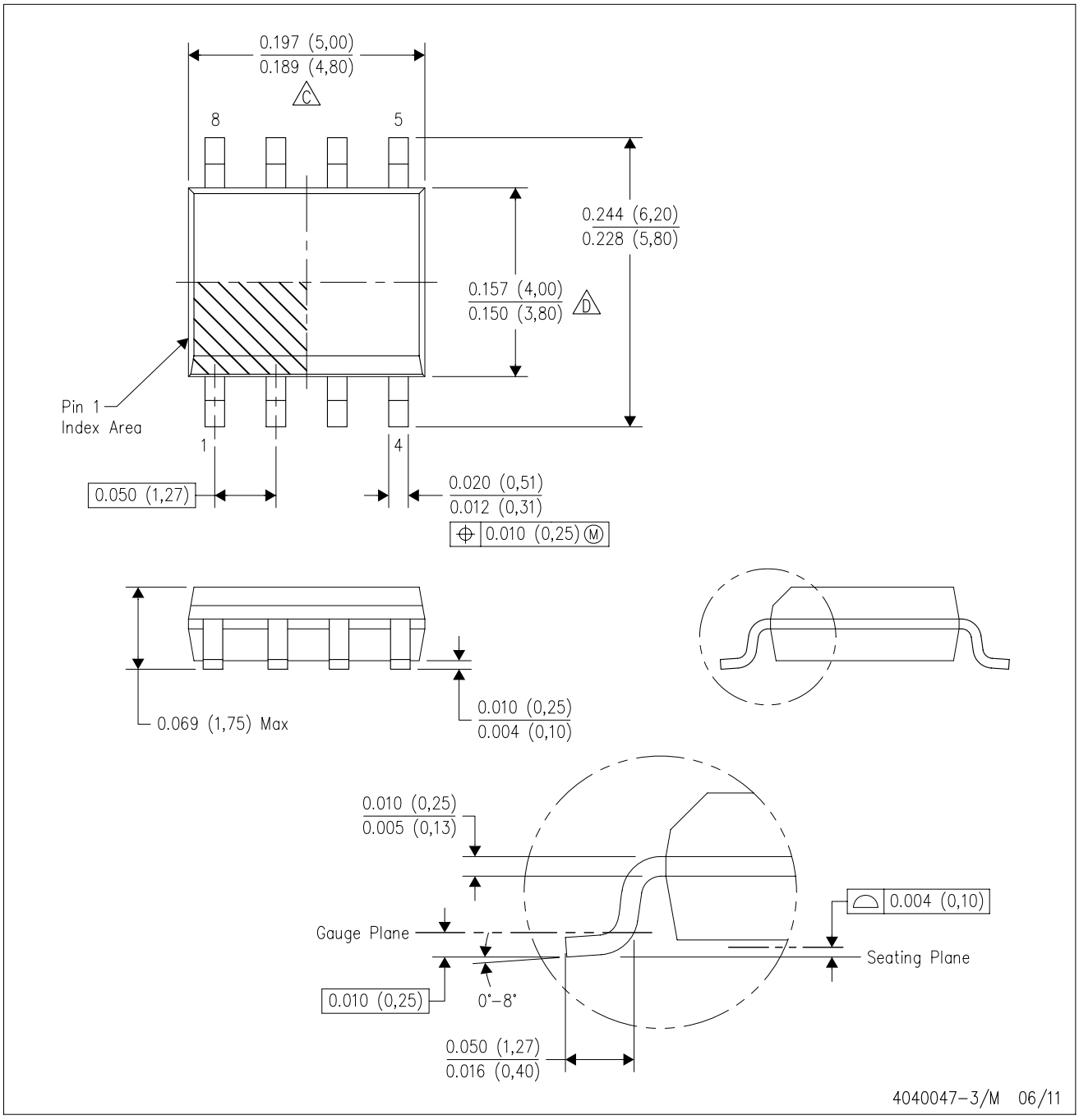
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMC6442AIMX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMC6442IMX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

## IMPORTANT NOTICE

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