Quad-port Gigabit Ethernet FMC

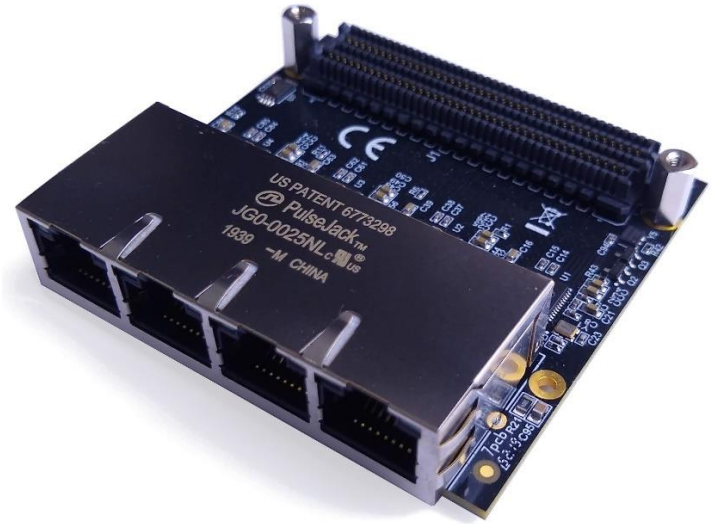
Overview

Description

The Ethernet FMC (FPGA Mezzanine Card) is an add-on/expansion board for FPGA and SoC based development boards. The mezzanine card has 4x Marvell 88E151x Gigabit Ethernet PHYs to provide 4 ports of gigabit Ethernet connectivity to the carrier development board.

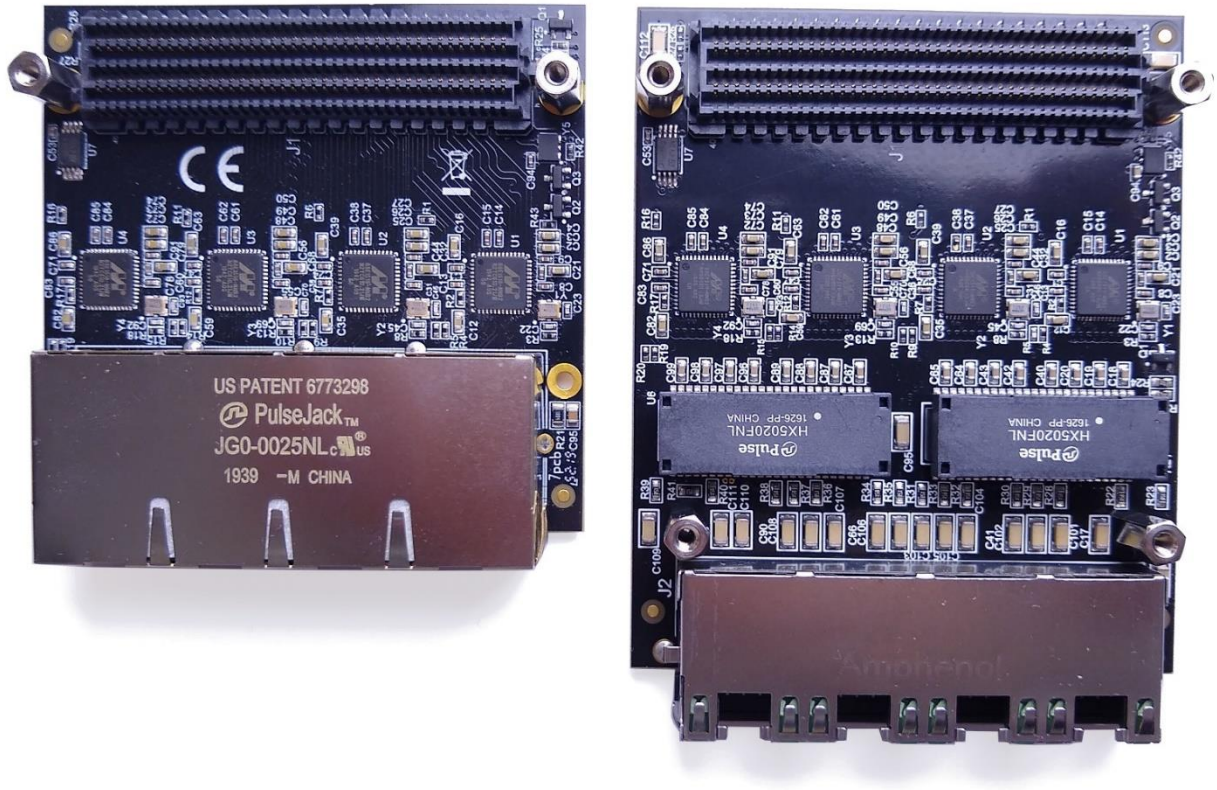
Features

- 4x Marvell 88E151x Gigabit Ethernet PHYs
- RGMII PHY interface
- Quad Ethernet RJ45 with magnetics
- FMC pinout conforms to VITA 57.1 FMC Standard
- Example designs with sources for several development boards
- Standalone and PetaLinux example designs



Variations

To enable support for the majority of FPGA/SoC development boards on the market, the Ethernet FMC is available in two models and two voltage specifications.



The image above illustrates the differences between the Ethernet FMC and Robust Ethernet FMC. They are two physically different boards, however they use the same pinout on the FMC connector, allowing them to be used interchangeably with the same software running on the carrier board. The main difference between the boards is that the Robust Ethernet FMC uses Ethernet magnetics that are external to the RJ45 connector. This allows the Robust Ethernet FMC to have a height profile that is physically compatible with more carrier boards than the Ethernet FMC. For more detail, see Mechanical Information.

Both the Ethernet FMC and the Robust Ethernet FMC are available in two different voltage ratings: 1.8VDC and 2.5VDC.

The table below lists the 4 variations and their part numbers.

Part name	Voltage rating (VADJ)	Part number
Ethernet FMC 1.8V	1.8VDC	OP031-1V8
Ethernet FMC 2.5V	2.5VDC	OP031-2V5
Robust Ethernet FMC 1.8V	1.8VDC	OP041-1V8
Robust Ethernet FMC 2.5V	2.5VDC	OP041-2V5

To determine which Ethernet FMC is compatible with your development board, please refer to the list of compatible boards in the User Guide.

Pin Configuration

Pinout table

The Ethernet FMC has a low pin count FPGA Mezzanine Card (FMC) connector, providing the connections to the FPGA on the development board. The following table defines the pinout of the FMC connector and applies to both the Ethernet FMC and the Robust Ethernet FMC.

Pin	Pin name	Net	Description
C1	GND	GND	Ground
C2	DP0_C2M_P	DP0_C2M_P	Not used
C3	DP0_C2M_N	DP0_C2M_N	Not used
C4	GND	GND	Ground
C5	GND	GND	Ground
C6	DP0_M2C_P	DP0_M2C_P	Not used
C7	DP0_M2C_N	DP0_M2C_N	Not used
C8	GND	GND	Ground
C9	GND	GND	Ground
C10	LA06_P	E1_RXD0	Port 1 RGMII Receive Data Bit 0 (PHY-to-FPGA)
C11	LA06_N	E0_MDIO	Port 0 MDIO Data (bidirectional)
C12	GND	GND	Ground
C13	GND	GND	Ground

C14	LA10_P	N/C	Not used
C15	LA10_N	E1_RXD2	Port 1 RGMII Receive Data Bit 2 (PHY-to-FPGA)
C16	GND	GND	Ground
C17	GND	GND	Ground
C18	LA14_P	REF_CLK_FSEL	Reserved
C19	LA14_N	E1_MDIO	Port 1 MDIO Data (bidirectional)
C20	GND	GND	Ground
C21	GND	GND	Ground
C22	LA18_P_CC	E3_RX_CLK	Port 3 RGMII Receive Clock (PHY-to-FPGA)
C23	LA18_N_CC	E3_RX_CTRL	Port 3 RGMII Receive Control (PHY-to-FPGA)
C24	GND	GND	Ground
C25	GND	GND	Ground
C26	LA27_P	E3_RXD1	Port 3 RGMII Receive Data Bit 1 (PHY-to-FPGA)
C27	LA27_N	E3_RXD3	Port 3 RGMII Receive Data Bit 3 (PHY-to-FPGA)
C28	GND	GND	Ground
C29	GND	GND	Ground
C30	SCL	I2C_SCL	I2C Clock (FPGA-to-PHY)
C31	SDA	I2C_SDA	I2C Data (bidirectional)
C32	GND	GND	Ground
C33	GND	GND	Ground
C34	GA0	GA0	EEPROM Address Bit 1 (A1)

C35	12P0V_1	12V0	12VDC (Not used)
C36	GND	GND	Ground
C37	12P0V_2	12V0	12VDC (Not used)
C38	GND	GND	Ground
C39	3P3V_1	3V3	3.3VDC
C40	GND	GND	Ground
D1	PG_C2M	PG	Power Good (Driven by carrier)
D2	GND	GND	Ground
D3	GND	GND	Ground
D4	GBTCLK0_M2C_P	N/C	Not used
D5	GBTCLK0_M2C_N	N/C	Not used
D6	GND	GND	Ground
D7	GND	GND	Ground
D8	LA01_P_CC	E1_RX_CLK	Port 1 RGMII Receive Clock (PHY-to-FPGA)
D9	LA01_N_CC	E1_RX_CTRL	Port 1 RGMII Receive Control (PHY-to-FPGA)
D10	GND	GND	Ground
D11	LA05_P	E0_MDC	Port 0 MDIO Clock (FPGA-to-PHY)
D12	LA05_N	E0_RESET_N	Port 0 PHY Reset (Active-Low)
D13	GND	GND	Ground
D14	LA09_P	E1_RXD1	Port 1 RGMII Receive Data Bit 1 (PHY-to-FPGA)
D15	LA09_N	E1_RXD3	Port 1 RGMII Receive Data Bit 3 (PHY-to-FPGA)
D16	GND	GND	Ground

D17	LA13_P	REF_CLK_OE	Enable LVDS 125MHz Clock (Active-High, enabled by default with pull-up)
D18	LA13_N	E1_MDC	Port 1 MDIO Clock (FPGA-to-PHY)
D19	GND	GND	Ground
D20	LA17_P_CC	E2_RX_CLK	Port 2 RGMII Receive Clock (PHY-to-FPGA)
D21	LA17_N_CC	N/C	Not used
D22	GND	GND	Ground
D23	LA23_P	E2_RXD2	Port 2 RGMII Receive Data Bit 2 (PHY-to-FPGA)
D24	LA23_N	E2_RXD3	Port 2 RGMII Receive Data Bit 3 (PHY-to-FPGA)
D25	GND	GND	Ground
D26	LA26_P	E3_RXD0	Port 3 RGMII Receive Data Bit 0 (PHY-to-FPGA)
D27	LA26_N	E3_RXD2	Port 3 RGMII Receive Data Bit 2 (PHY-to-FPGA)
D28	GND	GND	Ground
D29	TCK	N/C	Not used
D30	TDI	TDI-TDO	JTAG TDI (Connects to TDO to close JTAG chain)
D31	TDO	TDI-TDO	JTAG TDO (Connects to TDI to close JTAG chain)
D32	3P3VAUX	N/C	Not used
D33	TMS	N/C	Not used
D34	TRST_L	N/C	Not used

D35	GA1	GA1	EEPROM Address Bit 0 (A0)
D36	3P3V_2	3V3	3.3VDC
D37	GND	GND	Ground
D38	3P3V_3	3V3	3.3VDC
D39	GND	GND	Ground
D40	3P3V_4	3V3	3.3VDC
G1	GND	GND	Ground
G2	CLK1_M2C_P	N/C	Not used
G3	CLK1_M2C_N	N/C	Not used
G4	GND	GND	Ground
G5	GND	GND	Ground
G6	LA00_P_CC	E0_RX_CLK	Port 0 RGMII Receive Clock (PHY-to-FPGA)
G7	LA00_N_CC	E0_RX_CTRL	Port 0 RGMII Receive Control (PHY-to-FPGA)
G8	GND	GND	Ground
G9	LA03_P	E0_RXD2	Port 0 RGMII Receive Data Bit 2 (PHY-to-FPGA)
G10	LA03_N	E0_RXD3	Port 0 RGMII Receive Data Bit 3 (PHY-to-FPGA)
G11	GND	GND	Ground
G12	LA08_P	E0_TXD1	Port 0 RGMII Transmit Data Bit 1 (FPGA-to-PHY)
G13	LA08_N	E0_TXD2	Port 0 RGMII Transmit Data Bit 2 (FPGA-to-PHY)
G14	GND	GND	Ground

G15	LA12_P	N/C	Not used
G16	LA12_N	E1_TXD0	Port 1 RGMII Transmit Data Bit 0 (FPGA-to-PHY)
G17	GND	GND	Ground
G18	LA16_P	E1_TXD2	Port 1 RGMII Transmit Data Bit 2 (FPGA-to-PHY)
G19	LA16_N	E1_TXD3	Port 1 RGMII Transmit Data Bit 3 (FPGA-to-PHY)
G20	GND	GND	Ground
G21	LA20_P	E2_RX_CTRL	Port 2 RGMII Receive Control (PHY-to-FPGA)
G22	LA20_N	E2_RXD0	Port 2 RGMII Receive Data Bit 0 (PHY-to-FPGA)
G23	GND	GND	Ground
G24	LA22_P	E2_TXD1	Port 2 RGMII Transmit Data Bit 1 (FPGA-to-PHY)
G25	LA22_N	E2_TXD2	Port 2 RGMII Transmit Data Bit 2 (FPGA-to-PHY)
G26	GND	GND	Ground
G27	LA25_P	E2_TX_CTRL	Port 2 RGMII Transmit Control (FPGA-to-PHY)
G28	LA25_N	E2_MDIO	Port 2 MDIO Data (bidirectional)
G29	GND	GND	Ground
G30	LA29_P	N/C	Not used
G31	LA29_N	E3_TXD0	Port 3 RGMII Transmit Data Bit 0 (FPGA-to-PHY)

G32	GND	GND	Ground
G33	LA31_P	E3_TXD2	Port 3 RGMII Transmit Data Bit 2 (FPGA-to-PHY)
G34	LA31_N	E3_TXD3	Port 3 RGMII Transmit Data Bit 3 (FPGA-to-PHY)
G35	GND	GND	Ground
G36	LA33_P	N/C	Not used
G37	LA33_N	N/C	Not used
G38	GND	GND	Ground
G39	VADJ_3	VADJ	I/O Supply Voltage (1.8VDC or 2.5VDC)
G40	GND	GND	Ground
H1	VREF_A_M2C	N/C	Not used
H2	PRSNT_M2C_L	GND	Ground
H3	GND	GND	Ground
H4	CLK0_M2C_P	REF_CLK_P	LVDS 125MHz Precision Clock to FPGA
H5	CLK0_M2C_N	REF_CLK_N	LVDS 125MHz Precision Clock to FPGA
H6	GND	GND	Ground
H7	LA02_P	E0_RXD0	Port 0 RGMII Receive Data Bit 0 (PHY-to-FPGA)
H8	LA02_N	E0_RXD1	Port 0 RGMII Receive Data Bit 1 (PHY-to-FPGA)
H9	GND	GND	Ground
H10	LA04_P	E0_TXD0	Port 0 RGMII Transmit Data Bit 0 (FPGA-to-PHY)

H11	LA04_N	E0_TX_CLK	Port 0 RGMII Transmit Clock (FPGA-to-PHY)
H12	GND	GND	Ground
H13	LA07_P	E0_TXD3	Port 0 RGMII Transmit Data Bit 3 (FPGA-to-PHY)
H14	LA07_N	E0_TX_CTRL	Port 0 RGMII Transmit Control (FPGA-to-PHY)
H15	GND	GND	Ground
H16	LA11_P	E1_TXD1	Port 1 RGMII Transmit Data Bit 1 (FPGA-to-PHY)
H17	LA11_N	E1_TX_CLK	Port 1 RGMII Transmit Clock (FPGA-to-PHY)
H18	GND	GND	Ground
H19	LA15_P	E1_TX_CTRL	Port 1 RGMII Transmit Control (FPGA-to-PHY)
H20	LA15_N	E1_RESET_N	Port 1 PHY Reset (Active-Low)
H21	GND	GND	Ground
H22	LA19_P	E2_RXD1	Port 2 RGMII Receive Data Bit 1 (PHY-to-FPGA)
H23	LA19_N	E2_TXD0	Port 2 RGMII Transmit Data Bit 0 (FPGA-to-PHY)
H24	GND	GND	Ground
H25	LA21_P	E2_TX_CLK	Port 2 RGMII Transmit Clock (FPGA-to-PHY)
H26	LA21_N	E2_TXD3	Port 2 RGMII Transmit Data Bit 3 (FPGA-to-PHY)
H27	GND	GND	Ground
H28	LA24_P	E2_MDC	Port 2 MDIO Clock (FPGA-to-PHY)

H29	LA24_N	E2_RESET_N	Port 2 PHY Reset (Active-Low)
H30	GND	GND	Ground
H31	LA28_P	E3_TXD1	Port 3 RGMII Transmit Data Bit 1 (FPGA-to-PHY)
H32	LA28_N	E3_TX_CLK	Port 3 RGMII Transmit Clock (FPGA-to-PHY)
H33	GND	GND	Ground
H34	LA30_P	E3_TX_CTRL	Port 3 RGMII Transmit Control (FPGA-to-PHY)
H35	LA30_N	E3_MDC	Port 3 MDIO Clock (FPGA-to-PHY)
H36	GND	GND	Ground
H37	LA32_P	E3_MDIO	Port 3 MDIO Data (bidirectional)
H38	LA32_N	E3_RESET_N	Port 3 PHY Reset (Active-Low)
H39	GND	GND	Ground
H40	VADJ_4	VADJ	I/O Supply Voltage (1.8VDC or 2.5VDC)

Net lengths

The table below lists the trace lengths.

	Net	Length (mils)
Port 0	E0_TXD0	935.369
	E0_TXD1	1022.274
	E0_TXD2	1016.451
	E0_TXD3	973.815
	E0_TX_CLK	926.463

	E0_TX_CTRL	1025.089
	E0_RXD0	987.273
	E0_RXD1	1034.127
	E0_RXD2	1066.126
	E0_RXD3	989.16
	E0_RX_CLK	1055.744
	E0_RX_CTRL	1018.718
Port 1	E1_TXD0	821.649
	E1_TXD1	781.117
	E1_TXD2	830.455
	E1_TXD3	867.309
	E1_TX_CLK	767.898
	E1_TX_CTRL	847.395
	E1_RXD0	1336.123
	E1_RXD1	1345.882
	E1_RXD2	1336.42
	E1_RXD3	1296.088
	E1_RX_CLK	1262.112
	E1_RX_CTRL	1277.099
Port 2	E2_TXD0	910.149
	E2_TXD1	902.087
	E2_TXD2	922.798
	E2_TXD3	882.68

	E2_TX_CLK	895.55
	E2_TX_CTRL	968.80
	E2_RXD0	1106.905
	E2_RXD1	1133.374
	E2_RXD2	1165.735
	E2_RXD3	1169.388
	E2_RX_CLK	1105.029
	E2_RX_CTRL	1143.103
Port 3	E3_TXD0	1046.468
	E3_TXD1	983.755
	E3_TXD2	1062.666
	E3_TXD3	1075.708
	E3_TX_CLK	995.204
	E3_TX_CTRL	1056.065
	E3_RXD0	1535.853
	E3_RXD1	1502.359
	E3_RXD2	1499.971
	E3_RXD3	1590.42
	E3_RX_CLK	1512.856
	E3_RX_CTRL	1545.37

Specifications

Recommended Operating Conditions

SUPPLY VOLTAGE	MIN	TYP	MAX	UNIT
12 VDC	+11.4	+12	+12.6	V
3.3 VDC	+3.14	+3.3	+3.46	V
VADJ 2.5VDC	+2.38	+2.5	+2.62	V
VADJ 1.8VDC	+1.71	+1.8	+1.89	V

Power Consumption

The specifications below refer to the total current draw on each of the power supplies while the Ethernet FMC is connected to a development board and operating at 100% channel utilization.

SUPPLY	UTILIZATION	MIN	TYP	MAX	UNIT
12 VDC	100%		0		mA
3.3 VDC	100%		740		mA
VADJ 2.5 VDC	100%		144		mA
VADJ 1.8 VDC	100%		144		mA

- Tests performed at ambient temperature of 25 degrees C
- Tests performed using IP in the FPGA to generate the Ethernet packets

Note that Ethernet FMC usage will typically produce an increase in power consumption of the FPGA on the development board. This is due to the peripherals and IP that must be enabled in the FPGA to engage with the Ethernet PHYs. Also note that the total power consumption of the Ethernet FMC and development board is dependent on the ambient temperature and channel utilization.

Thermal Information

We have not performed comprehensive thermal testing on the Ethernet FMC, however we recommend that it be operated under ambient temperatures between 0 and 70 degrees C. This advice is based on the recommended ambient operating temperatures of the critical devices on the Ethernet FMC. These temperatures are listed in the table below.

Ethernet FMC Component Ambient Operating Temperatures

DEVICE	MIN	MAX	UNIT
Ethernet PHY	0	70	C
25MHz Crystal	-10	70	C
EEPROM	-40	85	C
MOSFET (FDV303N)	-55	150	C
125MHz LVDS Clock Oscillator	-20	70	C
RJ45 Connector (JG0-0025NL)	0	70	C
RJ45 Connector (LPJG48851AFNL)	0	70	C

Robust Ethernet FMC Component Ambient Operating Temperatures

DEVICE	MIN	MAX	UNIT
Ethernet PHY	0	70	C
25MHz Crystal	-10	70	C
EEPROM	-40	85	C
MOSFET (FDV303N)	-55	150	C
125MHz LVDS Clock Oscillator	-20	70	C

Ethernet Magnetics (HX5020FNL)	-40	85	C
Ethernet Magnetics (LP5020NLR)	-40	85	C
RJ45 Connector (RJE72-488-1411)	-40	85	C

Components that are not listed in the table above (such as resistors, capacitors) are selected to have minimum operating temperature that is lower than 0 degrees C, and maximum operating temperature that is greater than 70 degrees C.

Reset Timing

When hardware resetting the PHYs, we recommend using this timing:

1. Hold the RESET_N signal LOW for 10ms
2. Release the RESET_N signal (HIGH) and wait for 5ms

I2C (EEPROM) Timing

The serial EEPROM (part number M24C02-FDW6TP) has a maximum operating clock frequency of 400 kHz.

MDIO Timing

- The maximum MDC frequency supported by the 88E151x PHY is 12MHz.

88E151x Electrical and Timing

For electrical specs and timing related to the 88E151x signals listed below, please refer to the Marvell 88E151x public datasheet :

- Reset
- RGMII
- MDIO

Certifications

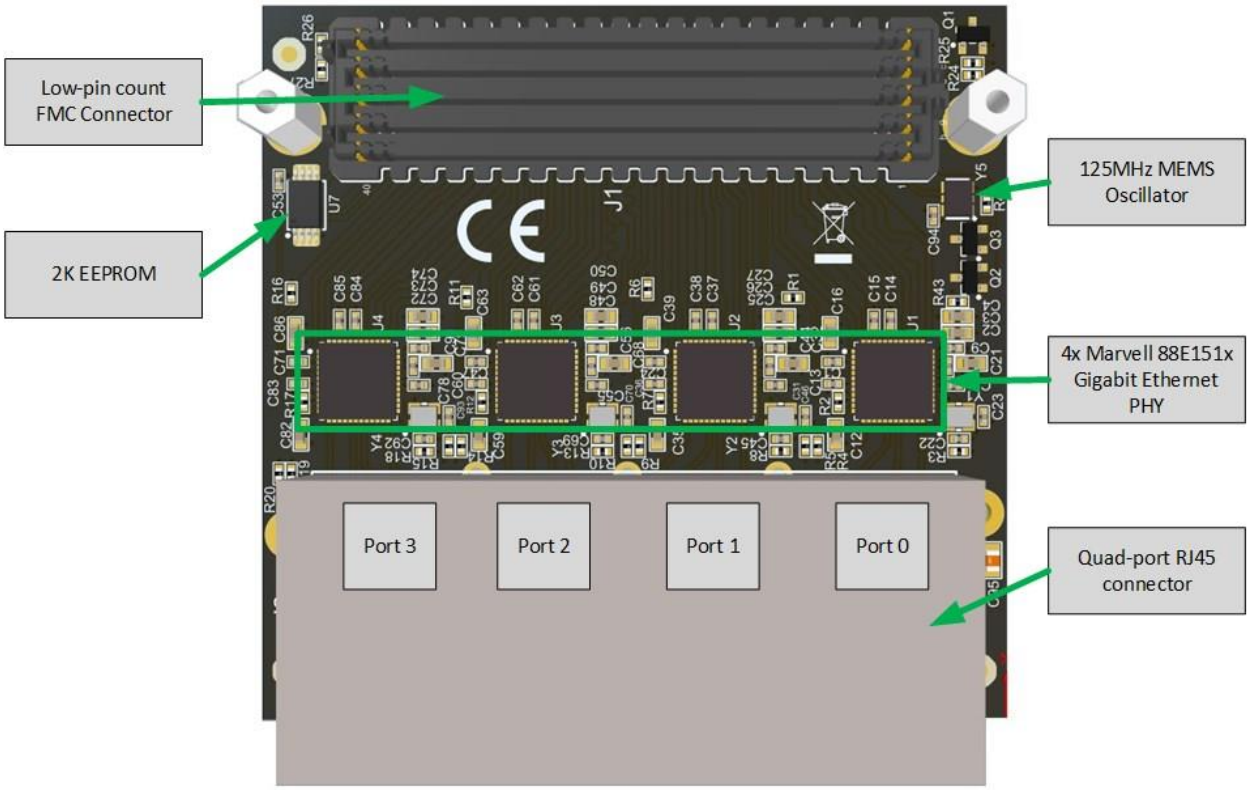
- RoHS
- CE

Detailed Description

Hardware Overview

Ethernet FMC

The figure below illustrates the various hardware components that are located on the top-side of the Ethernet FMC.

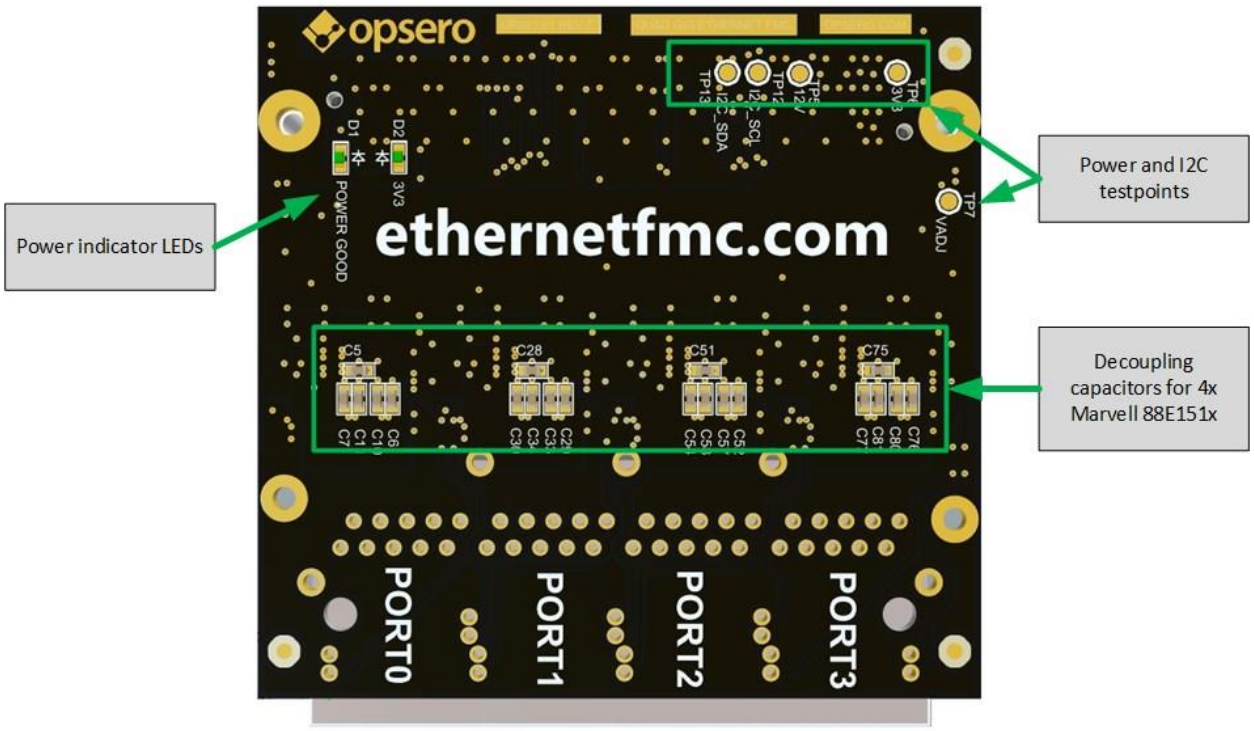


The main components on the top-side of the mezzanine card are:

- 4x Marvell 88E151x Gigabit Ethernet PHYs
- Low Pin Count FMC Connector
- 2K EEPROM
- 125MHz MEMS Clock Oscillator
- 4x 25MHz crystals

- Quad-port RJ45 connector

The figure below illustrates the various hardware components that are located on the bottom-side of the mezzanine card.

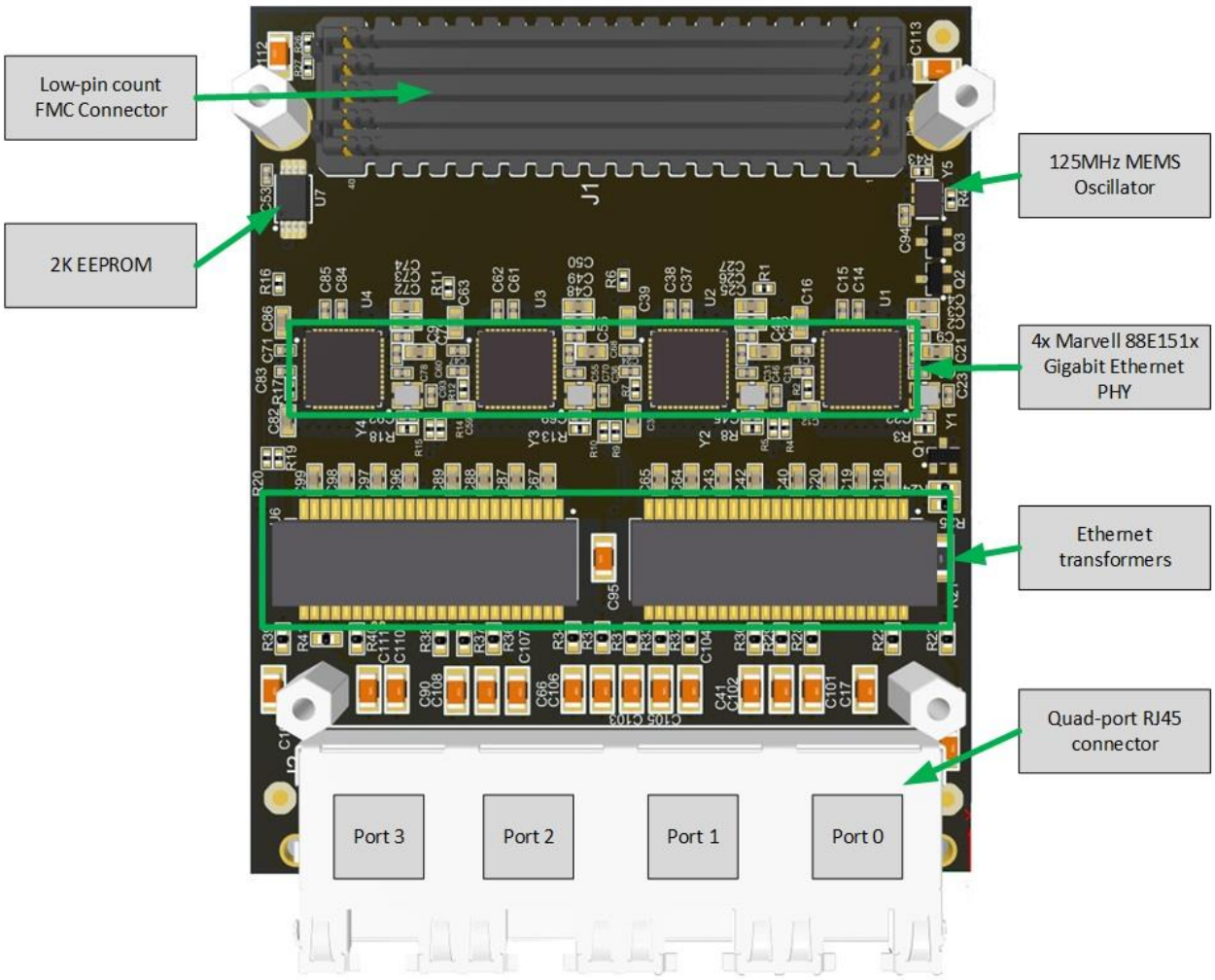


The main components on the bottom-side of the mezzanine card are:

- Decoupling capacitors for the Marvell 88E151x Ethernet PHYs
- Power indicator LEDs
- Test points for power and I2C

Robust Ethernet FMC

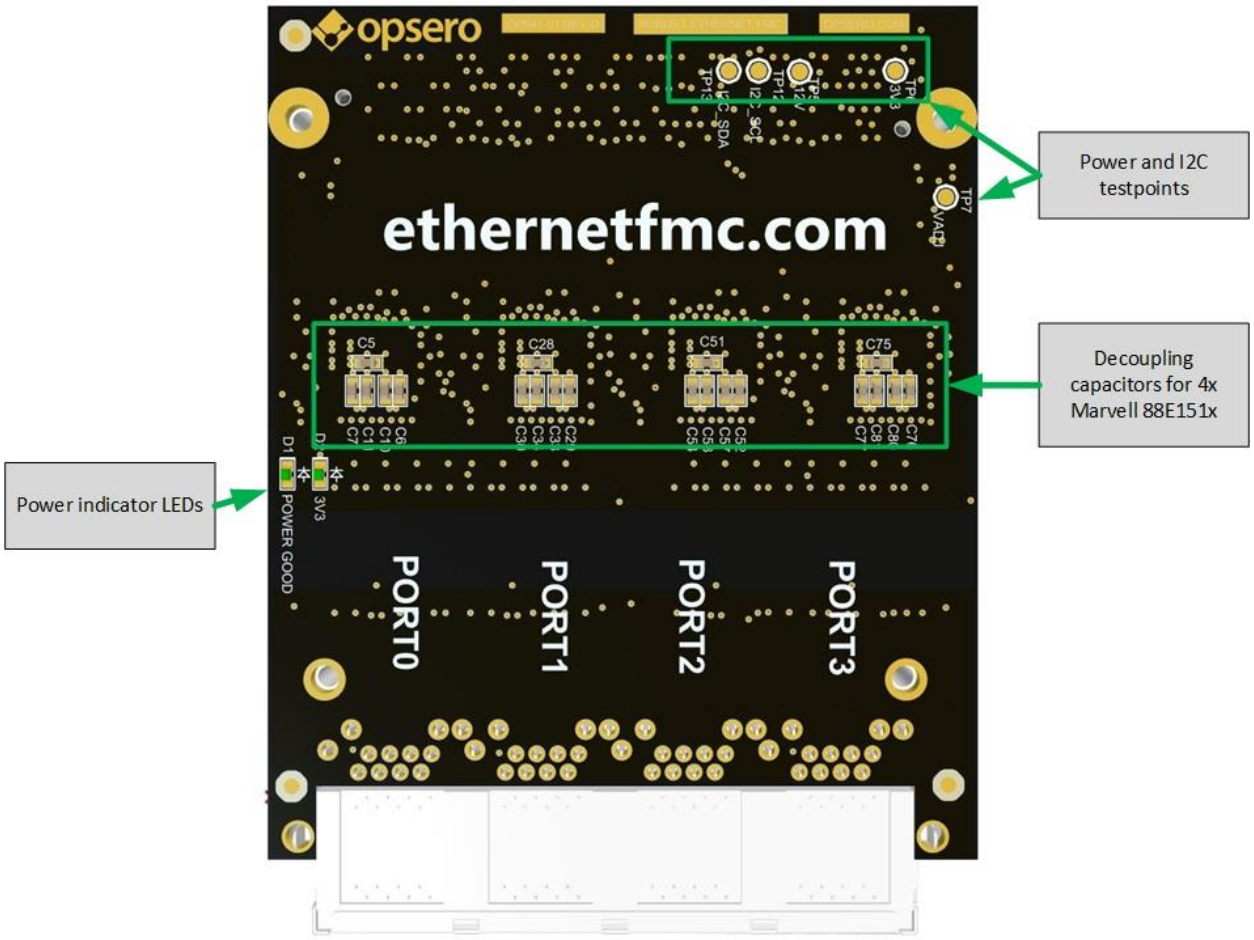
The figure below illustrates the various hardware components that are located on the top-side of the Robust Ethernet FMC.



The main components on the top-side of the mezzanine card are:

- 4x Marvell 88E151x Gigabit Ethernet PHYs
- Low Pin Count FMC Connector
- 2K EEPROM
- 125MHz MEMS Clock Oscillator
- 4x 25MHz crystals
- Ethernet transformers
- Quad-port RJ45 connector

The figure below illustrates the various hardware components that are located on the bottom-side of the mezzanine card.



The main components on the bottom-side of the mezzanine card are:

- Decoupling capacitors for the Marvell 88E151x Ethernet PHYs
- Power indicator LEDs
- Test points for power and I2C

Marvell 88E151x Gigabit Ethernet PHY

There are 4x Marvell 88E151x Gigabit Ethernet PHYs on the mezzanine card, one for each of the four Gigabit Ethernet ports. For interfacing with a MAC, the 88E151x has an RGMII (Reduced pin count GMII) interface. The 88E151x is designed for low-power and supports Synchronous Ethernet (SyncE) and Precise Timing Protocol (PTP) Time Stamping. For more specific information on the 88E151x, please refer to the Marvell 88E151x public datasheet .

Marvell has a more detailed datasheet that can be obtained by signing an NDA with them. To have an NDA setup, please contact your Marvell representative.

In this documentation, we will refer to the PHYs as PHY0, PHY1, PHY2 and PHY3, corresponding to their placement from right-to-left and as shown in Ethernet FMC top labelled image.

Precise Timing Protocol (PTP) Time Stamping Support

The Marvell 88E151x Gigabit Ethernet PHYs support Precise Timing Protocol (PTP). The feature allows time stamping of PTP frames with high precision. The supported time stamping frame formats are as defined in IEEE 802.1AS, IEEE 1588 version 1 and version 2.

The PTP feature can be used on the Ethernet FMC with the following limitations:

- **An external 125MHz clock cannot be used as the PTP reference clock source.** Required PTP control register setting: 20_6.8 = 0 (use internal 125MHz clock). An external PTP reference clock can be supplied to the CONFIG pin of the PHY, but the Ethernet FMC does not make this pin available to the FPGA. The PTP reference clock source must be set to use the internal 125MHz clock.
- **Capturing of external events via the PTP Event Request input pin is not supported.** Required PTP control register setting: 20_6.7 = 0. The PTP Event Request pin (LED1) allows the capture of external events and the recording of the time at which the event occurred, but the Ethernet FMC does not make this pin available to the FPGA, instead it is used to drive the right-side LED of the RJ45.
- **Generation of an external signal via the PTP Trigger Generate pin is not supported.** Required PTP control register setting: 20_6.6 = 0. The PTP Trigger Generate pin (LED1) allows the generation of an external signal when the internal Time of Day counter matches the value in a PHY register, but the Ethernet FMC does not make this pin available to the FPGA, instead it is used to drive the right-side LED of the RJ45.
- **Generation of an external interrupt via the LED2 pin is not supported.** The LED2 pin of the PHY can be used to generate an interrupt signal, but the Ethernet FMC does not make this pin available to the FPGA, instead it is used to drive the left-side LED of the RJ45.

Detailed information on using the PTP Time Stamping feature is contained in the complete datasheet of the 88E151x PHY that is only available through an NDA with Marvell.

RJ45 Connector

The table below lists the RJ45 connectors and Ethernet magnetics used on the Ethernet FMC and Robust Ethernet FMC.

	RJ45 P/N	Magnetics P/N
Ethernet FMC	JG0-0025NL	Integrated
Ethernet FMC	LPJG48851AFNL	Integrated
Robust Ethernet FMC	RJE72-488-1451	HX5020FNL

The differences between the Ethernet FMC and Robust Ethernet FMC all stem from the choice of RJ45 connector. The Ethernet FMC uses an RJ45 connector with integrated magnetics, whereas the Robust Ethernet FMC uses one without magnetics. Consequently, the Robust Ethernet FMC uses discrete Ethernet transformers that are separate from the RJ45 connector. The Robust Ethernet FMC was designed in this way to allow it's physical height profile to fit within that specified by the VITA 57.1 standard. For more information, see Mechanical information.

EEPROM

The 2K EEPROM stores IPMI FRU data that can be read by the carrier board and contains the following information:

- Manufacturer name (Opsero Electronic Design Inc.)
- Product name
- Product part number
- Serial number
- Power supply requirements

The FRU data is read by some carrier boards to determine the correct VADJ voltage to apply to the mezzanine card. All Opsero FMC products have their EEPROMs programmed with valid FRU data to allow these carrier boards to correctly power them.

Erasing or writing over the contents of the EEPROM can corrupt the IPMI FRU data making the mezzanine card unusable with carrier boards that require the information. We recommend that you do not use the mezzanine card's EEPROM for non-volatile storage but instead use the storage options provided by the carrier board. If you mistakenly erase or corrupt the contents of the EEPROM, you can reprogram it using the Opsero FMC EEPROM Tool. Read more about the FMC EEPROM tool in the User Guide.

Low Pin Count FMC Connector

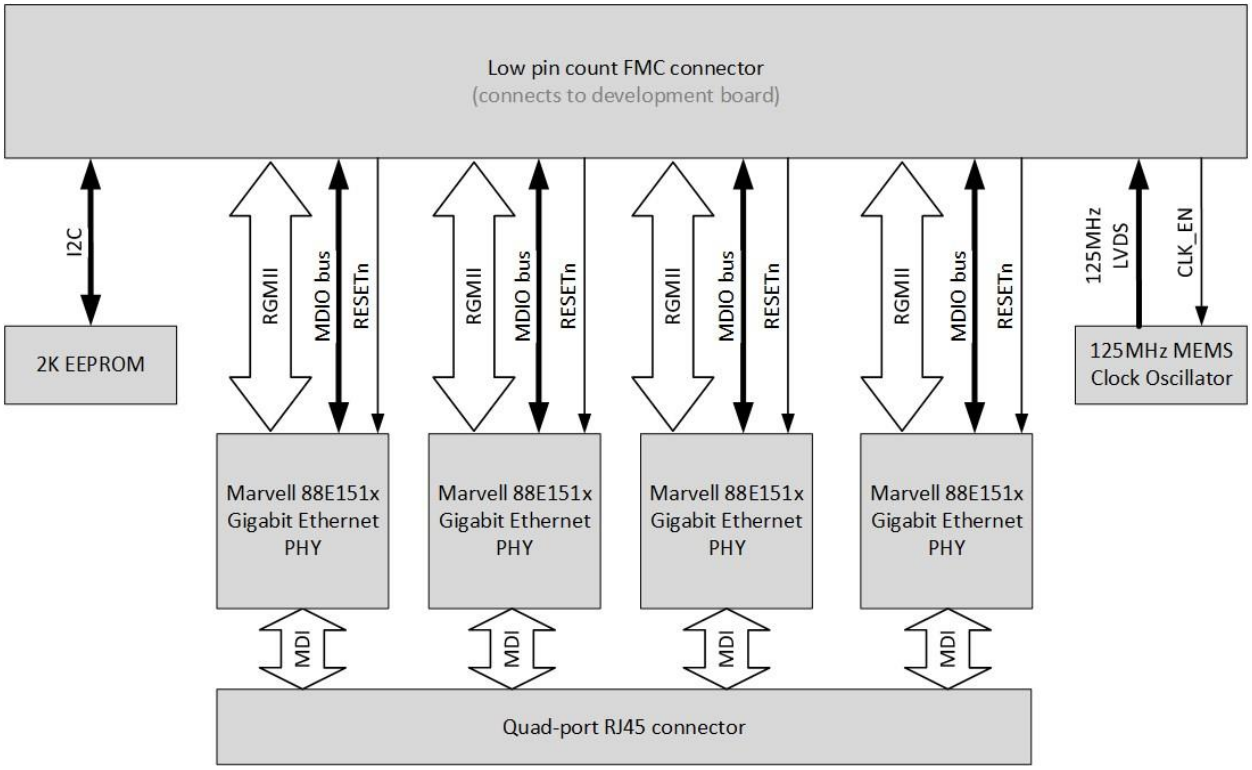
The Ethernet FMC has a low pin count FMC (FPGA Mezzanine Card) connector for interfacing with an FPGA or SoC development board. The part number of this connector is ASP-134604-01 datasheet . The pinout of this connector conforms to the VITA 57.1 FPGA Mezzanine Card Standard (for more information, see Pin configuration. For more information on the FMC connector and the VITA 57.1 standard, see the Samtec page on VITA 57.1 .

I/O Interfaces

The FMC connector provides power to the Ethernet FMC and also presents the following I/O signals to the FPGA fabric of the development board:

- RGMII for each of the 4x PHYs
- MDIO for each of the 4x PHYs
- I2C for EEPROM R/W access
- Clock enable for 125MHz oscillator
- 125MHz LVDS clock

The figure below illustrates the connections to the FMC connector.



RGMII

The 4x Reduced pin count GMII interfaces form the connection between the Ethernet PHYs and the MACs that are implemented in the FPGA or SoC on the development board. The RGMII interface is a DDR (double data rate) interface that is composed of the following 12 signals:

- Receive data (4 bits)
- Receive clock signal
- Receive control signal
- Transmit data (4 bits)
- Transmit clock signal
- Transmit control signal

MDIO

Each of the 4x MDIO interfaces consist of two signals:

- MDIO Clock signal (driven by the FPGA)
- MDIO Data signal (bidirectional)

The MDIO interface is used to configure the registers of the Ethernet PHYs. More information regarding the 88E151x registers can be found in the Marvell 88E151x public datasheet .

RESETn

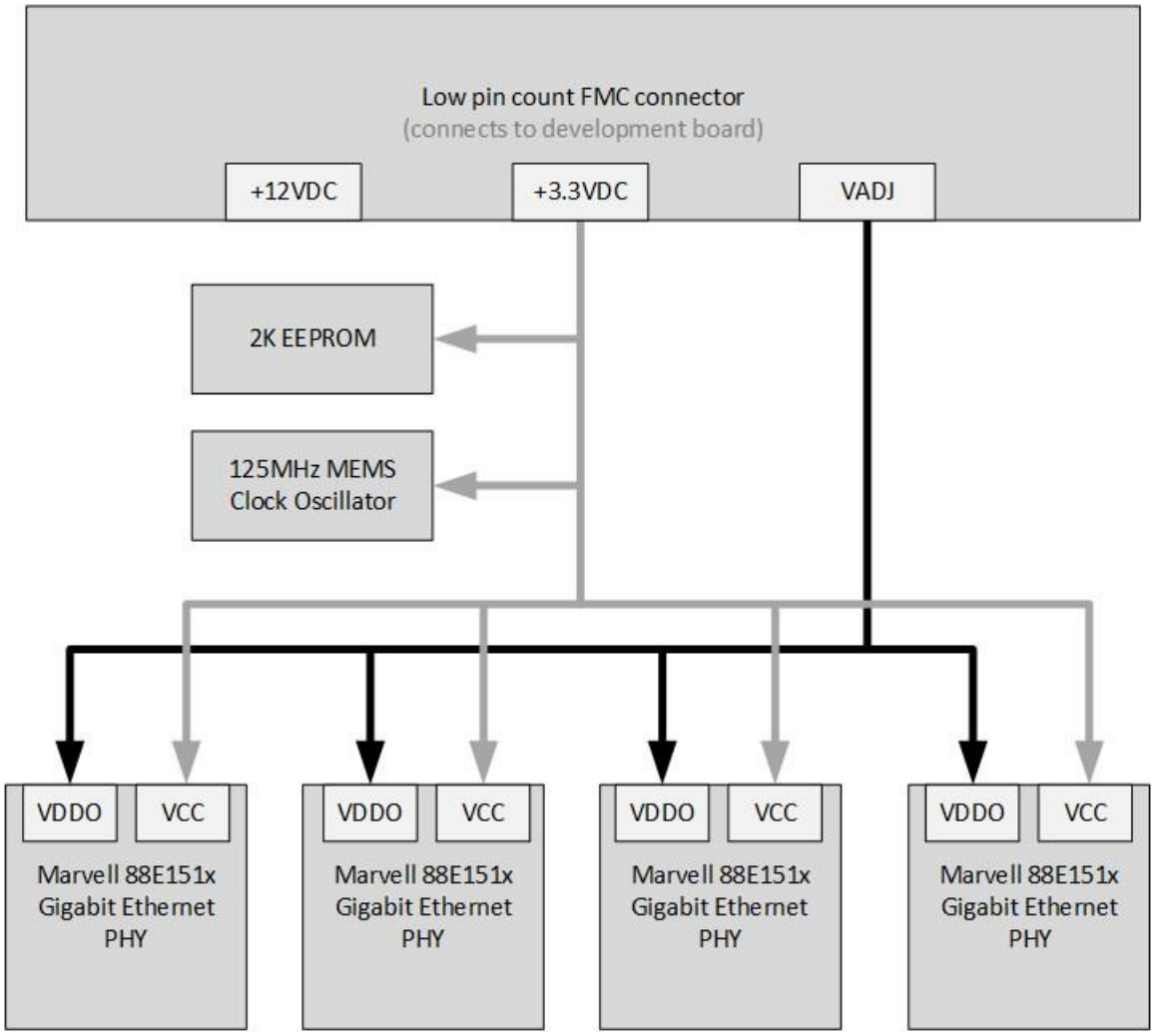
Each of the 4x Ethernet PHYs have an active-low reset input that must be driven by the FPGA.

Power Supplies

All power required by the Ethernet FMC is supplied by the development board through the FMC connector:

- +12VDC
- +3.3VDC
- VADJ: +2.5VDC or +1.8VDC

Note that although the FMC standard provides for a 12VDC supply, the Ethernet FMC does not use that supply nor does it draw current from that supply.
The VADJ voltage applied to the Ethernet FMC must match the version being used. To determine the appropriate VADJ voltage for your Ethernet FMC, refer to the serial number label - it should contain the numbering “1.8V” or “2.5V” next to the serial number.



3.3VDC Supply

The 3.3VDC supply is the main power supply for the 4x 88E151x Gigabit Ethernet PHYs and it also powers the EEPROM and 125MHz MEMS oscillator.

VADJ Supply

The Ethernet FMC is available in two versions: 1.8V and 2.5V, this corresponds to the VADJ voltage that is required by the board. The difference between the two versions is the part number of the Marvell Gigabit Ethernet PHY that is soldered onto the board. The 1.8V version is loaded with the 88E1518, while the 2.5V version is loaded with the 88E1510.

The VADJ supply is used as the I/O power supply of the 4x 88E151x Gigabit Ethernet PHYs, and this determines the voltage level that must be used by all I/O to and from the PHYs (RGMII, MDIO, RESET_N).

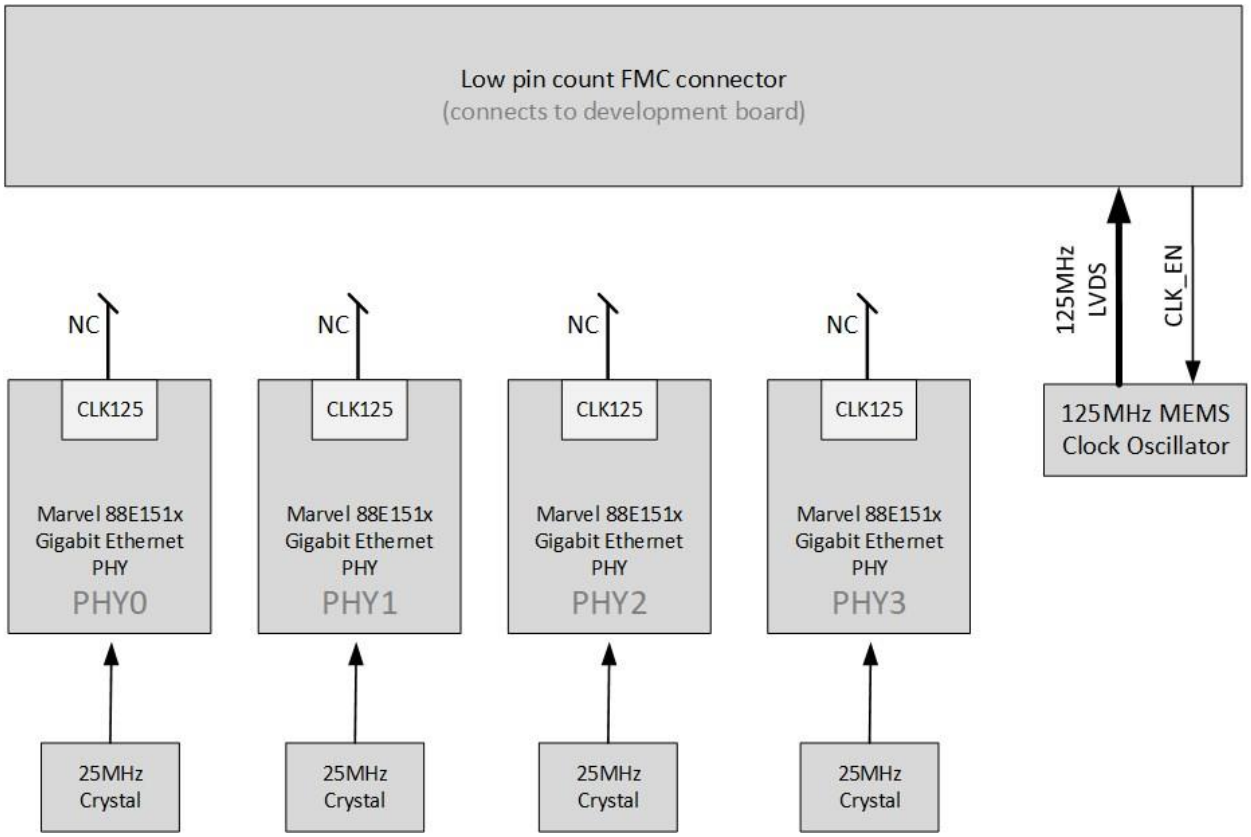
Power LEDs and testpoints

Two LEDs (labelled D1 and D2) on the Ethernet FMC are used to indicate when the required power supplies are active. LED D1 indicates the presence of the 3.3VDC supply and connects to the 3.3VDC power supply through a current limiting resistor. LED D2 indicates the presence of the VADJ power supply and connects to the POWER GOOD signal that is driven by the carrier board and is part of the Vita 57.1 FMC standard.

To aid hardware debug, there is a test point for each of the power supplies on the back side of the Ethernet FMC.

Clocks

The figure below illustrates the clock connections on the Ethernet FMC.



Each of the 4x 88E151x PHYs is connected to a 25MHz crystal for generation of it's own internal clocks. The Ethernet FMC also has a 125MHz MEMS clock oscillator with LVDS output to provide the FPGA fabric with a precision clock for driving the Ethernet MACs.

Each 88E151x PHY has a CLK125 pin that outputs a 125MHz clock that is synchronized with the 25MHz reference clock. Due to the limited number of pins on the LPC FMC connector, the CLK125 pins are left unconnected on the mezzanine card, hence these clocks are not available to the carrier board.

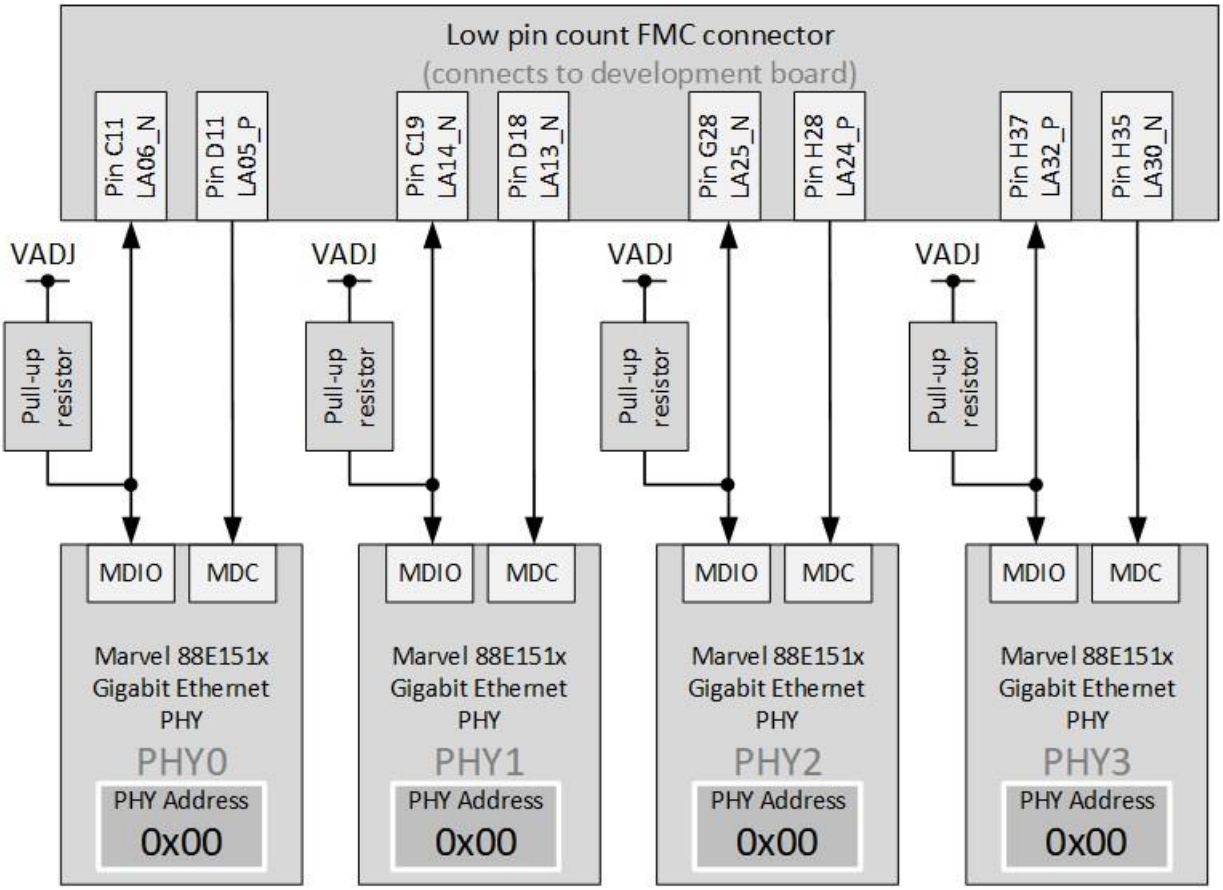
Resets

The 88E151x Ethernet PHYs each have a hardware reset pin (RESETn) that is routed separately to the FMC connector (see FMC Connector image for details). The reset pin must be driven by the development platform with an active-low signal. There are no pull-up resistors connected to the reset signals on the Ethernet FMC card, and we recommend always driving the reset pins from the development platform in order to ensure reliable reset behavior.

PHY Configuration

Configuration of the PHY by software is performed using the MDIO bus. The MDIO bus consists of two signals: a bidirectional data signal (MDIO) and a clock signal (MDC). The data signal (MDIO) is driven by the master and slaves as an open drain output, and it is connected to a pull-up resistor located on the mezzanine card. The clock signal (MDC) is driven by the master only (the FPGA on the development platform) and it does not require a pull-up resistor. For more information on the MDIO serial bus standard, please refer to the Wikipedia page on MDIO .

The MDIO bus of each PHY is routed independently to the FMC connector. The PHY address of all PHYs is 0 and the same for all ports (PHY0, PHY1, PHY2 and PHY3).



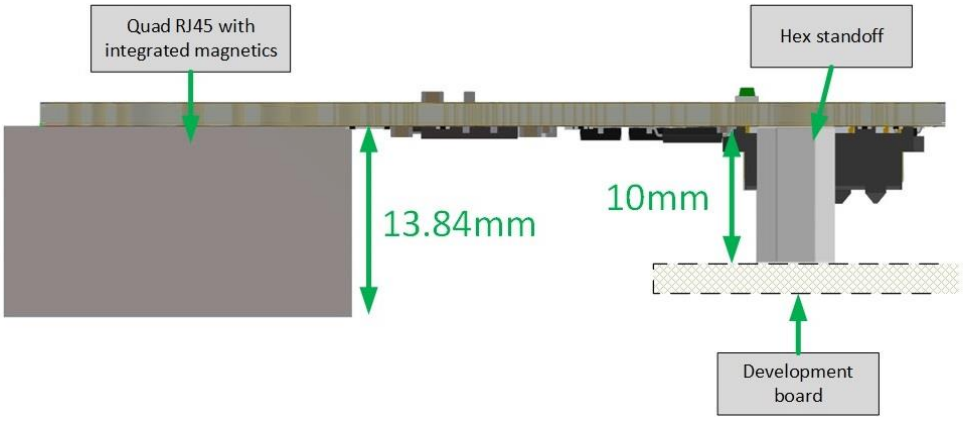
Mechanical Information

Height Profile

The height profile of the Ethernet FMC and Robust Ethernet FMC is the critical difference between the two models.

Ethernet FMC

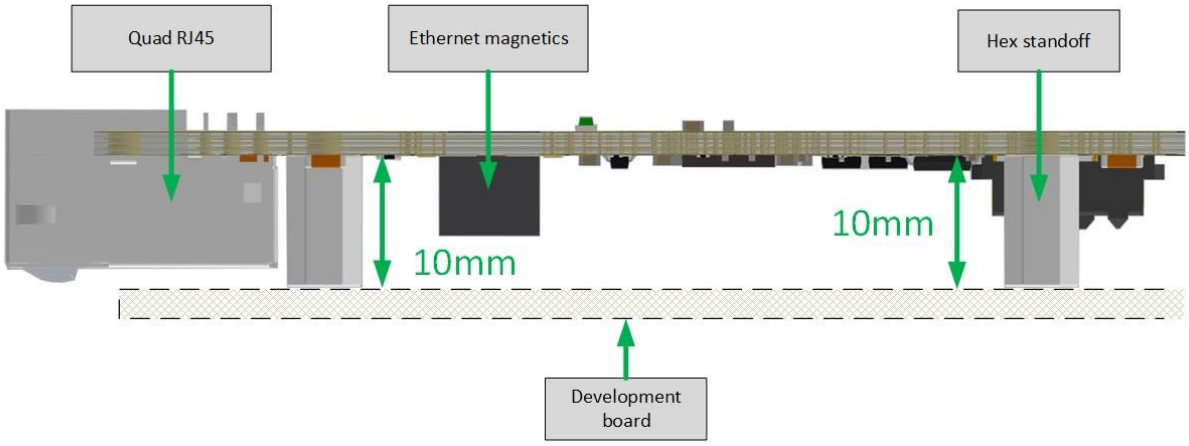
The figure below illustrates the height profile of the Ethernet FMC. Note that the quad RJ45 connector with integrated magnetics has a maximum height of 13.84mm; this limits the Ethernet FMC for mating **only** with FMC connectors that are located close to the edge of the carrier board. In other words, the Ethernet FMC must be able to extend over the edge of the carrier board to allow for clearance of the RJ45 connector. All of the Xilinx development boards provide this level of clearance and are designed with the FMC connectors in close proximity to the edge of the board.



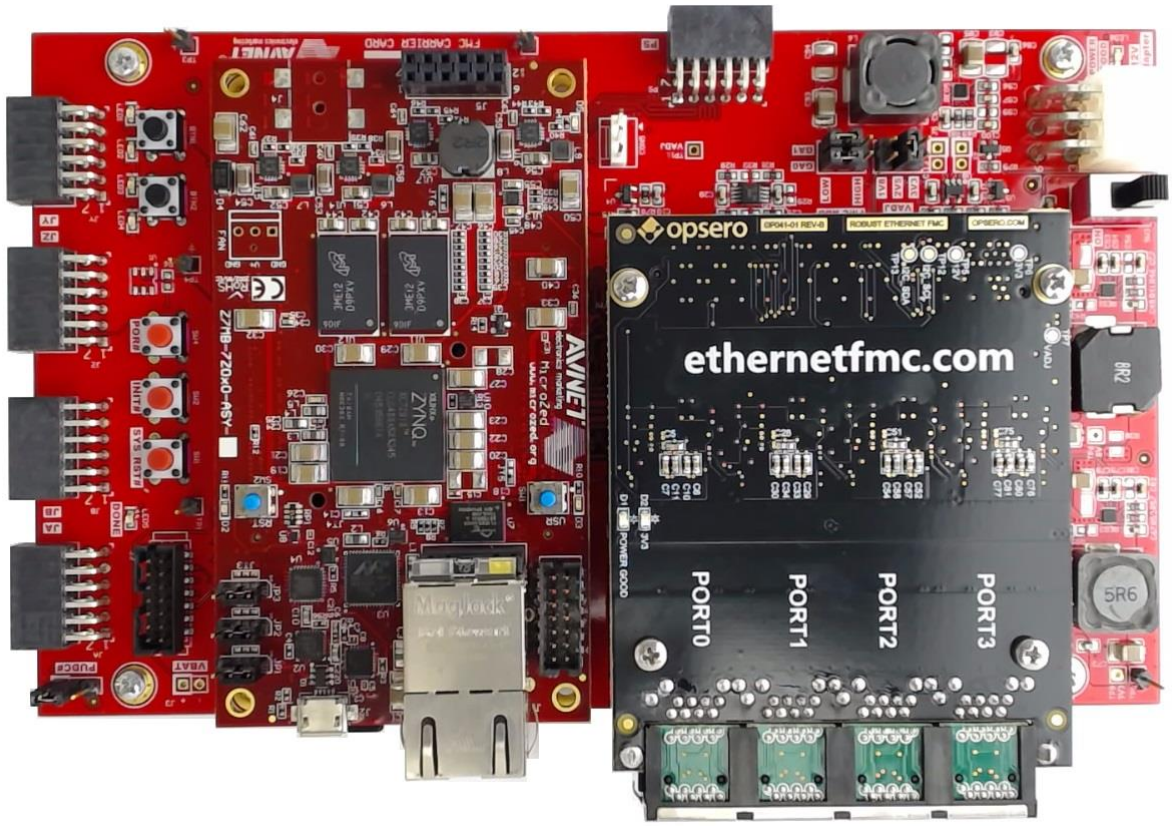
The figure below displays an example of a carrier board with an FMC connector that is located in close proximity to the board edge. The Ethernet FMC is limited to mating with this type of carrier board only.

Robust Ethernet FMC

The figure below illustrates the height profile of the Robust Ethernet FMC. All of the components on the Robust Ethernet FMC fit within the 10mm gap between the FMC card and the development board. It was designed this way to allow it to mate with all FMC carrier boards, including those that provide a dedicated area for fixing the FMC to the carrier by means of the 4 hex standoffs.



The figure below displays an example of a carrier board with a dedicated area for fixing the FMC. In this case, the FMC connector is **not** located close to the board edge and the FMC must have a height profile that fits within the 10mm gap. The Robust Ethernet FMC was designed for this type of carrier, but is not limited to this type.

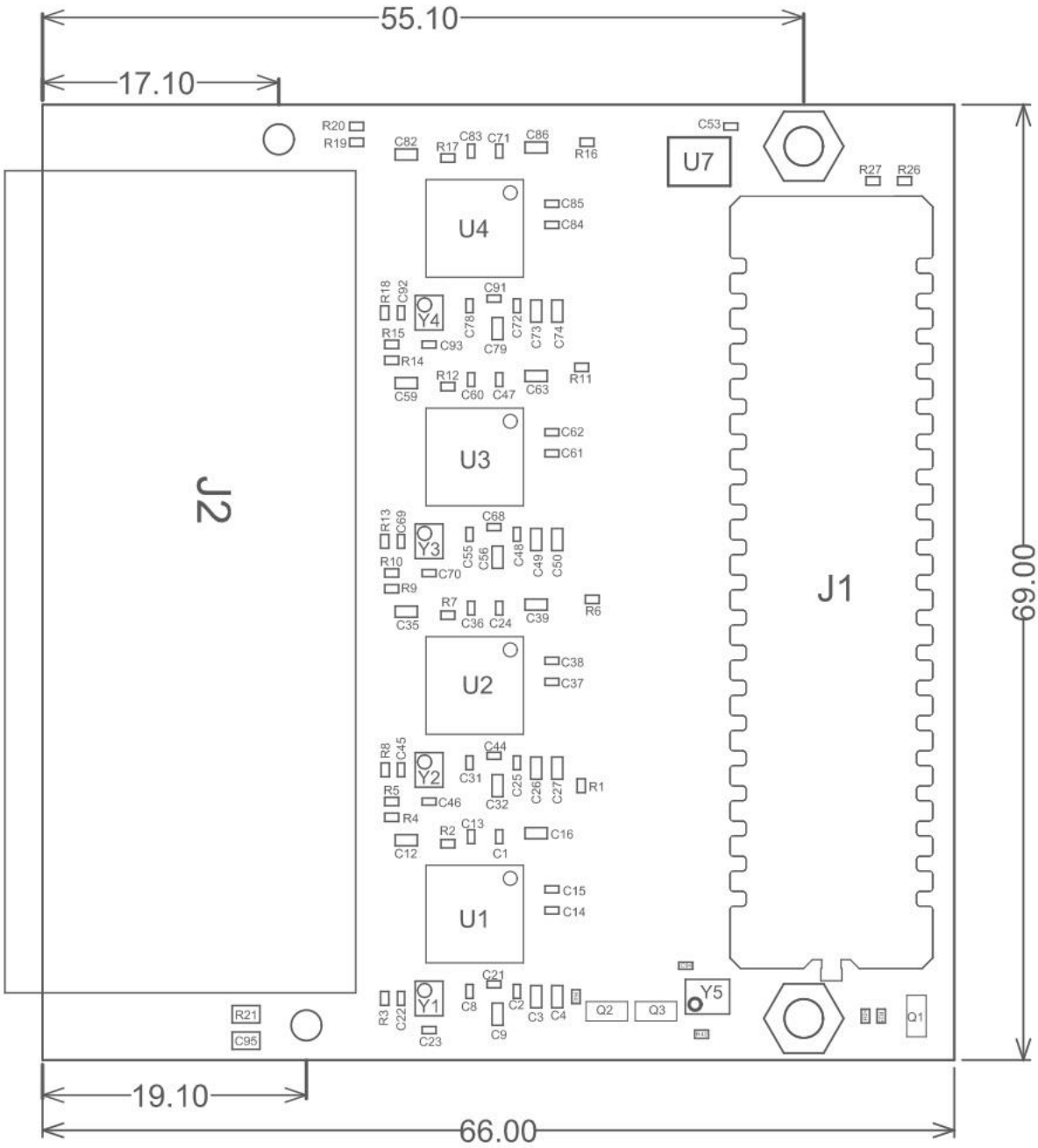


Dimensions

The mechanical dimensions of the Ethernet FMC and Robust Ethernet FMC are illustrated in the figures below. All dimensions are in millimeters (mm).

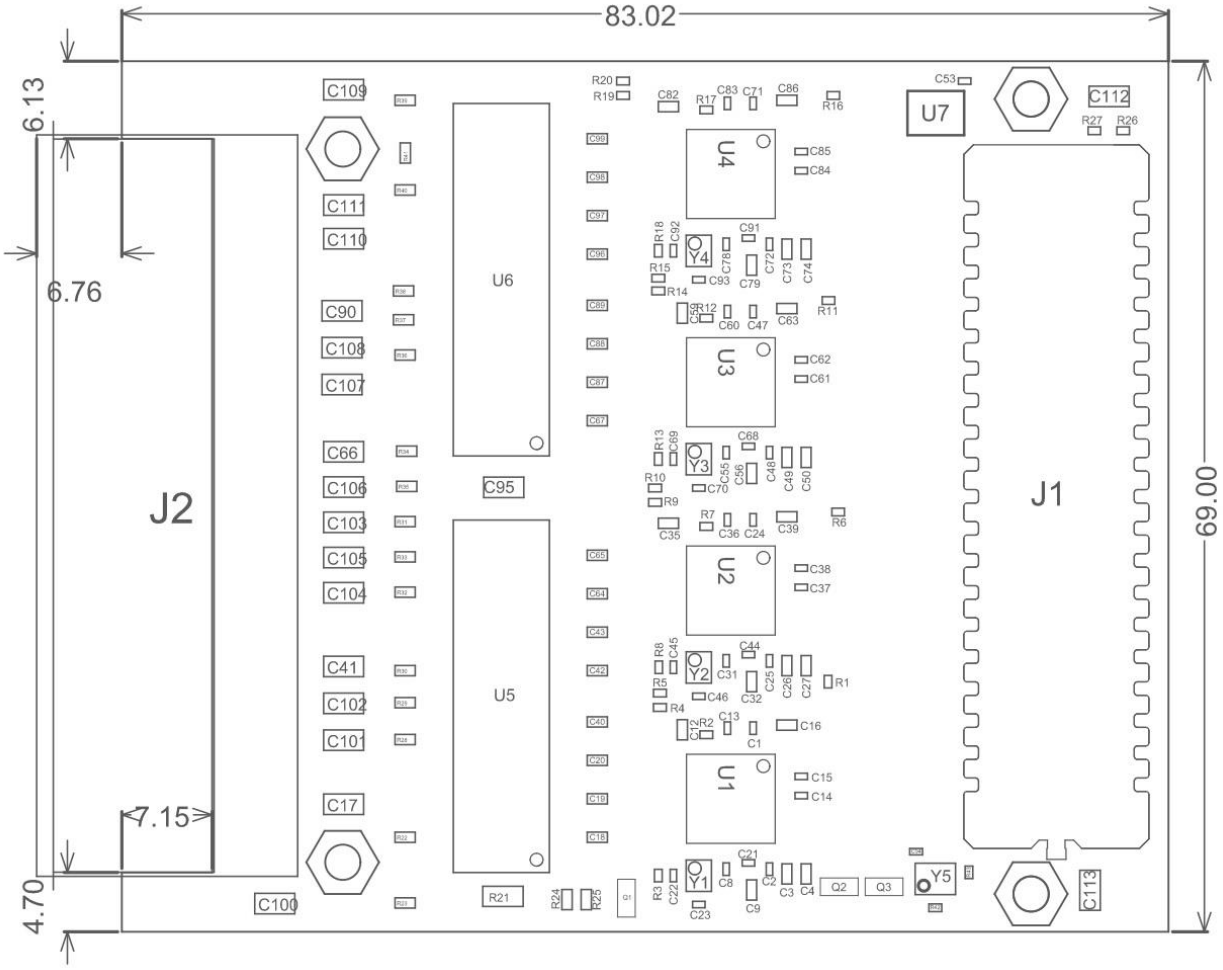
The assembly drawings are also available as PDF files that you can download at the provided links.

Ethernet FMC



- Ethernet FMC Rev-D Assembly Drawing
- Ethernet FMC Rev-E Assembly Drawing
- Ethernet FMC Rev-F Assembly Drawing

Robust Ethernet FMC



- Robust Ethernet FMC Rev-C Assembly Drawing
- Robust Ethernet FMC Rev-D Assembly Drawing

3D Model

The 3D model of the board is available as a STEP file at the links below:

Ethernet FMC

- Ethernet FMC Rev-D 3D STEP model
- Ethernet FMC Rev-E 3D STEP model
- Ethernet FMC Rev-F 3D STEP model

Robust Ethernet FMC

- Robust Ethernet FMC Rev-C 3D STEP model
- Robust Ethernet FMC Rev-D 3D STEP model

Ordering Information

Part number	Model	Voltage (VADJ)
OP031-1V8	Standard	1.8V
OP031-2V5	Standard	2.5V
OP041-1V8	Robust	1.8V
OP041-2V5	Robust	2.5V

Revision History

Date	Version	Description
2023-03-31	1.0	Initial PDF release.

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