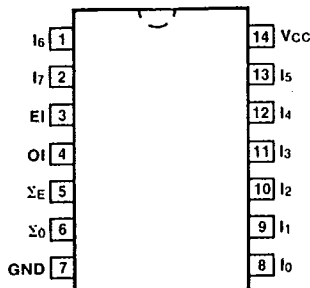


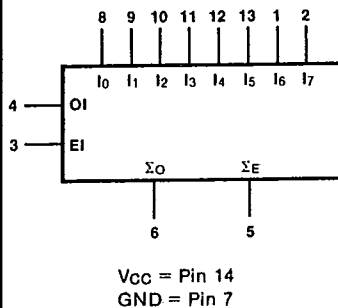
# 54/74180

## 8-BIT PARITY GENERATOR/CHECKER

### CONNECTION DIAGRAM PINOUT A



### LOGIC SYMBOL



**DESCRIPTION** — The '180 is a monolithic, 8-bit parity checker/generator which features control inputs and even/odd outputs to enhance operation in either odd or even parity applications. Cascading these circuits allows unlimited word length expansion. Typical application would be to generate and check parity on data being transmitted from one register to another. Typical power dissipation is 170 mW.

**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V, ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	74180PC		9A
Ceramic DIP (D)	A	74180DC	54180DM	6A
Flatpak (F)	A	74180FC	54180FM	3I

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
I <sub>0</sub> — I <sub>7</sub>	Data Inputs	1.0/1.0
OI	Odd Input	2.0/2.0
EI	Even Input	2.0/2.0
Σ <sub>O</sub>	Odd Parity Output	20/10
Σ <sub>E</sub>	Even Parity Output	20/10

### TRUTH TABLE

Σ OF 1's AT 0 THRU 7	INPUTS		OUTPUTS	
	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

