

# NP23N06YDG

## MOS FIELD EFFECT TRANSISTOR

R07DS0014EJ0100 Rev.1.00 Jul 01, 2010

### **Description**

The NP23N06YDG is N-channel MOS Field Effect Transistor designed for high current switching applications.

#### **Features**

- Low on-state resistance
  - $R_{DS(on)} = 27 \text{ m}\Omega$  MAX. ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 11.5 \text{ A}$ )
- Low Ciss: Ciss = 1200 pF TYP.  $(V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V})$
- Logic level drive type
- Designed for automotive application and AEC-Q101 qualified
- Small size package 8-pin HSON

### **Ordering Information**

Part No.	LEAD PLATING	PACKING	Package
NP23N06YDG -E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	8-pin HSON, Taping (E1 type)
NP23N06YDG -E2-AY *1			8-pin HSON, Taping (E2 type)

Note: \*1. Pb-free (This product does not contain Pb in the external electrode.)

## Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	60	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>C</sub> = 25°C)	I <sub>D(DC)</sub>	±23	A
Drain Current (pulse) *1	I <sub>D(pulse)</sub>	±46	A
Total Power Dissipation (T <sub>C</sub> = 25°C)	P <sub>T1</sub>	60	W
Total Power Dissipation (T <sub>A</sub> = 25°C) *2	P <sub>T2</sub>	1.0	W
Channel Temperature	T <sub>ch</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	-55 to +175	°C
Repetitive Avalanche Current *3	I <sub>AR</sub>	11	A
Repetitive Avalanche Energy *3	E <sub>AR</sub>	12	mJ

#### **Thermal Resistance**

Channel to Case Thermal Resistance  $R_{th(ch-C)}$  2.5 °C/W Channel to Ambient Thermal Resistance \*2  $R_{th(ch-A)}$  150 °C/W

Notes: \*1.  $T_C = 25^{\circ}C$ ,  $PW \le 10 \mu s$ , Duty Cycle  $\le 1\%$ 

\*2. Mounted on glass epoxy substrate of 40 mm x 40 mm x 0.8 mmt

\*3.  $T_{ch(peak)} \le 150^{\circ}C$ ,  $R_G = 25 \Omega$ 

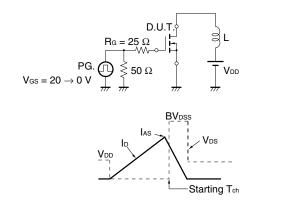
# Electrical Characteristics (T<sub>A</sub> = 25°C)

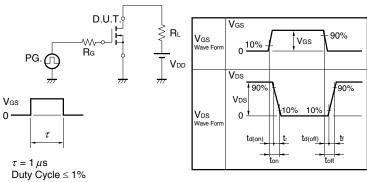
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			1	μA	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I <sub>GSS</sub>			±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	1.4	1.8	2.5	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$
Forward Transfer Admittance *1	y <sub>fs</sub>	9.0	18		S	$V_{DS} = 5 \text{ V}, I_{D} = 11.5 \text{ A}$
Drain to Source On-state	R <sub>DS(on)1</sub>		22	27	mΩ	$V_{GS} = 10 \text{ V}, I_D = 11.5 \text{ A}$
Resistance *1	R <sub>DS(on)2</sub>		24	37	mΩ	$V_{GS} = 5 \text{ V}, I_D = 11.5 \text{ A}$
Input Capacitance	C <sub>iss</sub>		1200	1800	pF	V <sub>DS</sub> = 25 V,
Output Capacitance	Coss		100	150	pF	$V_{GS} = 0 V$ ,
Reverse Transfer Capacitance	C <sub>rss</sub>		70	130	pF	f = 1 MHz
Turn-on Delay Time	t <sub>d(on)</sub>		12	24	ns	$V_{DD} = 30 \text{ V}, I_D = 11.5 \text{ A},$
Rise Time	t <sub>r</sub>		6	15	ns	$V_{GS} = 10 V$ ,
Turn-off Delay Time	t <sub>d(off)</sub>		36	72	ns	$R_G = 0 \Omega$
Fall Time	t <sub>f</sub>		4	10	ns	
Total Gate Charge	Q <sub>G</sub>		27	41	nC	V <sub>DD</sub> = 48 V,
Gate to Source Charge	Q <sub>GS</sub>		5		nC	$V_{GS} = 10 \text{ V},$
Gate to Drain Charge	$Q_{GD}$		8		nC	I <sub>D</sub> = 23 A
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>		0.9	1.5	V	I <sub>F</sub> = 23 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>		32		ns	I <sub>F</sub> = 23 A, V <sub>GS</sub> = 0 V,
Reverse Recovery Charge	Q <sub>rr</sub>		37		nC	di/dt = 100 A/μs

Note: \*1. Pulsed

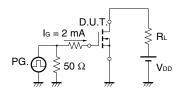
#### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

### TEST CIRCUIT 2 SWITCHING TIME



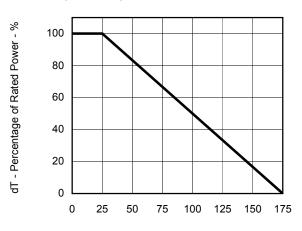


### **TEST CIRCUIT 3 GATE CHARGE**



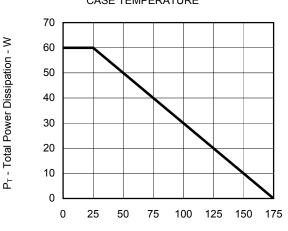
## Typical Characteristics ( $T_A = 25^{\circ}C$ )

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



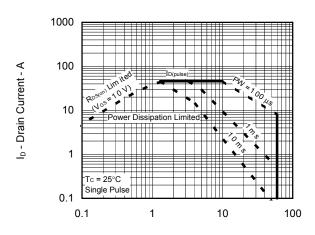
T<sub>C</sub> - Case Temperature - °C

# TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



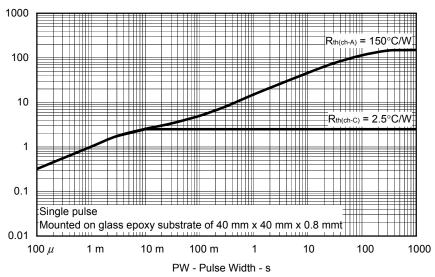
T<sub>C</sub> - Case Temperature - °C

#### FORWARD BIAS SAFE OPERATING AREA



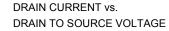
 $V_{\text{\scriptsize DS}}$  - Drain to Source Voltage - V

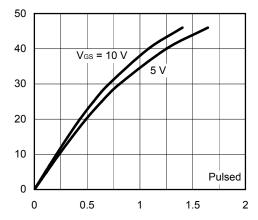
#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



I<sub>D</sub> - Drain Current - A

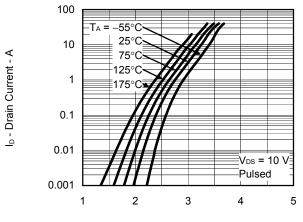
V<sub>GS(th)</sub> - Gate to Source Threshold Voltage - V





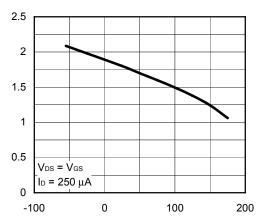
 $V_{\text{DS}}$  - Drain to Source Voltage - V

#### FORWARD TRANSFER CHARACTERISTICS

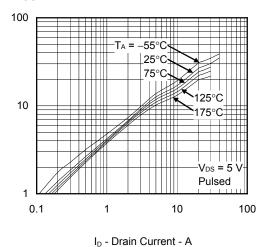


 $V_{\text{GS}}$  - Gate to Source Voltage - V

#### GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

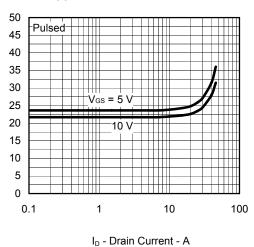


#### FORWARD TRANSFER ADMITTANCE vs. DRAIN **CURRENT**

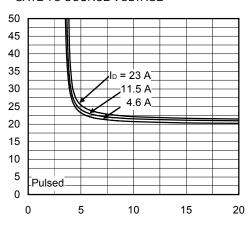


T<sub>ch</sub> - Channel Temperature - °C

#### DRAIN TO SOURCE ON-STATE RESISTANCE vs. **DRAIN CURRENT**



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



 $V_{\text{GS}}$  - Gate to Source Voltage - V

 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$  - Drain to Source On-state Resistance -  $m\Omega$ 

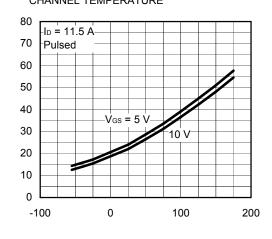
y<sub>fs</sub> | - Forward Transfer Admittance - S

 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$  - Drain to Source On-state Resistance -  $m\Omega$ 

t<sub>d(on)</sub>, t<sub>r</sub>, t<sub>d(off)</sub>, t<sub>f</sub> - Switching Time - ns

I<sub>F</sub> - Diode Forward Current - A

# DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



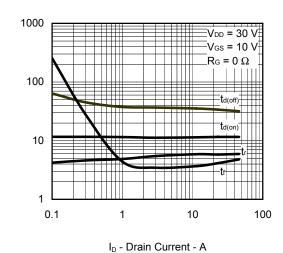
 $T_{\text{ch}}$  - Channel Temperature -  $^{\circ}C$ 

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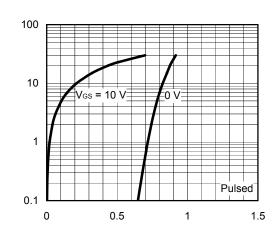
 $V_{\text{DS}}$  - Drain to Source Voltage - V

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

#### SWITCHING CHARACTERISTICS

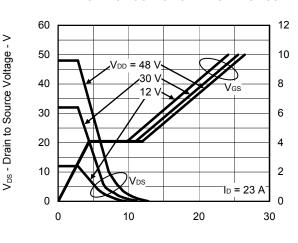


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



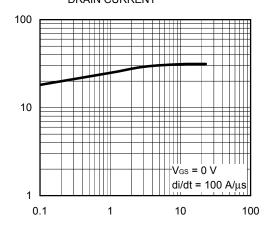
 $V_{F(S\text{-}D)}$  - Source to Drain Voltage - V

#### DYNAMIC INPUT/OUTPUT CHARACTERISTICS



Q<sub>G</sub> - Gate Charge - nC

# REVERSE RECOVERY TIME vs. DRAIN CURRENT

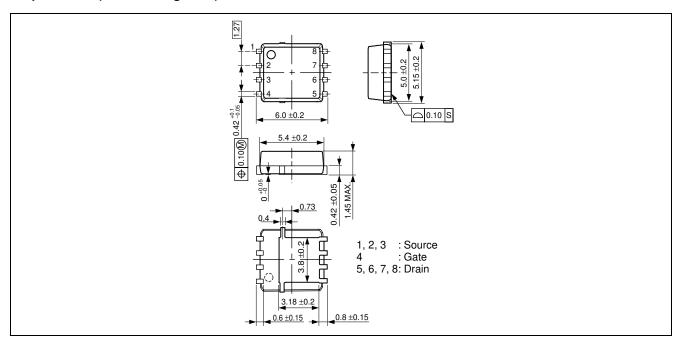


I<sub>F</sub> - Drain Current - A

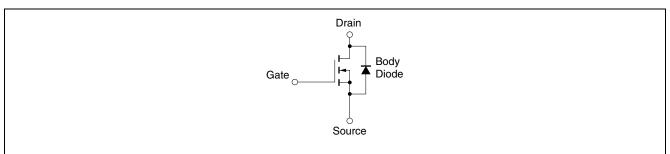
t<sub>rr</sub> - Reverse Recovery Time - ns

## Package Drawings (Unit: mm)

8-pin HSON (Mass: 0.13 g TYP.)



## **Equivalent Circuit**



**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History NP23N06YDG

		Description		
Rev.	Date	Page	Summary	
1.00	Jul 01, 2010	-	First Eddition Issued	

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