ML6510

Series Programmable Adaptive Clock Manager (PACMan™)

Features

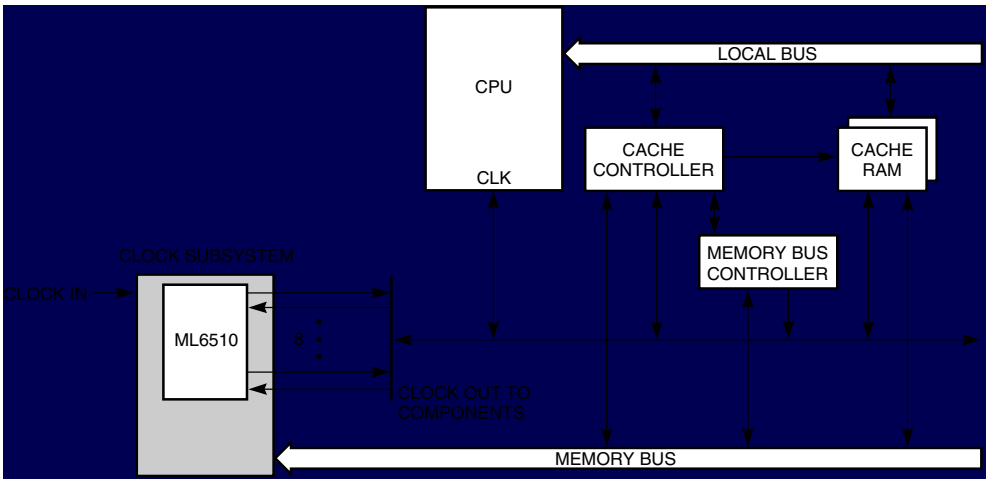
- Input clocks can be either TTL or PECL with low input to output clock phase error
- 8 independent, automatically deskewed clock outputs with up to 5ns of on-board deskew range (10ns round trip)
- Controlled edge rate TTL-compatible CMOS clock outputs capable of driving 40Ω PCB traces
- 10 to 80MHz (6510-80) input and output clock frequency range
- Less than 500ps skew between inputs **at the device loads**
- Small-swing reference clock outputs for minimizing part-to-part skew
- Frequency multiplication or division is possible using the M&N divider ratio
- Lock output indicates PLL and deskew buffer lock
- Test mode operation allows PLL and deskew buffer bypass for board debug
- Supports industry standard processors like Pentium,™ Mips, SPARC,™ PowerPC,™ Alpha,™ etc.

General Description

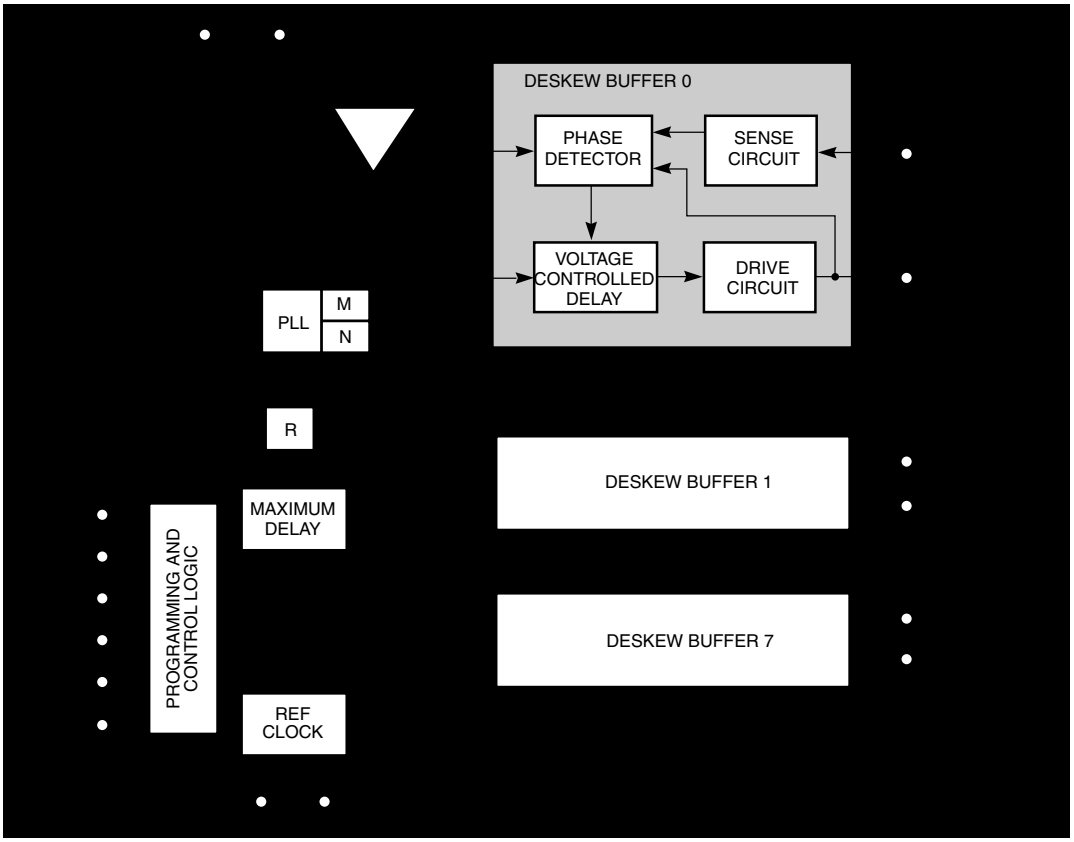
The ML6510 (Super PACMan™) is a Programmable Adaptive Clock Manager which offers an ideal solution for managing high speed synchronous clock distribution in next generation, high speed personal computer and workstation system designs. It provides eight channels of deskew buffers that adaptively compensate for clock skew using only a single trace. The input clock can be either TTL or PECL, selected by a bit in the control register. Frequency multiplication or division is possible using the M&N divider ratio, within the maximum frequency limit. 0.5X, 1X, 2X and 4X clocks can be easily realized.

The ML6510 is implemented using a low jitter PLL with on-chip loop filter. The ML6510 deskew buffers adaptively compensate for clock skew on PC boards. An internal skew sense circuit is used to sense the skew caused by the PCB trace and load delays. The sensing is done by detecting a reflection from the load and the skew is corrected adaptively via a unique phase control delay circuit to provide low load-to-load skew, at the end of the PCB traces. Additionally, the ML6510 supports PECL reference clock outputs for use in the generation of clock trees with minimal part-to-part skew. The chip configuration can be programmed to generate the desired output frequency using the internal ROM or an external serial EEPROM or a standard two-wire serial microprocessor interface.

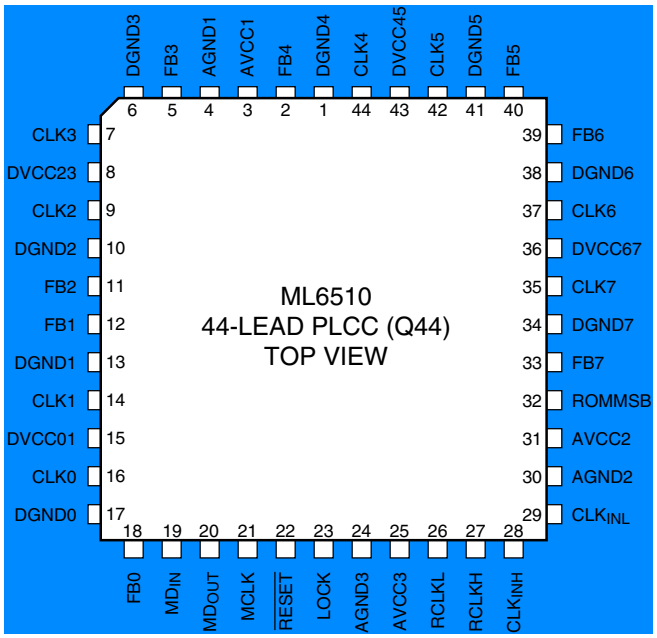
System Block Diagram



Block Diagram



Pin Assignments



Pin Definition

Pin Number	Name	Description
4, 30, 24	AGND[1–3]	Analog circuitry ground pins
3,31,25	AVCC[1–3]	Analog circuitry supply pins, separated from noisy digital supply pins to provide isolation. All supplies are nominally +5V.
16,14,9,7, 44, 42, 37, 35	CLK[0–7]	Clock outputs
28	CLK_{INH}	Input clock pins. For TTL clock reference use CLK_{INH} pin
29	CLK_{INL}	shorted to the CLK_{INL} pin. For PECL clock reference drive pins differentially. Input clock type is selected by the CS bit in the shift register.
17, 13, 10, 6, 1, 41, 38, 34	DGND[0–7]	Digital ground pins for CLK [0–7] output buffers. Each clock output buffer has its own ground pin to avoid crosstalk and ground bounce problems.
15	DVCC01	Digital supply pin for CLK0 and CLK1 output buffers. Nominally +5V.
8	DVCC23	Digital supply pin for CLK2 and CLK3 output buffers. Nominally +5V.
43	DVCC45	Digital supply pin for CLK4 and CLK5 output buffers. Nominally +5V.
36	DVCC67	Digital supply pin for CLK6 and CLK7 output buffers. Nominally +5V.
18,12,11,5, 2, 40, 39, 33	FB[0–7]	Clock feedback inputs for the deskew buffers
23	LOCK	Indicates when the PLL and deskew buffers have locked. Asserted polarity is high.
21	MCLK	Programming pin. See section on Programming the ML6510.
19	MD_{IN}	Programming pin. See section on Programming the ML6510.
20	MD_{OUT}	Programming pin. See section on Programming the ML6510.
27	RCLKH	part-to-part skew when building clock trees with other PACMan integrated circuits.
26	RCLKL	Differential reference clock output used to minimize
22	$\overline{\text{RESET}}$	Reset all internal circuits. Asserted polarity is low.
32	ROMMSB	MSB of the internal ROM address. Tie to GND if not used. See section on Programming the ML6510.

Absolute Maximum Ratings

Parameter	Min	Max	Units
VCC Supply Voltage Range	–0.3	6	V
Input Voltage Range	–0.3	VCC	V
Output Current			
CLK[0–7]		70	mA
All other outputs		10	mA
Junction Temperature		150	°C
Storage Temperature	–65	150	°C
Thermal Resistance (θ_{JA})		54	°C/W

Electrical Characteristics

The following specifications apply over the recommended operating conditions of DVCC = AVCC = 5V ± 5% and ambient temperature between 0°C and 70°C. Loading conditions are specified individually (Note 1)

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
Supply						
DVCCXX	Supply Current for each pair of clock outputs	f_{CLKX} = 0		50		µA
		C_L= 20pF, Z_O = 50Ω f_{OUT} = 80MHz		40	60	mA
IAVCC1	Static supply current, AVCC1 pin			100	120	mA
IAVCC2	Static supply current, AVCC2 pin			35	40	mA
IAVCC3	Static supply current, AVCC3 pin			1	2	mA
Low Frequency Inputs and Outputs (ROMMSB, MD_{OUT}, MD_{IN}, MCLK, $\overline{RESET}$, LOCK)						
V_{IH}	High level input voltage		DVCC – 0.5			V
V_{IL}	Low level input voltage				DGND + 0.5	V
V_{OH}	High level output voltage, MCLK and MDIN	I_{OH} = –100 µA	DVCC – 0.5			V
V_{OL}	Low level output voltage, MCLK and MDIN	I_{OL} = +200 µA			DGND + 0.5	V
V_{OH}	High level output voltage, LOCK output	I_{OH} = –100 µA I_{OH} = –10 µA	2.4 DVCC – 0.5			V V
V_{OL}	Low level output voltage, LOCK output	I_{OL} = +1 mA			0.4	V
I_{IN}	Static input current				10	µA
C_{IN}	Input capacitance			5		pF
High Frequency Inputs and Outputs (CLK_{INH}, CLK_{INL}, FB[0-7], CLK[0-7])						
V_{IH}	High level input voltage	CS = 0 (TTL Input Clock)	2.0			V
		CS = 1 (PECL Input Clock)	AVCC – 1.165		AVCC – 0.88	V
V_{IL}	Low level input voltage	CS = 0 (TTL Input Clock)			0.8	V
		CS = 1 (PECL Input Clock)	AVCC – 1.810		AVCC – 1.475	V
V_{ICM}	Common mode input voltage range for PECL reference clocks	CS = 1 (PECL Input Clock)	2.0		AVCC – 0.4	V
I_{IH}	High level input current	V_{IH} = 2.4V			100	µA
I_{IL}	Low level input current	V_{IL} = 0.4V	–400			µA
V_{OH}	High level output voltage	I_{OH} = –60mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = +60mA			0.4	V

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
AC Characteristics rise time, fall time and duty cycle are measured for a generic load; (see Load Conditions section).						
t_R	Rise time, LOAD [0-7] output	0.8 Ø 2.0V, 80MHz	150		1500	ps
t_F	Fall time, LOAD [0-7] output	2.0 Ø 0.8V, 80MHz	150		1500	ps
f_{IN}	Input frequency, CLK_{IN} pin		10		80	MHz
f_{OUT}	Output frequency , CLK [0-7] output	ML6510-80	10		80	MHz
f_{VCO}	PLL VCO operating frequency		80		160	MHz
DC	Output duty cycle	Measured at device load, at 1.5V	40		60	%
t_{JITTER}	Output jitter	Cycle-to-cycle		75		ps
		Peak-to-peak		150		ps
t_{LOCK}	PLL and deskew lock time	After programming is complete		11		ms
Skew Characteristics All skew measurements are made at the load, at 1.5V threshold each output load can vary independently within the specified range for a generic load (see Load Conditions section).						
t_{SKEWR}	Output to output rising edge skew, all clocks				500	ps
t_{SKEWF}	Output to output falling edge skew	Output clock frequency ≥ 50MHz			1.5	ns
t_{SKEWIO}	CLK_{IN} input to any LOAD [0-7] output rising edge skew	N = M = 0 N ≥ 2, M ≥ 2		600 1.25		ps ns
t_{RANGE}	Round trip delay CLKX to FBX pin; output CLK period = t_{CLK}	Output frequency < 50MHz Output frequency ≥ 50MHz	0 0		10 $t_{CLK}/2$	ns
t_{SKEWB}	Output-to-output rising edge skew, between matched loads	Providing first (see LOAD conditions) order matching order matching between outputs		250		ps
Part-To-Part Skew Characteristics Skew measured at the loads, at 1.5V threshold. Reference clock output pins drive clock input pins of another ML6510.						
t_{PP1}	Total load-to-load skew between multiple chips interfaced with reference clock pins.	Slave chip CS = 1, CM = 1 and N = 0, M = 0; RCLK outputs to CLK_{IN} inputs distance less than 2"			1	ns
t_{PP2}	Total load-to-load skew between multiple chips interfaced with reference clock pins.	Slave chip CS = 1, CM = 1 and N ≥ 2, M ≥ 2; RCLK outputs to CLK_{IN} inputs distance less than 2"			1	ns

Electrical Characteristics (Continued)

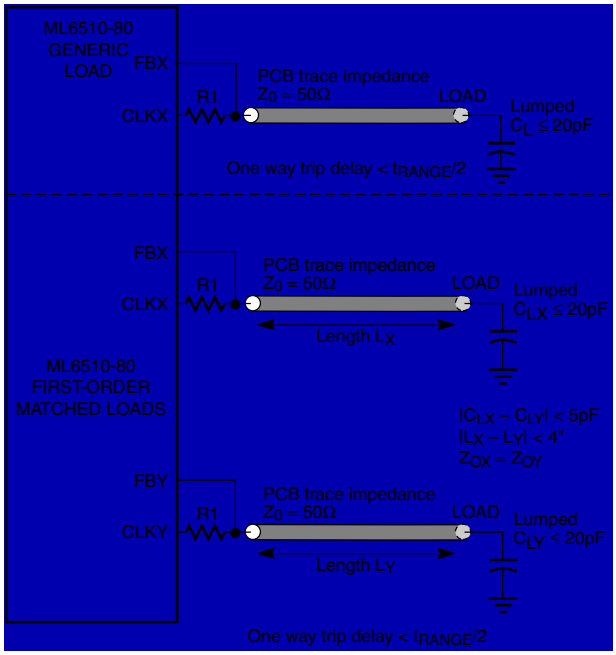
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Programming Timing Characteristics						
t$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ assertion pulse width		50			ns
t_{A1}	AUX mode MCLK high time		2000			ns
t_{A2}	AUX mode MCLK low time		2000			ns
t_{A3}	AUX mode MD_{OUT} data hold time		10			ns
t_{A4}	AUX mode MD_{OUT} data setup time		10			ns
t_{A5}	AUX mode MCLK period		5000			ns
t_{M1}	MAIN mode MCLK high time		900			ns
t_{M2}	MAIN mode MCLK low time		900			ns
t_{M3}	MAIN mode MCLK period		1800			ns
t_{M4}	MAIN mode MCLK to MD_{OUT} valid (EEPROM read time)				900	ns

Note 1:Limits are guaranteed by 100% testing, sampling or correlation with worst case test conditions.

ML6510 configured with bit CM = 0:

Note: All skew is measured at the device load input pin, NOT at the ML6510 clock output pin. Skew is always positive number, regardless of which edge is leading and which is trailing.

AC/Skew Characteristics Load Conditions



Functional Description

Micro Linear's ML6510 is the first clock chip to use a feedback mechanism to adaptively (on a real time basis), eliminate clock skew in high speed personal computer and workstation system designs. Figure 1 shows a basic configuration of the ML6510 in a system. The skew problem results due to the delaying of clock signals in the system, as shown in Figure 2. Clock skew results from variation in factors like trace length, PCB trace characteristics, load capacitance, parasitic capacitance, temperature and supply variations, etc. Figure 2 shows a representation of the clock skew problem from a timing perspective. It shows a worst case example where the clock signal is delayed so much that its rising edge completely misses the data it is intended to strobe.

Using a clock deskew mechanism, this problem can be eliminated and the strobe with the appropriate setup and hold times with respect to the data bus can be generated.

The ML6510 has eight deskew buffers, each with its own independent the reflection and error correction circuit. The deskew buffer eliminates skew by using the reflection from a remote chip to measure the clock error and then corrects it by generating the appropriate skew to the clock output to compensate.

Eight individually deskewed copies of the clock are provided by the ML6510.

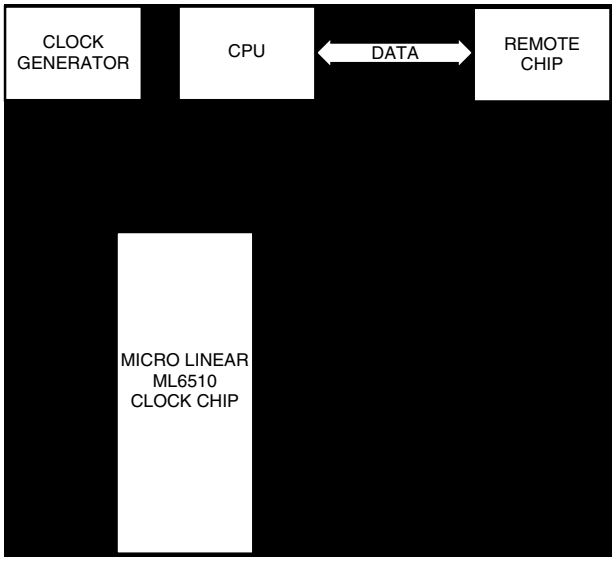


Figure 1. Basic System Configuration Using the ML6510

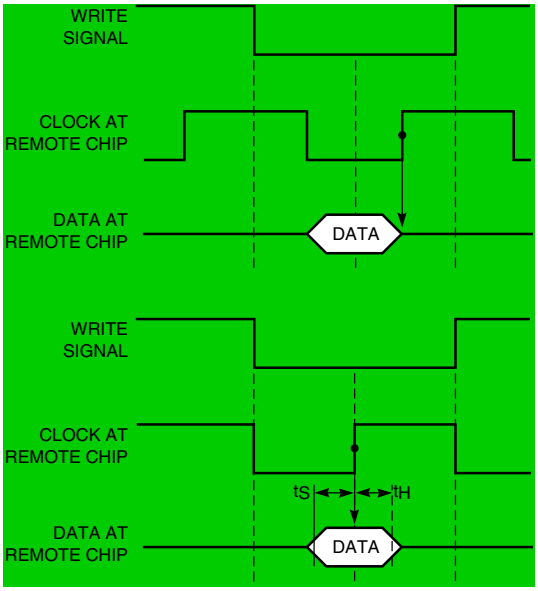


Figure 2. The Skew Problem

The deskew buffers compensate internally for board-level skew caused by the PCB trace length variations and device load variations. This is accomplished by sensing the round trip delay via a reflected signal, and then delaying or advancing the clock edge so that all 8 output clocks arrive at their loads in phase. Each of the eight clock lines can have any length PCB trace (up to 5ns each way or 1/4th of the output clock period, whichever is smaller) and the device loads can vary from line to line. The ML6510 will automatically compensate for these variations, keeping the device load clocks in phase. Although ML6510 will compensate for skew caused by loading, excessive capacitive loading can cause rise/fall time degradation at the load. Cascading one ML6510 to another ML6510 should be done using the PECL reference clock outputs, to minimize part-to-part skew.

Clock Regeneration

The programmable adaptive clock deskew can function in a clock regeneration mode to assist in building clock trees or to expand the number of deskewed clock lines. In this mode, it has the ability to do clock multiplication or division as well, while maintaining low skew between input clock and output clocks. It can thus generate a 2x or 4x or 0.5x frequency multiplication or division from input to output (e.g. 33 MHz input, 66 MHz output or 66 MHz input, 33 MHz output, etc.). It also can generate a 1x frequency output. The VCO frequency is defined by:

Figure 3. ML6510 Clock Generation Block Diagram.

and the output frequency is still given by:

$$f_{OUT} = f_{VCO}/2^R$$

R1	R0	INPUT/OUTPUT RANGE
0	0	80-130 MHz
0	1	40–80 MHz
1	0	20–40 MHz
1	1	10–20 MHz

Note: R implies R1, R0; for -80 version, Not valid: Defaults to R = 01

The VCO still must remain in the range 80–160 MHz, and the minimum phase detector input frequency is 625kHz = (80 MHz/128). Thus the product of (N + 1) and 2_R should be limited to 128:

$(N + 1) \times 2^R \leq 128$ to make sure that the phase detector inputs remain above the minimum frequency.

Example: Generating a 2x clock input frequency = 33 MHz

Set R = 01 (output range 40 – 80 MHz), N = 5 (0000101), M = 2 (000010), M/S = 0

$$f_{OUT} = f_{VCO}/2^R = 132\ MHz/2^1 = 66\ MHz$$

Example: Generating a 1x clock Input frequency = 66 MHz

Set R = 01 (output range 40–80 MHz), set M = 0 (000000), N = 0 (0000000), M/S = 0

$$f_{OUT} = f_{VCO}/2^R = 132\ MHz/2^1 = 66\ MHz$$

For doing frequency multiplication and division, keep M ≥ 2 and N ≥ 2 for the lowest skew between input clock and output clock. Several configurations for doing frequency multiplication and division are included in the 8 configurations stored in the on-chip ROM (see PROGRAMMING the ML6510).

Adaptive Deskew buffers

Each copy of the clock is driven by an adaptive deskew buffer. The deskew buffer compensates for skew time automatically in accordance to the flight time delay it senses from the reflection on the transmission line.

Figure 4 shows the simplified functional block diagram of the deskew circuit. The phase of the sense signal and the driver signal is presented to a three-input phase comparator and compared with the reference signal. The phase comparator then controls the voltage controlled delay in the output drive line to match the delay of the fixed reference delay line. Therefore, the sum of the delay of the driver circuit, PCB trace delay, rise time delay at the load and the adjustable delay will always equal the fixed maximum delay.

The sense circuit has an internal level detect such that any skew caused by loading is also accounted for. Since the delay of the circuit is matched for the entire loop, the phase of all the drivers are in close alignment at the inputs of the load.

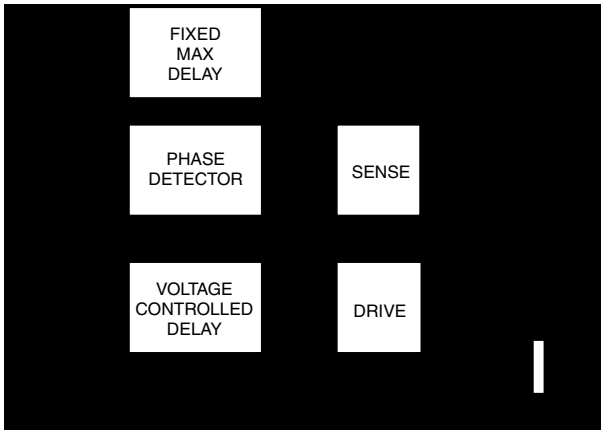


Figure 4. Deskew Circuit Block Diagram.

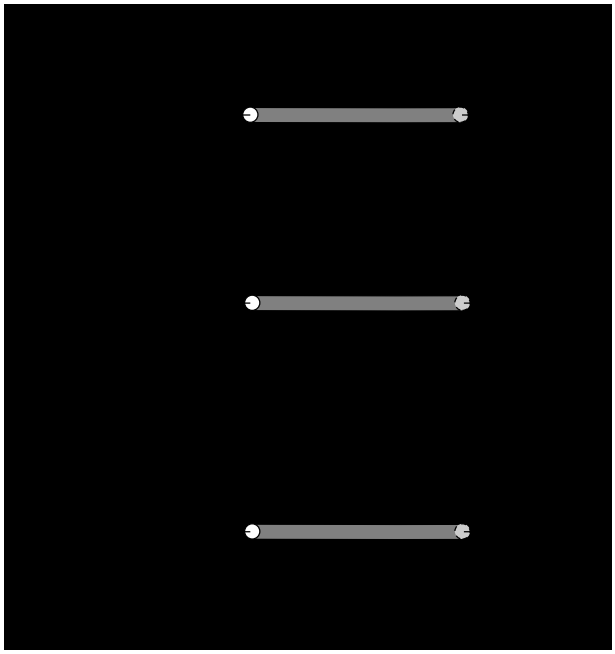
Load Conditions

The ML6510 has been designed to drive the wide range of load conditions that are encountered in a high frequency system. The eight output clock loads can each vary within a range of trace length and lumped capacitive load, and the ML6510 will maintain the low skew characteristics specified in Electrical Characteristics. The clock skew can be further minimized by providing some first-order matching between any two loads that require particularly well-matched clocks.

The ML6510-80 produces a 5V swing at the load and requires a single external termination resistor for each output. The FB input pin is connected to the other side of the termination resistor R1 or R2, with a short connection. Termination resistor valves should be chosen as follows:

$$R1 = Z_0 \quad R2 = 1.5 \times Z_0 \quad R3 = 3 \times Z_0$$

Trace Impedance	RESISTOR Values		
Z0	**R1**	**R2**	**R3**
40Ω	40	60	120
50Ω	50	75	150
63Ω	63	95	189



External Input clocks

The external input clock to the ML6510 can be either a differential Pseudo-ECL clock or a single-ended TTL clock. This is selected using the CS bit in the serial shift register. For the single-ended TTL clock tie the CLK_{INH} and CLK_{INL} pins together. The ML6510 ensures that there is a well-defined phase difference between the input and output clocks.

$\overline{\text{RESET}}$ and Lock

When $\overline{\text{RESET}}$ is de-asserted, the internal programming logic will become active, loading in the configuration bits (see Programming the ML6510). Once the configuration is loaded, the PLL will lock onto the reference signal, and then the deskew blocks will adapt to the load conditions. When all eight output clocks are stable and deskewed, LOCK will be asserted. The asserted polarity of lock is high. Thus, LOCK can be used to indicate that the system is ready, or it can be used to drive the $\overline{\text{RESET}}$ input of another PACMan in a clock tree.

$\overline{\text{RESET}}$ may be reasserted at any time to reset the chip operations. Following a $\overline{\text{RESET}}$ assertion of valid pulse width (see Programming Electrical Characteristics), the ML6510 must again be loaded with a configuration, then it will re-lock and reassert lock when all eight clock outputs are stable and deskewed.

Programming the ML6510

The configuration of the ML6510 is programmed by loading 18 (ML6510-80) into the configuration shift register. To load these bits, the user has 3 options: MAIN, AUX or ROM modes. Which mode is used is determined by the logic level on the MD_{IN} pin when $\overline{RESET}$ is deasserted. If MD_{IN} is tied high, the ML6510 will assume AUX mode; if its tied low, ROM mode. If MD_{IN} is high-impedance (i.e. tied to the input of an EEPROM), it will assume MAIN mode.

1. MAIN Mode

In this mode, the ML6510 will read the configuration bits from an external serial EEPROM, such as the 93C46, using the industry standard 3-wire serial I/O protocol. The serial EEPROM should be a 1K organized in 64 x 16 bits and the PACMan will read the configuration bits out of the two least significant 16-bit words. To use this mode, simply connect the EEPROM serial data input pin to MD_{IN} (ML6510 pin 19), the EEPROM serial data output pin to MD_{OUT} (ML6510 pin 20), and the EEPROM serial data clock pin to MCLK (ML6510 pin 21) and CS pin for the EEPROM should be tied to the $\overline{RESET}$ signal. After power up, when $\overline{RESET}$ is deasserted, the ML6510 will automatically generate the address and clock to read out the configuration bits. Refer MAIN Mode waveform in Figure 5.

MAIN Mode Configuration.

2. AUX Mode

When MD_{IN} is tied to VCC, programming the ML6510 will occur via the AUX Mode. This mode shifts the configuration bits into the shift register directly from the MD_{OUT} pin. The first 18 (ML6510-80) clock rising edges provided externally on the MCLK pin after $\overline{RESET}$ is deasserted will be used to load the shift register data, which should be provided on the MD_{OUT} pin. See figure 6.

AUX Mode Configuration.

3. ROM Mode

When MD_{IN} is tied to GND, programming the ML6510 will occur via the ROM Mode. This mode reads the configuration bits directly from an on chip ROM. The selection of one of the eight preset configuration codes is accomplished by means of the pins ROMMSB, MCLK and MD_{OUT} as shown in Tables 1 and 2. The TEST mode configuration (code 7) is enabled when the TEST bit is set. In this mode the PLL is bypassed for low frequency testing. Codes 0-2 are used when the ML6510 clock inputs are driven from another PACMan's reference clock outputs. Code 3 is used when zero phase error is desired between input and load clocks.

ROM Mode Configuration.

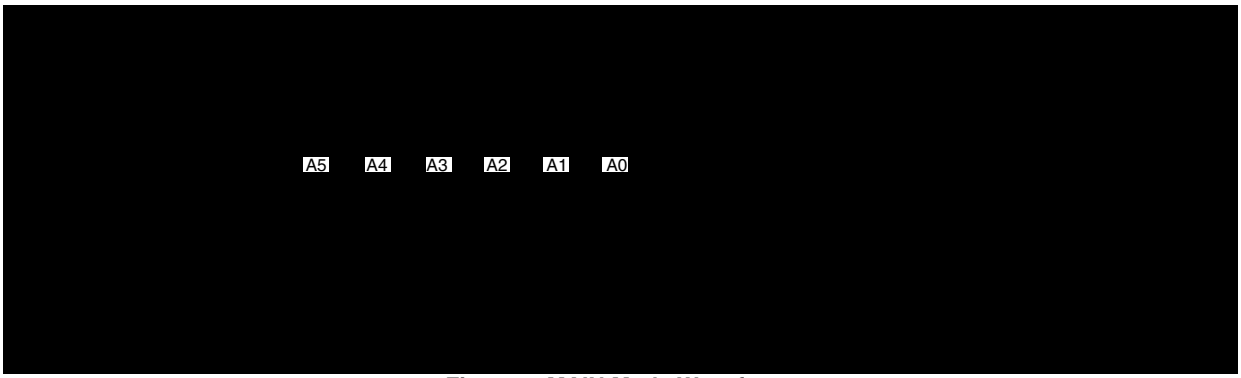


Figure 5. MAIN Mode Waveforms

Table 1. ML6510-80 ROM Codes

CODE	DESCRIPTION	SELECTION BITS			INPUT FREQ (MHz)	OUTPUT FREQ (MHz)	CONFIGURATION CODE					
		ROMMSB	MCLK	MDOUT			CS	CM	R1, R0	M	N	TEST
0	PECL Input Clock, 1x mode	0	0	0	40-80	40-80	1	1	01	0	0	0
1	PECL Input Clock, 0.5x mode	0	0	1	40-80	20-40	1	1	10	5	2	0
2	PECL Input Clock, 2x mode	0	1	0	20-40	40-80	1	1	01	2	5	0
3	PECL Input Clock, 1x mode	0	1	1	40-80	40-80	1	0	01	0	0	0
4	TTL Input Clock, 1x mode	1	0	0	40-80	40-80	0	0	01	0	0	0
5	TTL Input Clock, 0.5x mode	1	0	1	40-80	20-40	0	0	10	5	2	0
6	TTL Input Clock, 2x mode	1	1	0	20-40	40-80	0	0	01	2	5	0
7	TEST mode, TTL Input clock	1	1	1	0-50	0-50	0	—	—	—	—	1

Figure 6. AUX Mode Waveform.

Register Definitions

REGISTER	SIZE	FUNCTION
N	7 bit	This register is used to define the ratio for the desired frequency of the primary clock.
R	2 bit	This register defines the frequency of the primary clocks, CLK [0-7].
CM	1 bit	Set CM = 1 when the PECL input reference clock is from another 6510 reference clock output. Set CM = 0 if the clock reference is TTL or PECL from an external source and minimum phase error between input and output is desired.
CS	1 bit	CS = 0 selects TTL input clock, CS = 1 selects PECL input clock.
TEST	1 bit	When set to 1, the PLL is bypassed for low frequency testing.
M	6 bit	This register is used to define the ratio for the desired frequency of the primary clock.

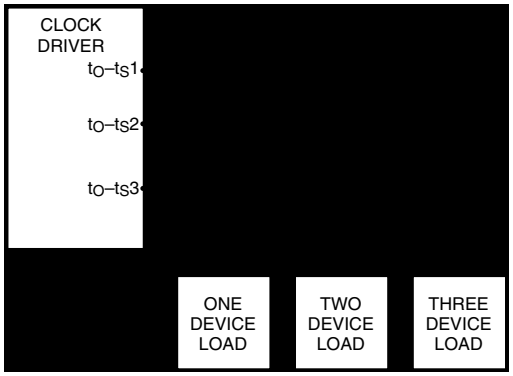
ML6510-80 Shift register chain

Applications

Zero skew clock generation

The most advantageous feature of using PACMan is its ability to deliver multiple copies of the clock to the load with very low skew. Because of its unique ability in deskewing, trace length and load consideration are no longer critical in board design.

Because of the unique deskewing scheme, neither the trace length nor the device loads need to be equal. This is true for loads, <20pF. Higher loads can be driven if they are placed close to the clock chip, to guarantee signal integrity.



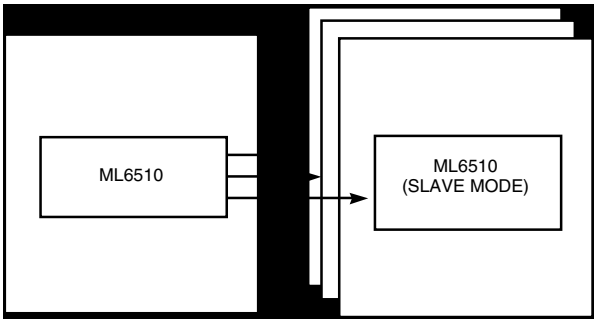
Low skew clock distribution

Clock distribution design is usually not a trivial task, especially when multiple clock chips are needed. By using closely grouped PACMans, 16 or more clock lines can be created with low part-to-part skew. Additional groups of clocks can be clustered and driven from deskewed clock lines, to minimize the number of long-distance clock lines.

Board to Board synchronization

Distribution of the synchronous clock could present significant difficulty at high frequency. With the system clock generated by the ML6510, a zero skew clock delivery to a backplane is now possible. By using the ML6510 slave chip or the ML6510 in slave mode at the receiver end, a near zero delay clock link can be accomplished between the mother board and the satellite boards.

Because the PACMan has frequency doubling capability, a lower frequency signal can be used to route across a back plane.



Example configuration

Shown in Figure 7 is an example configuration using two ML6510-80 chips in tandem to generate eight 66 MHz clocks and eight 33MHz low-skew clocks from a 66MHz input reference. This requires only the termination resistors. Configurations are loaded from the internal ROM. PCB traces 0 to 15 are each 50Ω impedance and the load capacitances C_{L0}-CL_{15} are 0 to 20pF each. No trace length matching is required among separate clock outputs. All traces are shown with a series termination at the output.

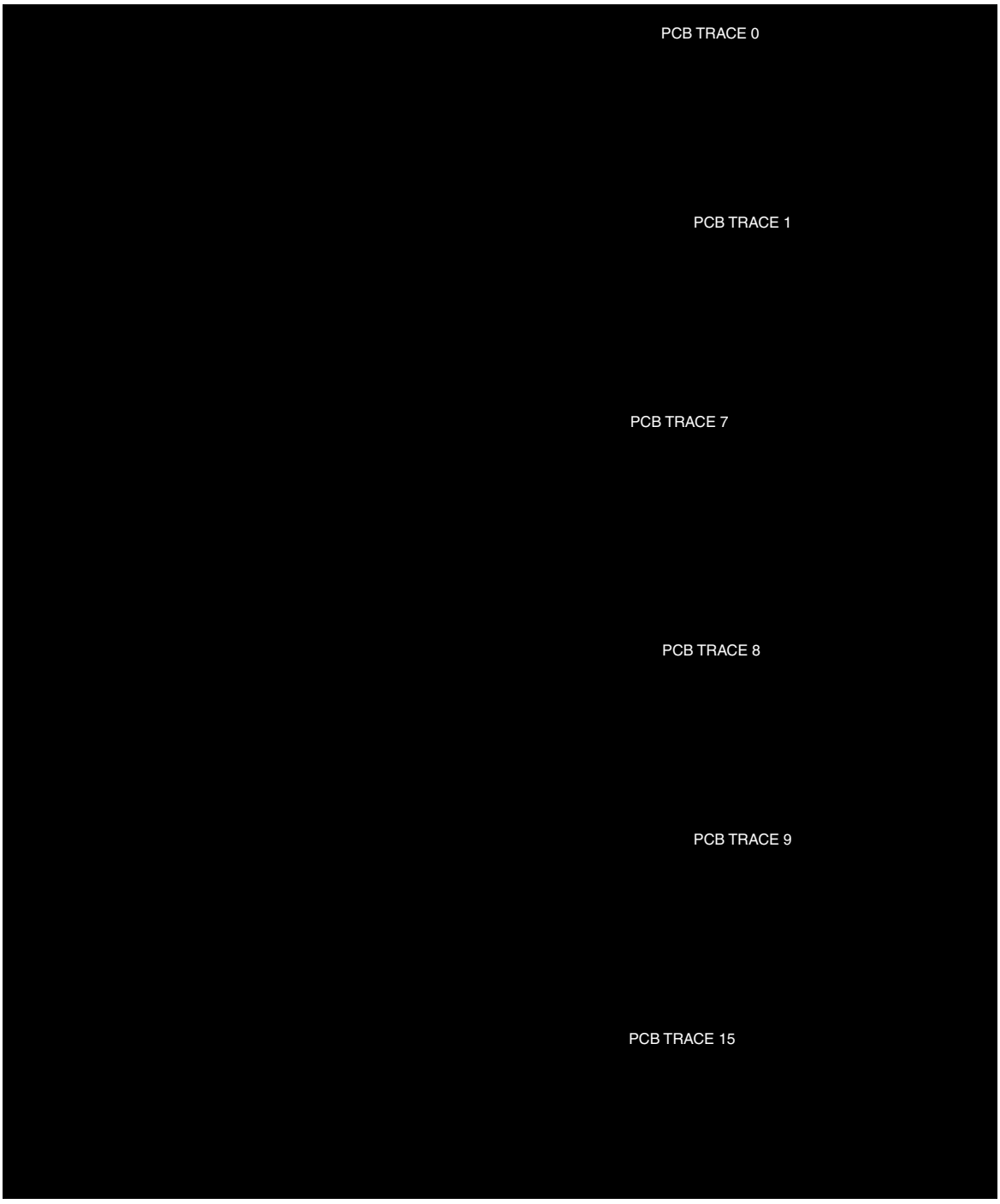
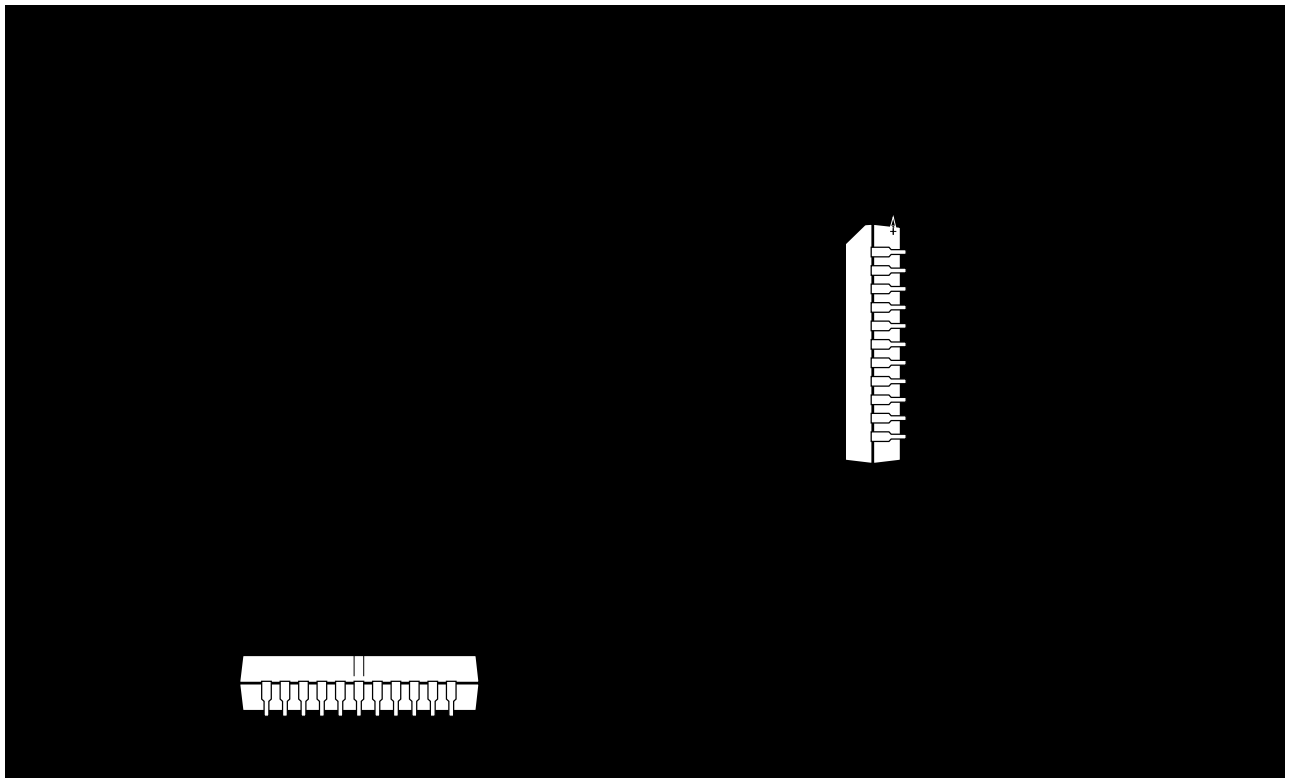


Figure 7. Example use of two ML6510-80 to generate multiple frequency clocks. First ML6510-80 generates eight 66MHz clocks while second ML6510-80 takes 66MHz small-swing reference from the first chip and generates eight 33MHz clocks.

Physical Dimensions inches (millimeters)



Ordering Information

Part Number	Temperature Range	Package
ML6510CQ80	0°C to 70°C	44-pin PLCC (Q44)

12/30/00 0.0m 002
Stock#DS30006510