

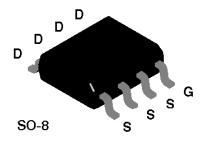
NDS8426A Single N-Channel Enhancement Mode Field Effect Transistor

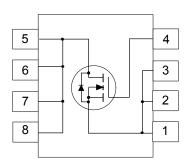
General Description

SO-8 N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 10.5 A, 20 V. $R_{DS(ON)} = 0.0135 \Omega$ @ $V_{GS} = 4.5 V$. $R_{DS(ON)} = 0.016 \Omega$ @ $V_{GS} = 2.7 V$.
- High density cell design for extremely low R_{DS(ON)}.
- High power and current handling capability in a widely used surface mount package.





ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS8426A	Units
V _{DSS}	Drain-Source Voltage		20	V
V _{GSS}	Gate-Source Voltage		±8	V
I _D	Drain Current - Continuous	(Note 1a)	10.5	A
	- Pulsed		30	
P _D	Maximum Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMA	L CHARACTERISTICS			
R _{eJA}	Thermal Resistance, Junction-to-Ambie	nt (Note 1a)	50	°C/W
R _{eJC}	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CHA	RACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 16 V, V _{GS} = 0 V				1	μΑ
			T _J = 55°C			10	μΑ
GSSF	Gate - Body Leakage, Forward	V _{GS} = 8 V, V _{DS} = 0 V	·			100	nA
GSSR	Gate - Body Leakage, Reverse	V _{GS} = -8 V, V _{DS} = 0 V				-100	nA
ON CHAR	ACTERISTICS (Note 2)	·			•	•	
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		0.4	0.6	1	V
			T _J = 125°C	0.3	0.5	0.8	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 10.5 \text{ A}$			0.012	0.0135	Ω
			T _J = 125°C		0.017	0.024	
		$V_{GS} = 2.7 \text{ V}, I_D = 10 \text{ A}$			0.014	0.016	
D(on)	On-State Drain Current	V _{GS} = 4.5 V, V _{DS} = 5 V		30			Α
) _{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_{D} = 10.5 \text{ A}$			43		S
DYNAMIC	CHARACTERISTICS						
C _{iss}	Input Capacitance	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz			2150		pF
Coss	Output Capacitance				890		pF
C _{rss}	Reverse Transfer Capacitance				165		pF
SWITCHIN	IG CHARACTERISTICS (Note 2)						
D(on)	Tum - On Delay Time	$V_{DD} = 5 \text{ V}, I_{D} = 1 \text{ A},$ $V_{GEN} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$			11	30	ns
r	Tum - On Rise Time				26	55	ns
D(off)	Turn - Off Delay Time				145	220	ns
f	Turn - Off Fall Time				40	100	ns
Q_g	Total Gate Charge	$V_{DS} = 10 \text{ V},$ $I_{D} = 10.5 \text{ A}, V_{GS} = 4.5 \text{ V}$			43	60	nC
Q_{gs}	Gate-Source Charge				7		nC
Q_{gd}	Gate-Drain Charge				8		nC

ELECTRICAL CHARACTERISTICS (T _A = 25°C unless otherwise noted)							
Symbol	Parameter	Conditions	Min	Тур	Max	Units	
DRAIN-SOURCE DIODE CHARACTERISTICS							
I _s	Continuous Source Diode Current 2.1		Α				
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.1 A (Note 2)		0.6	1.2	V	

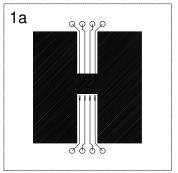
Notes:

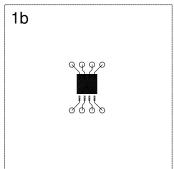
1. $R_{g,k}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{g,k}$ is guaranteed by design while $R_{g,k}$ is determined by the user's board design.

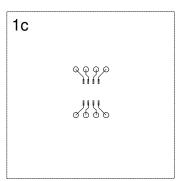
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{_{\theta^{JA}}}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- a. 50°C/W when mounted on a 1 in² pad of 2oz copper.
- b. 105°C/W when mounted on a 0.04 in² pad of 2oz copper.
- c. 125°C/W when mounted on a 0.006 in² pad of 2oz copper.







Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

Typical Electrical Characteristics

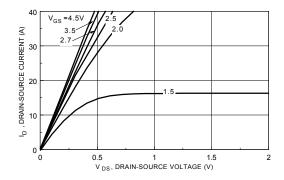


Figure 1. On-Region Characteristics.

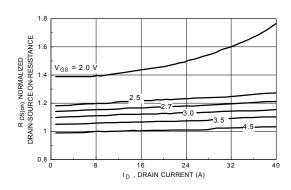


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

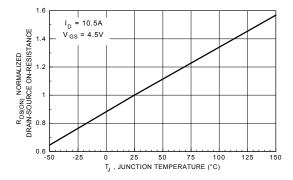


Figure 3. On-Resistance Variation with Temperature.

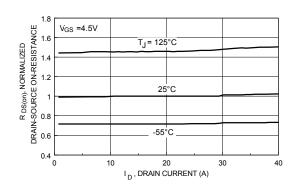


Figure 4. On-Resistance Variation with Drain Current and Temperature.

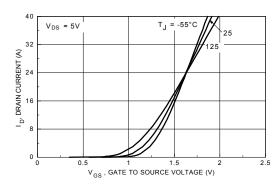


Figure 5. Transfer Characteristics.

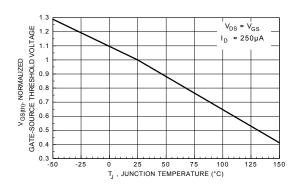


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

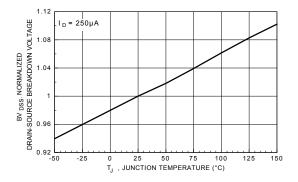


Figure 7. Breakdown Voltage Variation with Temperature.

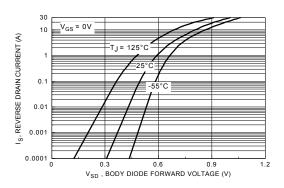


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature.

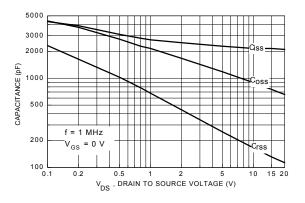


Figure 9. Capacitance Characteristics.

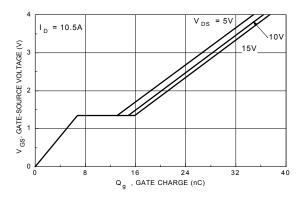


Figure 10. Gate Charge Characteristics.

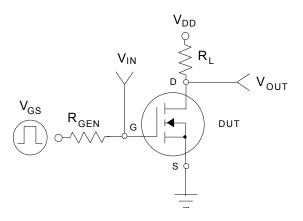


Figure 11. Switching Test Circuit.

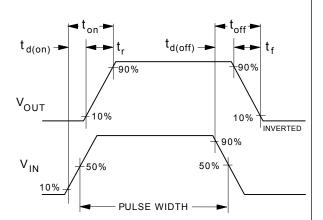


Figure 12. Switching Waveforms.

Typical Electrical and Thermal Characteristics (continued)

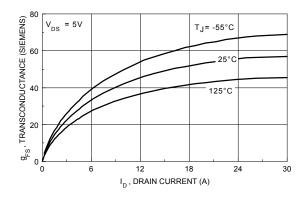
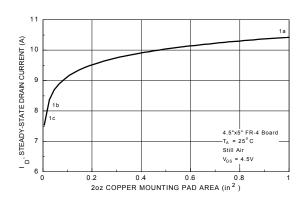


Figure 13. Transconductance Variation with Drain Current and Temperature.

Figure 14. SO-8 Maximum Steady-State Power
Dissipation versus Copper Mounting Pad Area.



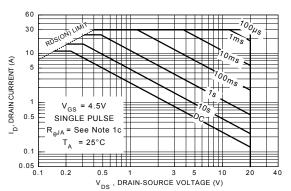


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

Figure 16. Maximum Safe Operating Area.

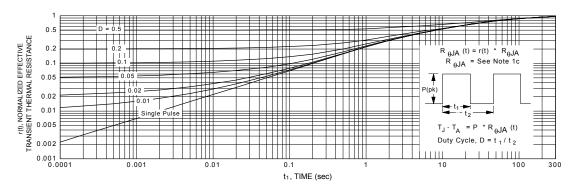


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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