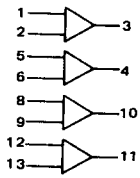
# MC1020
# MC1220

Four differential amplifiers with emitter follower outputs, for use as a comparator or for sensing differential signals over long lines. Each amplifier provides the OR or NOR logic function depending on which input is biased at a given reference voltage.

## POSITIVE LOGIC

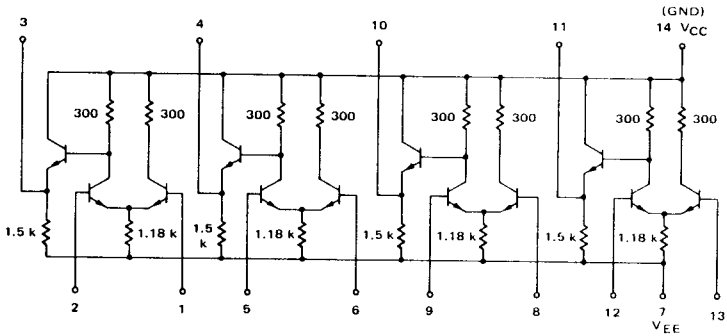



DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 115 mW typ

## TRUTH TABLE

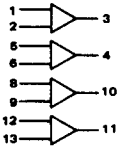
| | | | |
|---|---|---|---|
| 1 | 2 | 3 | |
| 6 | 5 | 4 | |
| 8 | 9 | 10 | |
| 13 | 12 | 11 | |
| $V_{BB}$ | H | L | NOR |
| $V_{BB}$ | L | H | NOR |
| H | $V_{BB}$ | H | OR |
| L | $V_{BB}$ | L | OR |

## CIRCUIT SCHEMATIC



## ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one line receiver.
The other line receivers are tested in the same manner.

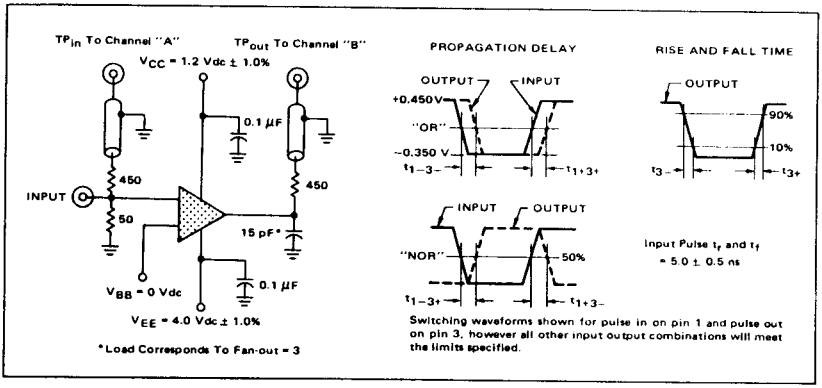



| | @Test Temperature | $V_{IL\ min}$ to $V_{IL\ max}$ | $V_{IH\ min}$ to $V_{IH\ max}$ | $V_{IH\ max}$ | $V_{EE}$ | $V_{BB}$ | $I_L$ |
|---|---|---|---|---|---|---|---|
| | | TEST VOLTAGE/CURRENT VALUES | | | | | |
| | | Vdc ±1.0% | | | | | mAdc |
| MC1220 | −55°C | -5.2 to -1.405 | -1.165 to -0.825 | - | -5.2 | -1.270 | -2.5 |
| | +25°C | -5.2 to -1.325 | -1.025 to -0.700 | -0.700 | -5.2 | -1.175 | -2.5 |
| | +125°C | -5.2 to -1.205 | -0.875 to -0.530 | - | -5.2 | -1.025 | -2.5 |
| MC1020 | 0°C | -5.2 to -1.350 | -1.070 to -0.740 | - | -5.2 | -1.210 | -2.5 |
| | +25°C | -5.2 to -1.325 | -1.025 to -0.700 | -0.700 | -5.2 | -1.175 | -2.5 |
| | +75°C | -5.2 to -1.260 | -0.950 to -0.615 | - | -5.2 | -1.115 | -2.5 |

| Characteristic | Symbol | Pin Under Test | MC1220 Test Limits −55°C Min | −55°C Max | +25°C Min | +25°C Max | +125°C Min | +125°C Max | Unit | MC1020 Test Limits 0°C Min | 0°C Max | +25°C Min | +25°C Max | +75°C Min | +75°C Max | Unit | TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ min}$ to $V_{IL\ max}$ | $V_{IH\ min}$ to $V_{IH\ max}$ | $V_{IH\ max}$ | $V_{EE}$ | $V_{BB}$ | $I_L$ | $V_{CC}$ (Gnd) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Power Supply Drain Current | $I_E$ | 7 | - | - | - | 28 | - | - | mAdc | - | - | - | 28 | - | - | mAdc | - | - | - | 2,5,7,9,12 | 1,6,8,13 | - | 14 |
| Input Current | $I_{in}$ | 1 | - | - | - | 100 | - | - | μAdc | - | - | - | 100 | - | - | μAdc | - | - | 1 | 5,6,7,8,9,12,13 | 2 | - | 14 |
| | | 2 | - | - | - | 100 | - | - | μAdc | - | - | - | 100 | - | - | μAdc | - | - | 2 | 5,6,7,8,9,12,13 | 1 | - | 14 |
| Input Leakage Current | $I_R$ | 1 | - | - | - | 0.2 | - | 1.0 | μAdc | - | - | - | 0.2 | - | 1.0 | μAdc | - | - | - | 1,5,6,7,8,9,12,13 | 2 | - | 14 |
| | | 2 | - | - | - | 0.2 | - | 1.0 | μAdc | - | - | - | 0.2 | - | 1.0 | μAdc | - | - | - | 2,5,6,7,8,9,12,13 | 1 | - | 14 |
| "NOR" Logical "1" Output Voltage† | $V_{OH}$† | 3 | -0.990 | -0.825 | -0.850 | -0.700 | -0.700 | -0.530 | Vdc | -0.895 | -0.740 | -0.850 | -0.700 | -0.775 | -0.615 | Vdc | 2 | - | - | 5,6,7,8,9,12,13 | 1 | 3 | 14 |
| "NOR" Logical "0" Output Voltage | $V_{OL}$ | 3 | -1.890 | -1.580 | -1.800 | -1.500 | -1.720 | -1.380 | Vdc | -1.830 | -1.525 | -1.800 | -1.500 | -1.760 | -1.435 | Vdc | - | 2 | - | 5,6,7,8,9,12,13 | 1 | - | 14 |
| "OR" Logical "1" Output Voltage† | $V_{OH}$† | 3 | -0.990 | -0.825 | -0.850 | -0.700 | -0.700 | -0.530 | Vdc | -0.895 | -0.740 | -0.850 | -0.700 | -0.775 | -0.615 | Vdc | - | 1 | - | 5,6,7,8,9,12,13 | 2 | - | 14 |
| "OR" Logical "0" Output Voltage | $V_{OL}$ | 3 | -1.890 | -1.580 | -1.800 | -1.500 | -1.720 | -1.380 | Vdc | -1.830 | -1.525 | -1.800 | -1.500 | -1.760 | -1.435 | Vdc | 1 | - | - | 5,6,7,8,9,12,13 | 2 | - | 14 |
| Switching Times | | | Typ | Max | Typ | Max | Typ | Max | | Typ | Max | Typ | Max | Typ | Max | | Pulse In | Pulse Out | | $V_{EE}$ = −4.0 Vdc | | | (+1.2V) |
| Propagation Delay (Fan-Out = 3) | $t_{1+3-}$ | 3 | 4.0 | 7.0 | 4.0 | 7.0 | 5.0 | 8.0 | ns | 4.0 | 7.0 | 4.0 | 7.0 | 4.0 | 7.5 | ns | 1 | 3 | - | 5,6,7,8,9,12,13 | 2 | - | 14 |
| | $t_{1-3+}$ | | 4.0 | 7.0 | 4.0 | 7.0 | 5.0 | 8.0 | | 4.0 | 7.0 | 4.0 | 7.0 | 4.0 | 7.5 | | | | - | | | - | |
| Rise Time (Fan-Out = 3) | $t_{3+}$ | | 4.0 | 7.0 | 4.0 | 7.0 | 5.0 | 8.0 | | 4.0 | 7.0 | 4.0 | 7.0 | 4.0 | 7.5 | | | | - | | | - | |
| Fall Time (Fan-Out = 3) | $t_{3-}$ | | 5.0 | 8.0 | 5.0 | 8.0 | 6.0 | 9.0 | | 5.0 | 8.0 | 5.0 | 8.0 | 5.0 | 8.5 | | | | - | | | - | |

† $V_{OH}$ limits apply from no load (0 mA) to full load (-2.5 mA).

**SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C**




## APPLICATIONS INFORMATION

The MC1020/MC1220 quad line receiver is used primarily to receive data from balanced twisted pair lines, as indicated in Figure 1. Any MECL II gate with differential outputs may be used to drive the twisted pair line. The line is terminated in its characteristic impedance (around 100 ohms). A voltage divider is formed between the high-level gate output, the terminating resistor, and the pull-down resistor on the low-level gate output. The equivalent dc circuit is shown in Figure 2. The voltage swing across the terminating resistor ($R_T$) is typically ± 275 mV. Any input voltage swing in excess of 120 mV is adequate due to the voltage gain of the MC1020/MC1220. The output of the line receiver is the same as a standard MECL II gate. For worst-case pull-down resistors in the driving gate (1.5 k ohms ± 20%) and a $V_{OH\ min}$, the differential drop across an $R_T$ of 100 ohms is ± 230 mV.

Very long lines may be used with excellent results. The only restriction on lead length (other than common mode noise) is series line resistance. The nominal voltage drop across $R_T$ is actually shared with the series resistance of the twisted pair line. The resistance of # 22 AWG wire averages about 16 ohms per 1000 feet, while # 24 AWG wire averages about 26 ohms per 1000 feet. For very long lines, an additional voltage drop across $R_T$ is easily obtained by paralleling additional pull-down resistors with those internal to the driver gate. For example, by paralleling a 1.5 k ohm resistor with each output, the voltage drop across $R_T$ is effectively doubled.

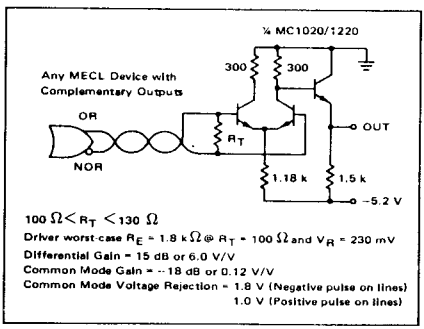
Extensive data have shown that a positive transient of 1.0 V or a negative transient of 1.8 V may be introduced on the twisted pair line before noise can propagate through another MECL device tied to the line receiver output. This method of data transmission is useful at frequencies to 50 MHz and results in the highest bandwidth – noise immunity product obtainable with digital logic. A twisted pair is recommended for clock distribution in high-speed systems since distribution skew time may be balanced out by adjusting line lengths. Propagation delay times are approximately 1.0 ns per eight inches of line.

In system design it is often convenient to organize information transfer with a data bus or "party-line" approach. In this application, one of many sources may "talk" to the common data line and multiple receivers may "listen". Figure 3 illustrates such a data bus utilizing MECL II gates as drivers and MC1020's as line receivers. Note that the line is unbalanced, but this will in turn allow all drivers to be ORed together. Bandwidth of data distribution is excellent. The technique may be used to 50 MHz at 25°C and to 40 MHz over the entire military temperature range. Noise immunity is also good due to the low impedance methods of transmission and the common mode rejection of the line receiver. The following results were obtained during an evaluation of the data bus shown in Figure 3 under worst-case conditions:

Number of driver gates: 6
Number of receivers: 8
Line length: 24 feet
Differential temperature from transmitter gate to receiver gate: 100°C
Maximum operating frequency: 40 MHz
Total terminating resistance: 45 ohms
Differential power supply voltage from transmitter gate to receiver gate: ± 5.0%

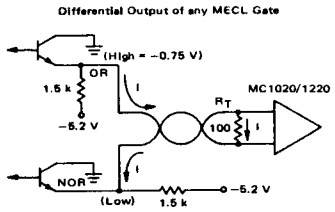
The quad line receiver can also be used in many linear applications. The voltage gain is typically 7.0, with a bandwidth of approximately 70 MHz for each differential amplifier. The device makes an excellent FM limiter with minimal phase shift. By employing feedback, both selective band-pass amplifiers and notch frequency rejection amplifiers may be built. Figure 4 shows ¼ of the quad line receiver used as a parallel tuned-crystal oscillator that exhibits excellent stability.

**FIGURE 1 - MECL LINE RECEIVER**




100 Ω < $R_T$ < 130 Ω
Driver worst-case $R_E$ = 1.8 kΩ @ $R_T$ = 100 Ω and $V_R$ = 230 mV
Differential Gain = 15 dB or 6.0 V/V
Common Mode Gain = -18 dB or 0.12 V/V
Common Mode Voltage Rejection = 1.8 V (Negative pulse on lines)
1.0 V (Positive pulse on lines)

FIGURE 2 - LINE RECEIVER DC EQUIVALENT CIRCUIT



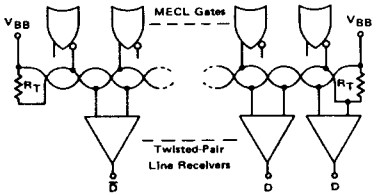

$V_R$ = voltage drop across terminating resistor ($R_T$)

$$V_R = \frac{(5.2\ V - 0.75\ V)\ (100\Omega)}{1.5\ k\Omega + 100\Omega}$$

$$= \frac{4.45\ (100)}{1.6\ k}$$

$$= 275\ mV$$

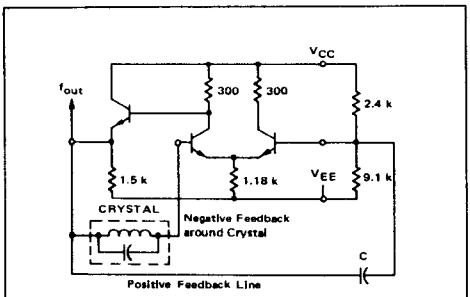
FIGURE 3 - DATA BUS DRIVING WITH MECL II




System Design Criteria

1. A total of two emitter pull-down resistors is recommended in the driver gates.
2. $R_T$ should be $Z_{out}$ of the twisted pair line $\approx$100 ohms
3. Either OR or NOR outputs may drive the line.
4. All driver gates are ORed together.
5. The line reciver output is Data or $\overline{Data}$ depending upon the input configuration.
6. $V_{BB}$ should be able to source 7.0 mA or sink 8.0 mA total current.

FIGURE 4 - ¼ MC1020/1220 AS A PARALLEL-TUNED CRYSTAL OSCILLATOR




For further information see Application Note AN-417.