

05

T-45-23-21

9305

VARIABLE MODULUS COUNTER

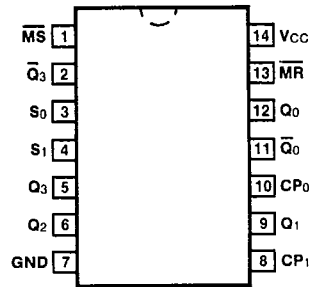
DESCRIPTION — The '05 is a monolithic, high speed, variable modulus counter circuit. It is a semisynchronous counter which can be programmed without extra logic to provide division or counting by either 2 and 4, 5, 6, 7, 8 or 10, 12, 14, 16. A binary count sequence can be obtained for all of the preceding counter modulus as well as 50% duty cycle output for dividers of 8, 10, 12, 14, 16. The device also features asynchronous overriding Master Reset and Set inputs and the negation output of the final flip-flop output which allows the cascading of stages.

- **VARIOUS BINARY COUNTING MODES**
 MODULO 2 AND MODULO 5, 6, 7, 8
 MODULO 10 (8421 BCD) 12, 14, 16
- **VARIOUS DIVISION MODES WITH 50% DUTY CYCLE OUTPUT**
 MODULO 8, 10, 12, 14, 16
- **LOGIC SELECTION OF COUNTING MODE**
- **ASYNCHRONOUS MASTER RESET AND SET INPUTS**
- **MULTISTAGE COUNTING OPERATION**

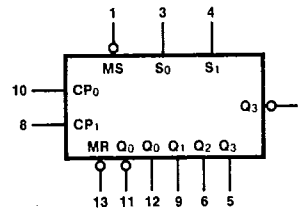
ORDERING CODE: See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE | MILITARY GRADE | PKG TYPE |
|-----------------|---------|--|--|----------|
| | | V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C | V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C | |
| Plastic DIP (P) | A | 9305PC | | 9A |
| Ceramic DIP (D) | A | 9305DC | 9305DM | 6A |
| Flatpak (F) | A | 9305FC | 9305FM | 3B |

CONNECTION DIAGRAM PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

| PIN NAMES | DESCRIPTION | 93XX (U.L.) HIGH/LOW |
|---------------------------------|--|----------------------|
| S ₀ , S ₁ | Select Inputs | 1.0/1.0 |
| CP ₀ | First Stage Clock Pulse Input (Active Rising Edge) | 1.0/1.0 |
| CP ₁ | Three Stage Clock Pulse Input (Active Rising Edge) | 1.0/1.0 |
| MS | Master Set Input (Active LOW) | 1.0/1.0 |
| MR | Master Reset Input (Active LOW) | 1.0/1.0 |
| Q ₀ | First Stage Output | 16/8.0 |
| Q ₀ | Complementary First Stage Output | 16/8.0 |
| Q ₁ — Q ₃ | Three Stage Counter Outputs | 16/8.0 |
| Q ₃ | Complementary Last Stage Output | 20/10 |

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FUNCTIONAL DESCRIPTION — The '05 consists of four master/slave flip-flops which are separated into two functional units — a single toggle stage and a three stage synchronous counter. All four flip-flops change state on the LOW-to-HIGH transition of the clock. The three stage counter can be programmed with external connections to provide moduli of either 5, 6, 7 or 8. This basic configuration allows synchronous binary counting by the last three stages and independent modulo 2 operation with the first single stage.

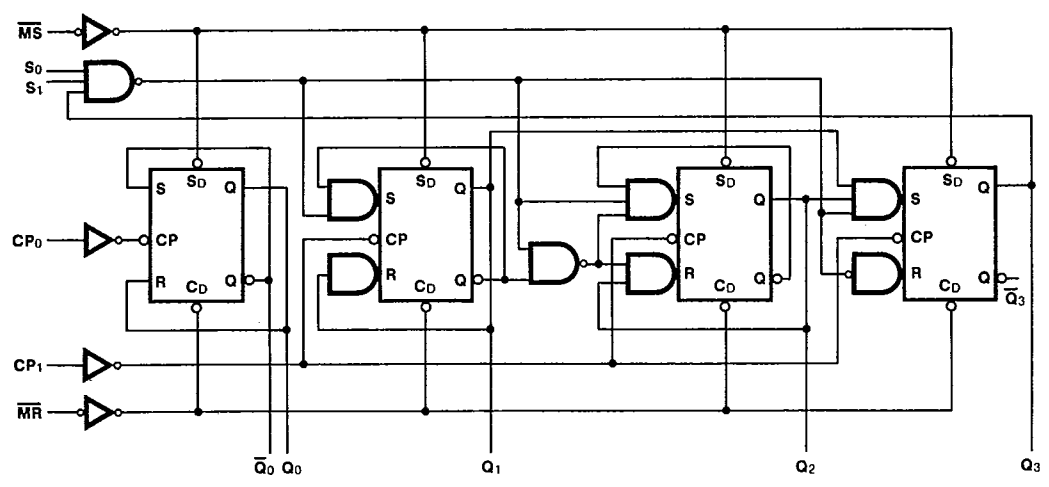
A four stage binary counter with a modulo of 10, 12, 14 or 16 is obtained by applying the incoming clock to the single toggle stage and feeding its negation output to the clock input of the three stage counter. A 4-stage divider with 50% duty cycle output is produced by feeding the incoming clock to the three stage counter and clocking the single stage with the \overline{Q}_3 output. In either the binary or 50% division mode the modulo (10, 12, 14, 16) is determined by the external programming connections for the three stage counter. These 4-stage counters or dividers are not fully synchronous (semisynchronous) but have only one flip-flop ripple delay in either configuration. Counter moduli other than 10, 12, 14, 16 can be formed with a few extra gates.

Several '05 variable modulus counters programmed in any modulo can be connected together without extra logic to form asynchronous (ripple) type multistage counters. This is done by connecting the \overline{Q}_3 output of the less significant counter to the clock input of the following counter.

The Master Set and Reset will asynchronously set or reset all four stages when activated. The active LOW Reset input when LOW will clear the counter, overriding the clock and forcing the outputs $Q_0 - Q_3$ LOW and outputs $\overline{Q}_0, \overline{Q}_3$ HIGH. The active LOW Set input when LOW will preset the counter, overriding the clock and forcing the outputs $Q_0 - Q_3$ HIGH and outputs $\overline{Q}_0, \overline{Q}_3$ LOW. The master set provides a synchronous clear, since the first clock pulse following the asynchronous master set will reset all stages. This action is independent of the modulo programmed.

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LOGIC DIAGRAM



COUNTING MODE

The following are rules specifying the external connections required for various counter and divider modulus.

ASYNCHRONOUS MODE

| INPUTS | | OUTPUTS | | | | | |
|--------|----|----------------|----------------|----------------|----------------|----------------|----------------|
| MS | MR | Q ₀ | Q ₀ | Q ₁ | Q ₂ | Q ₃ | Q ₃ |
| L | H | H | L | H | H | H | L |
| H | L | L | H | L | L | L | H |
| H | H | COUNT* | | | | | |

*As determined by programming connections.
 H = HIGH Voltage Level
 L = LOW Voltage Level

PROGRAMMING CONNECTIONS FOR LAST THREE STAGES

| S ₀ | S ₁ | MODULO |
|----------------|----------------|--------|
| NC | NC | 5 |
| Q ₁ | NC | 6 |
| NC | Q ₁ | 6 |
| Q ₂ | NC | 7 |
| NC | Q ₂ | 7 |
| Q ₁ | Q ₂ | 8 |
| Q ₂ | Q ₁ | 8 |

NC = Not Connected

CONNECTIONS FOR MODULO 10, 12, 14, 16 BINARY COUNTERS AND 50% DUTY CYCLE DIVIDERS

| |
|---|
| For Binary Counting Q ₀ connected to CP ₁ Incoming clock to CP ₀ |
| For 50% Duty Cycle Output Q ₃ connected to CP ₀ Incoming Clock to CP ₁ |

ALTERNATE PROGRAMMING CONNECTIONS FOR LAST THREE STAGES**

| MODULO | INPUTS | | OUTPUT | AVAILABLE OUTPUT FAN-OUT |
|--------|----------------|----------------|----------------|--------------------------|
| | S ₀ | S ₁ | | |
| 5 | Q ₃ | Q ₃ | Q ₃ | 14/8.0 |
| 6 | Q ₁ | Q ₁ | Q ₁ | 14/7.0 |
| 7 | Q ₂ | Q ₂ | Q ₂ | 14/7.0 |
| 8 | Q ₁ | Q ₂ | Q ₂ | 15/7.0 |
| 8 | Q ₂ | Q ₁ | Q ₁ | 15/7.0 |

**The alternate programming connections program the counter and conveniently terminate unused select inputs (NC). Since these inputs form the inputs to a single NAND gate (See logic diagram), their connection to the counter outputs for the various count modulus provides the indicated output drive.

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| SYMBOL | PARAMETER | 93XX | | UNITS | CONDITIONS |
|-----------------|------------------------------|------|-----|-------|---|
| | | Min | Max | | |
| I _{SC} | Output Short Circuit Current | -20 | -70 | mA | V _{CC} = Max, V _{OUT} = 0 V |
| I _{CC} | Power Supply Current | | 66 | mA | V _{CC} = Max |

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

| SYMBOL | PARAMETER | 93XX | | UNITS | CONDITIONS |
|--------------------------------------|---|------------------------|----------|-------|---|
| | | C _L = 15 pF | | | |
| | | Min | Max | | |
| f _{max} | Maximum Count Frequency | 23 | | MHz | Modulo 16 (S ₀ to Q ₁ , S ₁ to Q ₂ , Q ₀ to CP ₁ , Input to CP ₀) Figs. 3-1, 3-8 |
| t _{PLH} t _{PHL} | Propagation Delay CP ₀ to Q ₃ (Modulo 16 Connection) | | 38 48 | ns | |
| t _{PLH} t _{PHL} | Propagation Delay CP ₀ to Q ₀ | | 21 30 | ns | Modulo-16 Figs. 3-1, 3-8 |
| t _{PLH} t _{PHL} | Propagation Delay CP ₁ to Q ₃ or Q ₃ | | 23 30 | ns | Modulo-8 Figs. 3-1, 3-8 |
| t _{PLH} | Propagation Delay M _S to Q ₁ | | 26 | ns | Modulo-8 Figs. 3-1, 3-16 |
| t _{PHL} | Propagation Delay M _R to Q ₁ | | 35 | ns | Modulo-8 Figs. 3-1, 3-16 |

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

| SYMBOL | PARAMETER | 93XX | | UNITS | CONDITIONS |
|------------------|--|------|-----|-------|------------|
| | | Min | Max | | |
| t _w | CP ₀ Pulse Width | 22 | | ns | Fig. 3-8 |
| t _w | M _R or M _S Pulse Width | 24 | | ns | Fig. 3-16 |
| t _{rec} | Recovery Time M _S to CP ₁ | 25 | | ns | Fig. 3-16 |
| t _{rec} | Recovery Time M _R to CP ₁ | 30 | | ns | Fig. 3-16 |

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