Data Sheet | September 2003 | FN9060.2

Integrated Power Stage

Processors that operate above 1GHz require fast, intelligent power systems. The ISL6580 Integrated Power Stage is a High Side FET/driver combination that provides high current capability per converter phase at high switching frequency. The chip incorporates intelligence to provide fast transient response and digital communication to the ISL6590 Digital Controller. The ISL6580 integrates key power stage components for fast power delivery, effective thermal design and increased noise immunity. It incorporates an integrated P-channel high side MOSFET, high side MOSFET driver and a driver for external synchronous rectifier, low side MOSFETs. The ISL6580 also features a window comparator for fast transient response as well as on-board voltage and current A/D converters for intelligent digital communication and control by the ISL6590 Controller.

Furthermore, through the communication bus, configuration and fault monitoring via the ISL6590 are available.

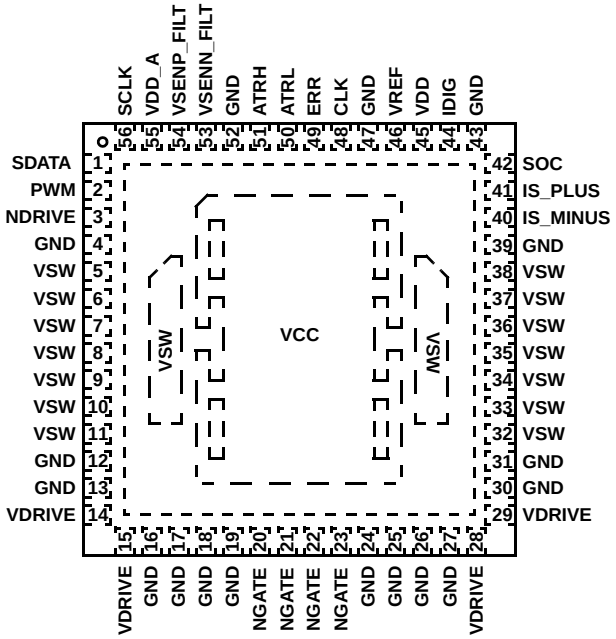
For more information, see the ISL6590 datasheet.

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. DWG. #
ISL6580CR	0 to 70	56 Ld 8x8 QFN	L56.8x8C
ISL6580CR-T	56 Ld QFN Tape & Reel		
ISL6580/90EVAL1	Evaluation Board		
ISL6580/90EVAL2	Evaluation Board		
ISL6580/90EVAL3	Evaluation Board		

Pinout

ISL6580 (QFN)
TOP VIEW



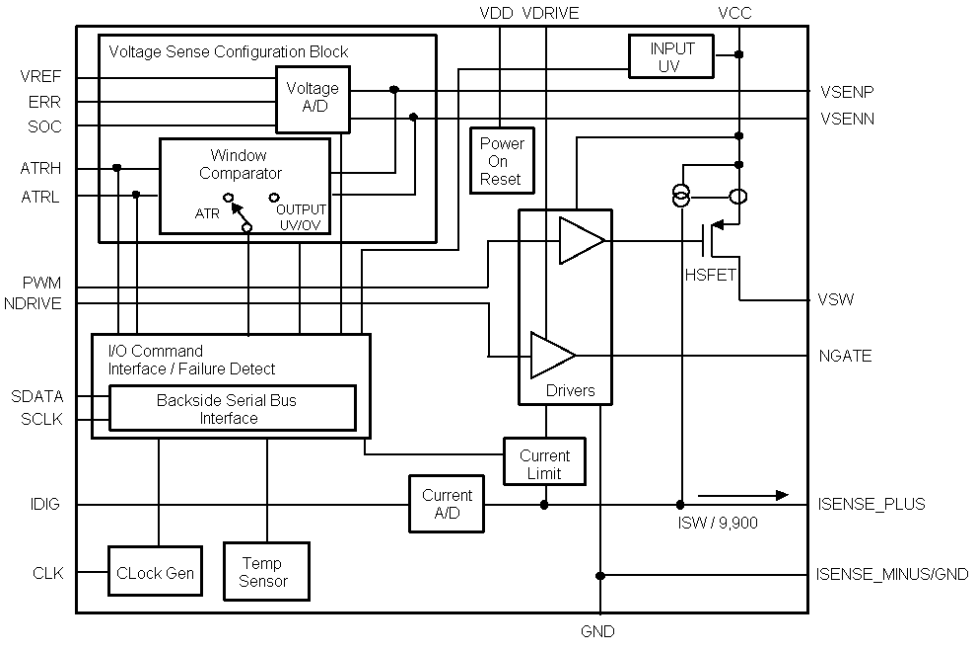
Features

- Optimized for Intel VR10 applications
- V_{IN} = 12V
- Phase switching frequencies of 250kHz to 1MHz
- Phase current capability up to 25A
- High Side P-channel MOSFET
- Low Side MOSFET drivers
- Accurate, lossless, Current Sense
- Programmable MOSFET non-overlap timing (through the ISL6590 Digital Controller)
- Active Transient Response (ATR) minimizes voltage droop/overshoot during large load current transients.
- Serial control interface for system monitoring and configuration (with ISL6590 Controller)
  - Input Under Voltage Protection
  - Output Under/Over Voltage Protection
  - Peak Current Limit
  - Thermal Shutdown
  - ATR Limits
- Provides an optimal power solution when combined with the ISL6590 Digital Controller
  - Output voltage regulation range of 0.3VDC to 1.85VDC
  - VRM-9 and VRM-10 VID Codes
- Digital interface for high noise immunity and point-of-load placement
- On board analog-to-digital converters
  - 10 Msample/sec voltage A/D
  - 1 Msample/sec current A/D

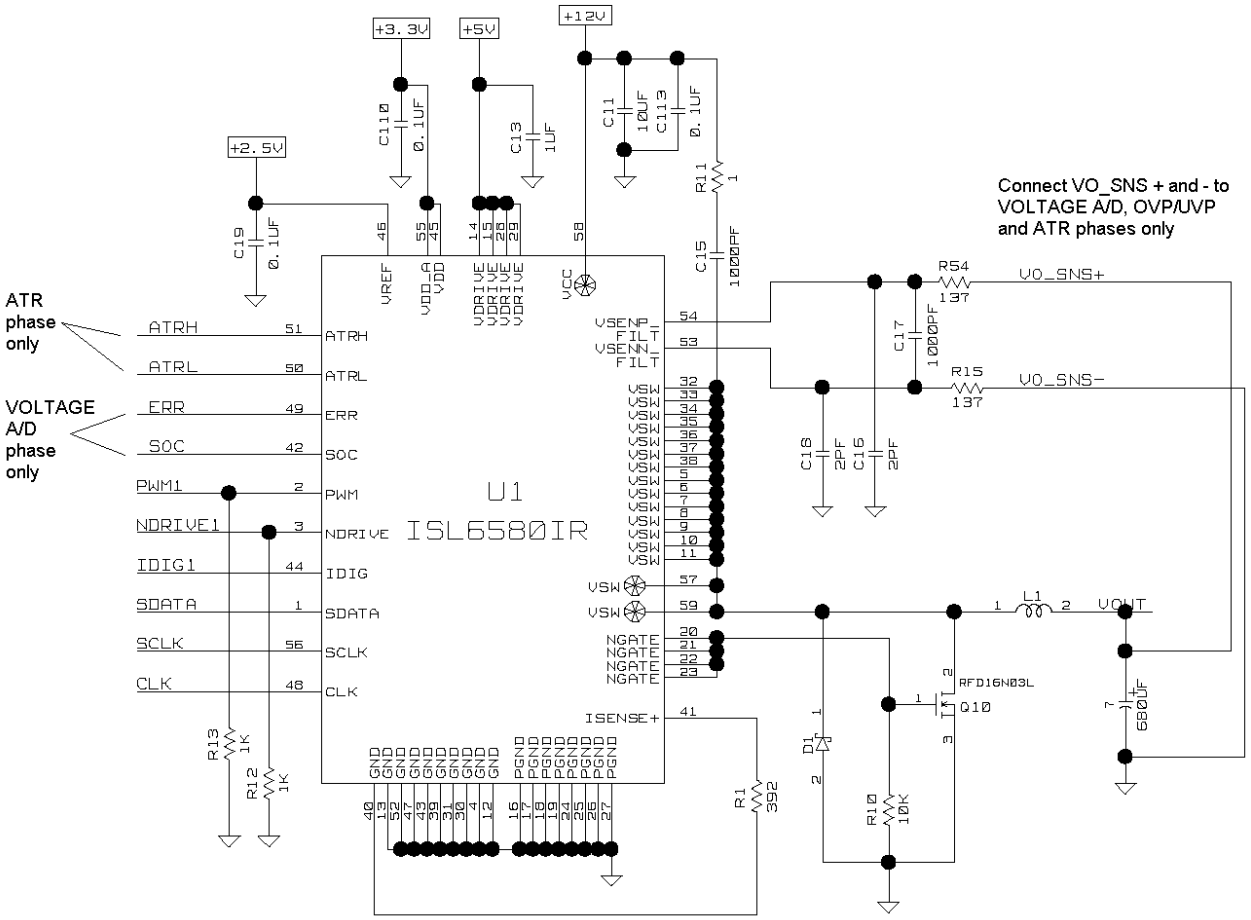
Related Literature

- ISL6590 Datasheet
- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB379 “Thermal Characterization of Packaged Semiconductor Devices”
- Technical Brief TB389 “PCB Land Pattern Design and Surface Mount Guidelines for QFN (MLFP) Packages”

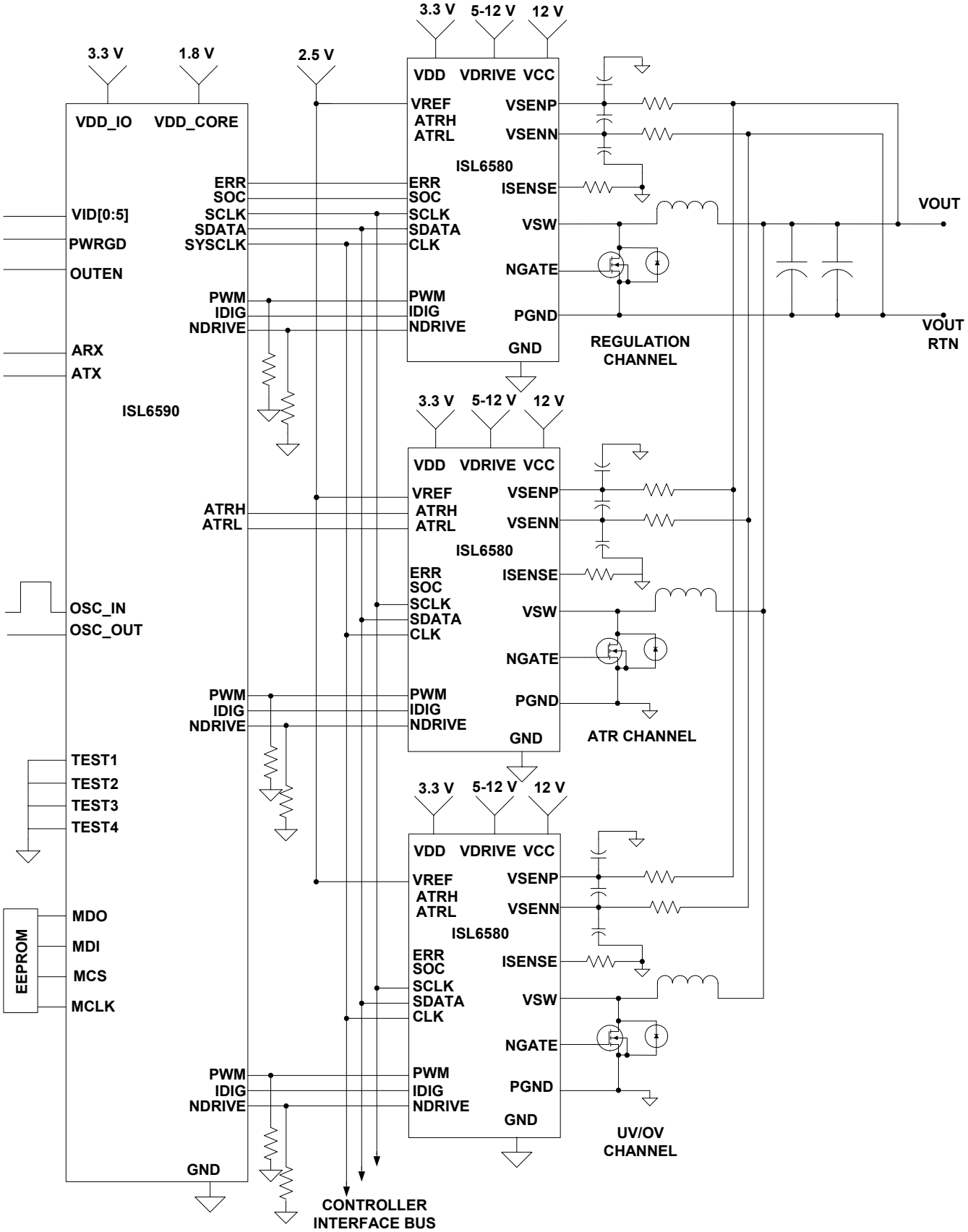
Block Diagram



Typical Power Stage Schematic



Typical Application



Functional Pin Description

PIN #	NAME	I/O	TYPE	DESCRIPTION
1	SDATA	I/O	3.3V CMOS	Digital I/O; serial data line that carries configuration and monitoring information to and from the Intersil ISL6590 digital controller via the shared controller interface bus. Information transmitted via SDATA includes: PVID information, input UVLO fault, output under/over voltage fault, thermal shutdown fault, peak current limit setpoint, ATRH and ATRL trip levels
2	PWM	I	3.3V CMOS	Digital input; pulse width modulation input to the high side driver.
3	NDRIVE	I	3.3V CMOS	Digital input; multifunction pin used for assigning device ID at startup. During operation, provides pulse width modulation for the low side driver
4	GND	I	GND	IC ground
5	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high and no fault condition, VCC is switched to VSW
6	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high and no fault condition, VCC is switched to VSW
7	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high and no fault condition, VCC is switched to VSW
8	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high and no fault condition, VCC is switched to VSW
9	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high and no fault condition, VCC is switched to VSW
10	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high and no fault condition, VCC is switched to VSW
11	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high and no fault condition, VCC is switched to VSW
12	GND	I	GND	IC ground
13	GND	I	GND	IC ground
14	VDRIVE	I	VDRIVE	Power input typically connected to a 5V supply. Provides the supply voltage for driving the gate of the Low side NFET
15	VDRIVE	I	VDRIVE	Power input typically connected to a 5V supply. Provides the supply voltage for driving the gate of the Low side NFET
16	GND	I	GND	IC ground
17	GND	I	GND	IC ground
18	GND	I	GND	IC ground
19	GND	I	GND	IC ground
20	NGATE	O	HV ANALOG	High voltage analog output used to drive the low side NFET. When NDRIVE is high, NGATE is switched to VDRIVE. When NDRIVE is low, NGATE is switched to ground.
21	NGATE	O	HV ANALOG	High voltage analog output used to drive the low side NFET. When NDRIVE is high, NGATE is switched to VDRIVE. When NDRIVE is low, NGATE is switched to ground.
22	NGATE	O	HV ANALOG	High voltage analog output used to drive the low side NFET. When NDRIVE is high, NGATE is switched to VDRIVE. When NDRIVE is low, NGATE is switched to ground.
23	NGATE	O	HV ANALOG	High voltage analog output used to drive the low side NFET. When NDRIVE is high, NGATE is switched to VDRIVE. When NDRIVE is low, NGATE is switched to ground.
24	GND	I	GND	IC ground
25	GND	I	GND	IC ground
26	GND	I	GND	IC ground
27	GND	I	GND	IC ground
28	VDRIVE	I	VDRIVE	Power input typically connected to a 5V supply. Provides the supply voltage for driving the gate of the low side NFET
29	VDRIVE	I	VDRIVE	Power input typically connected to a 5V supply. Provides the supply voltage for driving the gate of the low side NFET
30	GND	I	GND	IC ground
31	GND	I	GND	IC ground
32	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high and no fault condition, VCC is switched to VSW

Functional Pin Description (Continued)

PIN #	NAME	I/O	TYPE	DESCRIPTION
33	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high and no fault condition, VCC is switched to VSW
34	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high and no fault condition, VCC is switched to VSW
35	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high and no fault condition, VCC is switched to VSW
36	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high and no fault condition, VCC is switched to VSW
37	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high and no fault condition, VCC is switched to VSW
38	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high and no fault condition, VCC is switched to VSW
39	GND	I	GND	IC ground
40	ISENSE MINUS/ GND	I	GND	Ground pin for current sense resistor
41	ISENSE PLUS	I/O	ANALOG	Low voltage analog output; current representing 1/9900 of the high side PFET current
42	SOC	O	3.3V CMOS	Digital outupt; start of conversion signal (SOC). This signal frames the error word generated by the voltage A/D when configured in regulation mode.
43	GND	I	GND	IC ground
44	IDIG	O	3.3V CMOS	Digital output; 7 bit serial word transmitted typically at 66.67MHz. The first bit is a start bit (start=1). This signal represents the sampled peak current in the high side PFET, MSB first
45	VDD	I	VDD	Power supply for the logic typically set at 3.3V
46	VREF	I	VREF	Low voltage analog input; 2.5V reference signal used by the A/D converter and the thermal shutdown circuits
47	GND	I	GND	IC ground
48	CLK	I	3.3V CMOS	Digital input; typically a 133MHz clock supplied to the Intersil ISL6590
49	ERR	O	3.3V CMOS	Digital output; Voltage A/D output word indicating the error from the desired output voltage and VSENP-VSENN measured voltage (Output voltage-VID). The error signal is a 6 bit serial word (MSB first) transmitted typically at 66.67MHz.
50	ATRL	O	3.3V CMOS	Digital output; Active Transient Response Low (ATRL). ATRL indicates the regulated output voltage has"spiked" above the programmed level.
51	ATRH	O	3.3V CMOS	Digital output; Active Transient Response High (ATRH). ATRH indicates the regulated output voltage has"drooped" below the programmed level.
52	GND	I	GND	IC ground
53	VSENN	I	LV ANALOG	Low voltage analog input; negative input for the remote sense used to differentially sense the regulated output voltage. The IC is configurable for thre modes of operation: Regulation mode, ATR mode, and output OV/UV mode
54	VSENP	I	LV ANALOG	Low voltage analog input; positive input for the remote sense used to differentially sense the regulated output voltage. The IC is configurable for thre modes of operation: Regulation mode, ATR mode, and output OV/UV mode
55	VDD	I	VDD	Power supply for the logic typically set at 3.3V
56	SCLK	I	3.3V CMOS	Digital input; typically 16.67MHz clock supplied by the Intersil ISL6590 digital controller for the controller interface bus Paddle
PADDLE	VCC	I	VCC	Power supply input typically set at 12V. Provides gate drive and source connection for the integrated high side PFET
Side Bar 1	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high, VCC is switched to VSW
Side Bar 2	VSW	O	HV ANALOG	Drain of high side PFET. When the PWM signal is high, VCC is switched to VSW

Absolute Maximum Ratings

V_{CC} . . . . . -0.3V to 18V
V_{DD} . . . . . -0.3V to 3.6V
V_{REF} (see Note 1) . . . . . -0.3V to V_{DD}
V_{DRIVE} (see Note 1) . . . . . -0.3V to V_{CC}
V_{CC}-V_{SW} (PChannel VBRSS). 20V
ISW peak 35A
ICC average. 3.5A
MOSFET Gate Capacitance . . . . . See Max Gate Drive section
All Logic . . . . . -0.3V to 3.6V
VSENN, VSENP . . . . . -0.3V to 3.6V
ESD Rating
Human Body Model (Per JEDEC JESD22-A114) 1.5KV

Operating Conditions

Temperature Range . . . . . 0^oC to 85^oC
V_{CC} (Typical) 12V
V_{DD} (Typical) 3.3V
V_{DRIVE} (Typical) 5V
V_{REF} (Typical) 2.5V

Thermal Information

Thermal Resistance	θ_{JA}(^oC/W)	θ_{JB}(^oC/W)	θ_{JC}(^oC/W)
Junction to bottom of case	N/A	N/A	3
Junction to top of case	N/A	N/A	12.0
Junction to board (Note 2)	N/A	9	N/A
Still air (Note 2)	26.0	N/A	N/A
100LFM (Note 2)	23.5	N/A	N/A
200LFM (Note 2)	22.3	N/A	N/A
400LFM (Note 2)	21.2	N/A	N/A

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range. . . . . -65^oC to 175^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. See "Bias Supply Power On Sequence" section.
2. θ_{JA} is measured with the component mounted on a "High Effective" Thermal Conductivity Board with "Direct Attach" Features. See Technical Brief TB379 "Thermal Characterization of Packaged Semiconductor Devices".

Electrical Specifications

V_{DD} = 3.3VDC, V_{CC} = 12VDC, V_{DRIVE} = 5VDC, V_{REF} = 2.5V, SYSCLK = 133.33MHz, SCLK = 16.67MHz, T_A = 25°C Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER STAGE					
SWITCHING FREQUENCY					
Switching Frequency	Switching Frequency Range	0.25		1	MHz
POWER STAGE: NGATE					
NGATE SIGNAL PARAMETERS; V_{DRIVE} = 5VDC					
NGATE Voltage	Voltage Swing for Driving External NFET (I_{DRIVE} = 2A)		5		V
NGATE Pullup Resistance	Pullup Resistance of ISL6580 for Biasing gate of External, Synchronous Rectifier, N Channel MOSFETs		1.3		Ω
NGATE Pulldown Resistance	Pulldown Resistance of ISL6580 for Biasing gate of External, Synchronous Rectifier, N Channel MOSFETs		0.4		Ω
Gate Rise Time	Gate Rise Time of External NFET, Transition from 0.5 to 4.5V; into 3nF		8		ns
Gate Fall Time	Gate Fall Time of External NFET Transition from 4.5 to 0.5V; into 3nF		4		ns
Turn on Delay Time	C_{LOAD} = 3nF		25		ns
POWER STAGE: INTERNAL P CHANNEL, HIGH SIDE SWITCH PARAMETERS					
P Channel RDS(on)	Static Drain-to-Source ON resistance of Internal P Channel FET, ID =10 amps; Measured between V_{CC} and V_{SW} pins		20		mΩ
P Channel V_{BRSS}	Switch breakdown voltage of internal P Channel FET. ID = 1.5 mA		20		V

Electrical Specifications V_{DD} = 3.3VDC, V_{CC} = 12VDC, V_{DRIVE} = 5VDC, V_{REF} = 2.5V, SYSCLK = 133.33MHz, SCLK = 16.67MHz, T_A = 25°C Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC SIGNALS					
LOGIC SIGNAL EXPECTED RANGES (PWM, SCLK, SDATA, SOC, CLK, NDRIVE)					
HIGH voltage	Logic Level HIGH Voltage Range	2.0			V
LOW voltage	Logic Level LOW Voltage Range			0.8	V
HIGH current	Output source current HIGH	-5.0	-20		mA
LOW current	Output sink Current LOW	5.0	20		mA
INPUT LOGIC CURRENT REQUIREMENTS (CLK, SCLK, NDRIVE)					
I_{IH}	Input High Current	1.7		2.7	mA
I_{IL}	Input Low Current	1.7		2.7	mA
MASTER CLOCK (CLK)					
Frequency	Master clock frequency		133		MHz
R	Input pull up and pull down resistance	1335	1907	2480	Ω
VOLTAGE A/D CONVERTER **Note: DC accuracy of Voltage A/D is by reference** (Output = ERR = 6 bit, serial data word, MSB first, 66MHz clock frequency)					
INPUT SENSE SIGNALS					
VSENP	Positive Core Voltage of the Processor (filtered); RL = 10kΩ, -400µA current draw	0.3		Vdd	V
VSENN	Return Core Voltage of the Processor (filtered); RL = 10kΩ, -400µA current draw	-0.3		0.3	V
VSENP-VSENN	Differential Return Core Voltage of the Processor (filtered); RL = 10kΩ, -400µA current draw	.3		1.8875	V
I VSENP	Current into the VSENP pin	-240		240	uA
I VSENN	Current into the VSENNP pin	-10		10	uA
REGULATION ERROR STEPS					
ERR regulation step	Voltage increment step per LSB (Over regulation range of 0.3 to 1.85VDC)		4.167		mV
ERR window	Voltage window of ERR signal.	-133		+128.83	mV
DC ACCURACY					
Resolution	Any Channel; Minimum Resolution for which No Missing Codes are Guaranteed	6			Bits
Differential Nonlinearity	Any Channel; LSB max		± 1		Bits
Integral Nonlinearity	Any Channel; LSB max		± 1		Bits
Gain Error	Any Channel; LSB max		± 1		Bits
Offset Error	Any Channel; LSB max		± 1		Bits

Electrical Specifications V_{DD} = 3.3VDC, V_{CC} = 12VDC, V_{DRIVE} = 5VDC, V_{REF} = 2.5V, SYSCLK = 133.33MHz, SCLK = 16.67MHz, T_A = 25°C Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT A/D CONVERTER (Output = I_{DIG} = 7-bit serial signal, first bit = START bit, 6 bit current word length (MSB first), 66MHz clock frequency)					
CURRENT INFORMATION STEP					
I_{SENSE} step	Incremental step per LSB of voltage at I_{SENSE} pin (I_{SENSE} * R_{SENSE})		19.5		mV
I_{SENSE} range	Voltage on the I_{SENSE} pin that produces full scale output from the I_{SENSE} A/D			1.25	V
DC ACCURACY					
Resolution	Any Channel; Minimum Resolution for which No Missing Codes are Guaranteed	6			Bits
Differential Nonlinearity	Any Channel; LSB max		± 1		Bits
Integral Nonlinearity	Any Channel; LSB max		± 1		Bits
Gain Error	Any Channel; LSB max		± 1		Bits
Offset Error	Any Channel; LSB max		± 1		Bits
P CHANNEL DRAIN CURRENT SENSE (I_{SENSE})					
I_{SENSE} ratio	Ratio of V_{SW} current to I_{SENSE} current		9900		
WINDOW COMPARATOR					
ACTIVE TRANSIENT RESPONSE (ATR) CONFIGURATION VALUES (sensed at the processor load)					
t_{ATR}	ATRL and ATRH signal delay		10		ns
OUTPUT UNDER VOLTAGE/ OVER VOLTAGE RANGE OF CONFIGURATION VALUES					
Over Voltage	Range of adjustment of the Over Voltage threshhold	0	+150	232	mV
Under Voltage	Range of adjustment of the Under Voltage threshhold	-232	-150	0	mV
INPUT UNDER VOLTAGE PROTECTION VALUES When VCC is below the threshold a comparator (with hysteresis) sets a bit in the fault register. The digital controller reads the fault register and sets PWM and NDRIVE to ground if IUVP is enabled and the fault bit is set.					
Vtlh	V_{CC} Threshold, low to high (sweep Vcc from 6V to 10V).	8.6	9.1	9.6	V
Vthl	V_{CC} Threshold, high to low (sweep Vcc from 10V to 6V).	7.0	7.6	8.2	V
Vtlh-Vthl	V_{CC} Threshold hysteresis, low to high to low (sweep V_{CC} 6V to 10V to 6V).	1.35	1.5	1.65	V
Idd	V_{DD} current (V_{DD} = 3.3V)		8.5		mA
Iref	V_{REF} current (V_{REF} = 2.5V)		1.3		mA
PROGRAMMABLE FUNCTIONS					
CURRENT LIMIT (VOLTAGE ON THE I_{SENSE} PIN THAT TRIP THE PULSE BY PULSE CURRENT LIMIT)					
Step	adjustment step size		0.2		V
Range	Range of adjustment	.8		1.4	V
Default	Current Limit Default		1.0		V
TEMPERATURE SENSE (JUNCTION TEMPERATURE THAT SETS THE OVER TEMPERATURE REGISTER)					
Step	Temperature Sense Step		10		°C
Range	Over Temperature adjustment Range	85		145	°C
Default	Over Temperature Default		145		°C

Electrical Specifications V_{DD} = 3.3VDC, V_{CC} = 12VDC, V_{DRIVE} = 5VDC, V_{REF} = 2.5V, SYSCLK = 133.33MHz, SCLK = 16.67MHz, T_A = 25°C Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ATRH (ACTIVE TRANSIENT RESPONSE HIGH)					
Step	ATRH Step		-7.5		mV
Range	ATRH adjustment Range	-233		0	mV
Default	Address Register Default		-67.5		mV
ATRL (ACTIVE TRANSIENT RESPONSE LOW)					
Step	ATRL Step		7.5		mV
Range	ATRL adjustment Range	0		233	mV
Default	ATRL Default		75		mV
VID STEP					
Step	VID Step		12.5		mV
Range	VID Range	.8325		1.6	V

Multi-Phase Power Conversion

Microprocessor load current profiles have changed to the point where the multi-phase power conversion advantage is pronounced. The technical challenges associated with producing a single-phase converter which is both cost-effective and thermally viable have forced a change to the cost-saving approach of multi-phase. The ISL6590 controller and ISL6580 Power Stages help reduce the complexity of implementation by integrating vital functions and requiring minimal output components. The *Typical Application Drawing* provides a top level view of multi-phase power conversion using the ISL6590 and ISL6580. The *Typical Application Drawing* and the waveforms below describe a 3 phase converter. The ISL6590 can control up to 6 interleaved phases.

Interleaving

The switching of each channel in a multi-phase converter is timed to be symmetrically out of phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the three-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

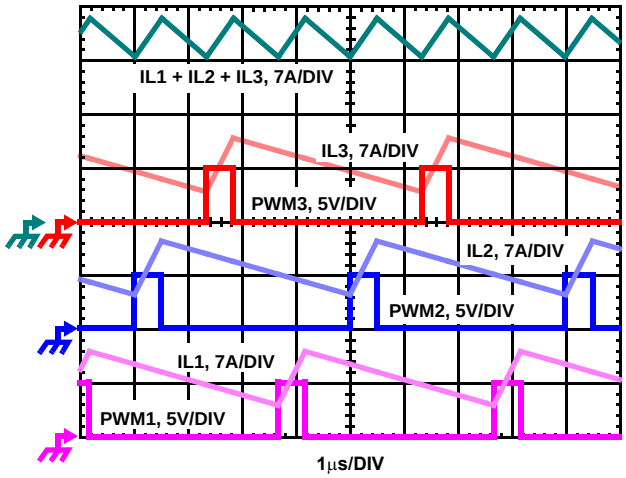


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

Figure 1 illustrates the multiplicative effect on output ripple frequency. The three channel currents (IL1, IL2, and IL3), combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. The peak-to-peak current waveforms for each phase is about 7A, and the dc components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multi-phase circuit, examine the equation representing an individual channel's peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{Lf_S V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multi-phase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output-voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C,PP} = \frac{(V_{IN} - N\,V_{OUT})V_{OUT}}{Lf_S V_{IN}} \quad \text{(EQ. 2)}$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multi-phase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 2 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

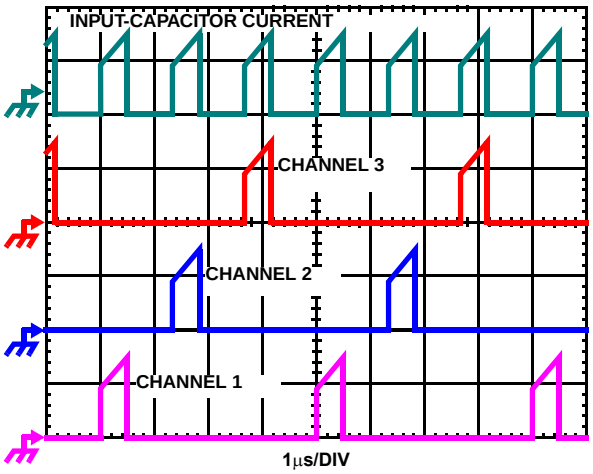


FIGURE 2. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

The converter depicted in Figure 2 delivers 36A to a 1.5V load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has 11.9A RMS input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

Voltage Control Loop

One of the ISL6580 power stages in a multiphase converter is used for voltage feed back. Output voltage is fed back to this power stage which subtracts the reference voltage (based on VID, see the VID table below) and converts the error voltage to a binary number. The digital error number is sent to the controller on the ERR line. The controller adds offset proportional to the load current for the load line (see next section on AVP) and passes the error number to the digital Proportional, Integral, Derivative (PID) compensator. The PID compensator is described in detail in a later section. Output from the PID compensator drives the 6 phase digital Pulse Width Modulator which produces the 6 PWM and DRIVE signals that control switching of the power MOSFETs.

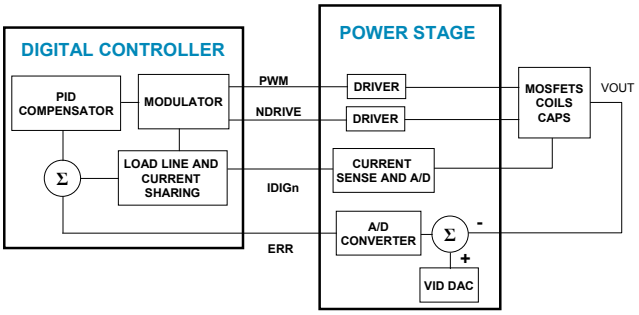


FIGURE 3. VOLTAGE CONTROL LOOP BLOCK DIAGRAM

Voltage Identification Codes (VID)

V_{OUT} (V)	VID4	VID3	VID2	VID1	VID0	VID5
0.8375	0	1	0	1	0	0
0.8500	0	1	0	0	1	1
0.8625	0	1	0	0	1	0
0.8750	0	1	0	0	0	1
0.8875	0	1	0	0	0	0
0.9000	0	0	1	1	1	1
0.9125	0	0	1	1	1	0
0.9250	0	0	1	1	0	1
0.9375	0	0	1	1	0	0
0.9500	0	0	1	0	1	1
0.9625	0	0	1	0	1	0
0.9750	0	0	1	0	0	1
0.9875	0	0	1	0	0	0
1.0000	0	0	0	1	1	1
1.0125	0	0	0	1	1	0
1.0250	0	0	0	1	0	1
1.0375	0	0	0	1	0	0
1.0500	0	0	0	0	1	1
1.0625	0	0	0	0	1	0
1.0750	0	0	0	0	0	1
1.0875	0	0	0	0	0	0
OFF	1	1	1	1	1	1
OFF	1	1	1	1	1	0
1.1000	1	1	1	1	0	1
1.1125	1	1	1	1	0	0
1.1250	1	1	1	0	1	1
1.1375	1	1	1	0	1	0
1.1500	1	1	1	0	0	1
1.1625	1	1	1	0	0	0
1.1750	1	1	0	1	1	1
1.1875	1	1	0	1	1	0
1.2000	1	1	0	1	0	1
1.2125	1	1	0	1	0	0
1.2250	1	1	0	0	1	1
1.2375	1	1	0	0	1	0
1.2500	1	1	0	0	0	1
1.2625	1	1	1	0	0	0
1.2750	1	0	1	1	1	1
1.2875	1	0	1	1	1	0
1.3000	1	0	1	1	0	1
1.3125	1	0	1	1	0	0
1.3250	1	0	1	0	1	1
1.3375	1	0	1	0	1	0
1.3500	1	0	1	0	0	1
1.3625	1	0	0	0	0	0
1.3750	1	0	0	1	1	1
1.3875	1	0	0	1	1	0
1.4000	1	0	0	1	0	1
1.4125	1	0	0	1	0	0
1.4250	1	0	0	0	1	1
1.4375	1	0	0	0	1	0
1.4500	1	0	0	0	0	1
1.4625	1	0	1	0	0	0
1.4750	0	1	1	1	1	1
1.4875	0	1	1	1	1	0
1.5000	0	1	1	1	0	1
1.5125	0	1	1	1	0	0
1.5250	0	1	1	0	1	1
1.5375	0	1	1	0	1	0
1.5500	0	1	1	0	0	1
1.5625	0	1	0	0	0	0
1.5750	0	1	0	1	1	1
1.5875	0	1	0	1	1	0
1.6000	0	1	0	1	0	1

AVP (Adaptive Voltage Positioning)

Load Line Specifications

Recent Voltage Regulator specs require the regulated output voltage to decrease as load current increases as it would with a small output resistance (~0.5 to 1.5mΩ). A typical (VRD10) specification for output voltage is:

$Vout\_max = V_{VID} - Iload*.00135$

$Vout\_min = V_{VID} - 0.04V - Iload*0.00135$

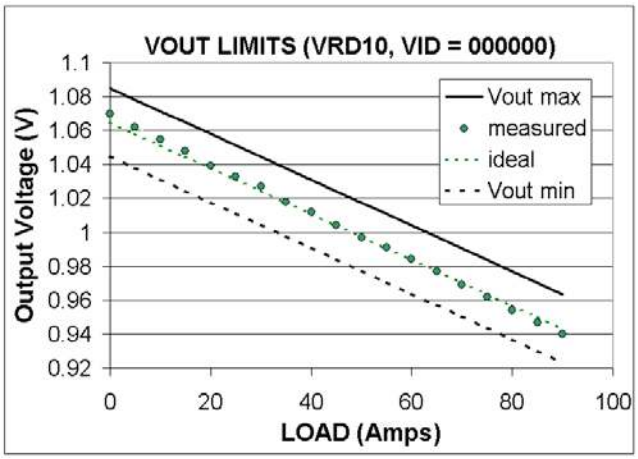


FIGURE 4. TYPICAL LOAD LINE SPECS (VRD10) AND THE AFFECT OF AVP LOAD LINE SETTINGS

V_{VID} is the maximum output voltage at 0 load. It is set by a 5 or 6 bit binary input to the voltage regulator called VID (Voltage ID). For VRD10, VID = 100011 indicates V_{OUT} max = 1.000V. The slope of the load line is different for other applications. For VRM 9, Vout_max = V_{VID} – Iload*.00095. The slope and offset from V_{VID} is adjustable in the ISL6580 / ISL6590 using the user interface software. See the User Interface Software section.

The ISL6580 / ISL6590 realize this behavior in a programmable, lossless way. Load current is measured in each ISL6580 output stage. A fraction (1/9900) of the current in the upper MOSFET is mirrored and sent through an external resistor. The voltage on the current sense resistor is sampled near the end of the upper FET's ON time, converted to a digital number and sent to the ISL6590 controller on the IDIGn line (see Figure 5). Current sensing is described in more detail in the next section.

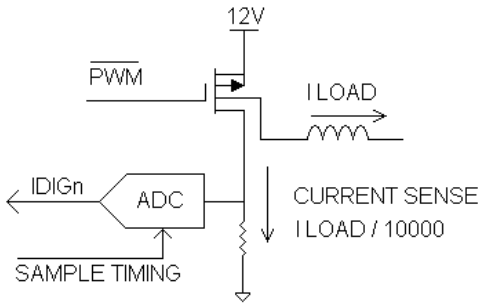


FIGURE 5. CURRENT SENSE BLOCK DIAGRAM

The sum of all power device currents is multiplied by a gain factor, passed through a digital low pass filter and added to the error voltage (see Figure 6).

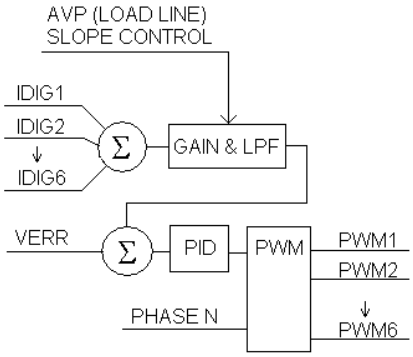


FIGURE 6. AVP LOAD LINE CONTROL IS ADDED TO THE ERROR SIGNAL

The gain factor controls how much the output voltage 'droops' and is set by the system designer using the user interface software. The user interface software calculates a number of internal register values based on data in the Large Signal Design, Inputs window. All values on the Inputs window must be entered correctly for the AVP loadline to be programmed correctly to the controller.

The user interface software will generate a plot of the loadline. It is viewed by clicking on the AVP line button at the bottom of all of the user interface software windows.

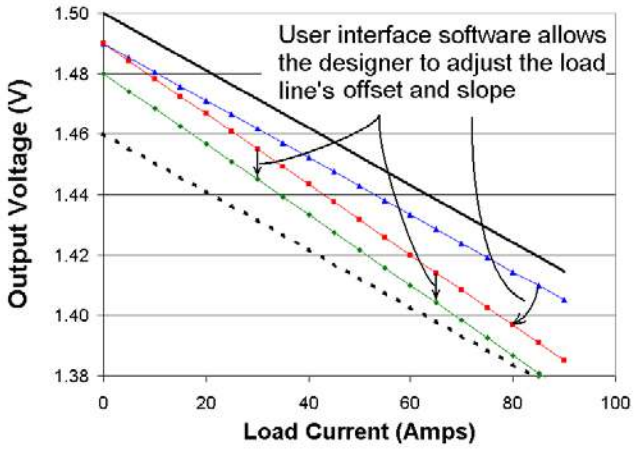


FIGURE 7. USER INTERFACE LOAD LINE ADJUSTMENTS

AVP offset moves the load line relative to the voltage required by the input VID. It can be adjusted from 0 to 50mV in steps of 3.125mV. AVP LoadLine controls the slope of the load line. This gives the designer complete flexibility within the specified "max" and "min" limits.

Current Sensing

Current sensing is a key feature in the Intersil Digital Architecture. Precision current sensing is required to maintain accurate load lines, good current sense balancing between phases, thermal balancing, overload current, and peak current limit protection.

By integrating the high side MOSFET in the power stage of the Intersil Digital Architecture (see Figure 8), very accurate current sensing can be achieved across temperature. This method of current sense through integration is called current mirroring. A current mirror simply designates a certain ratio of transistors on the silicon of FET to have a separate source output but a common drain node. As a result, a small current sample from the FET can be drawn external to the power stage and through a sense resistor. Voltage across the sense resistor represents the total current through the High Side FET. Since the mirror is using the same silicon as the main current path, variations in Rdson and switching characteristics mirror that of the main FET channel. The internal structure of the sampling circuitry is seen in Figure 8.

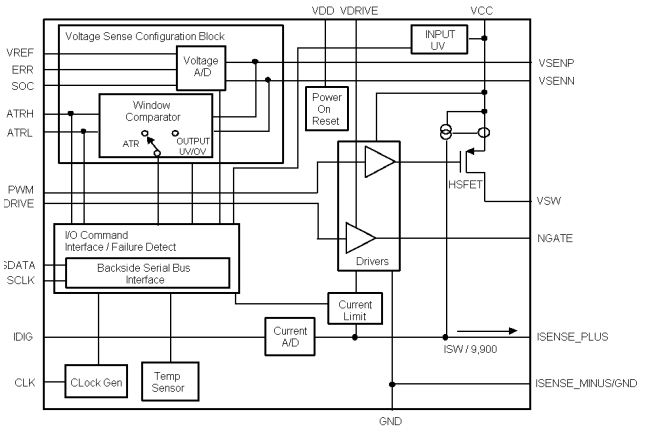


FIGURE 8. INTERNAL STRUCTURE OF THE ISL6580 POWER STAGE

A sample of the peak current through the MOSFET is taken each clock cycle, converted to a digital signal, and sent to the controller. The master oscillator frequency inside the Intersil Digital Architecture is 133.33MHz. Figure 9 shows the voltage drop across the sense resistor, the voltage at the switch node, the inductor current, and the digital voltage signal. The inductor current signal is delayed slightly due to the probe parasitics. As can be seen from the figure, 13nS prior to the turn off of the high side MOSFET a sample of the voltage across the sense resistor is taken (I_{SENSE}). This is done to avoid voltage spiking during the switching of the node. After sampling, I_{SENSE} is converted to a digital signal (I_{DIG}). The controller receives the digital signal from the I_{DIG} pin.

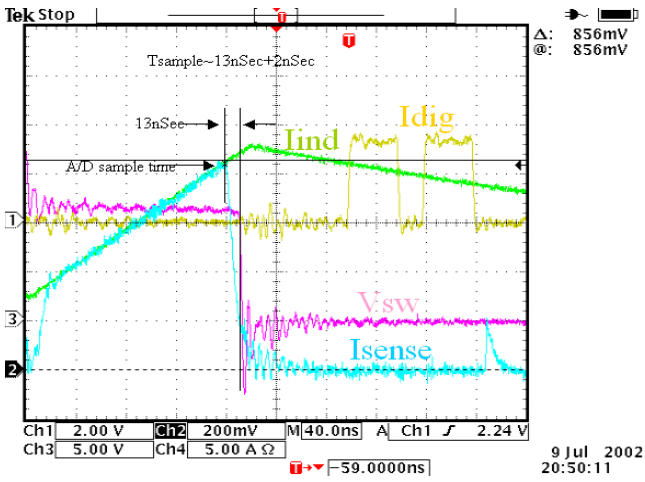


FIGURE 9. VOLTAGE DROP ACROSS THE SENSE RESISTOR, VOLTAGE AT SWITCH NODE, INDUCTOR CURRENT, AND DIGITAL VOLTAGE SIGNAL

Current Sharing

Each ISL6580 senses current in it's upper MOSFET as described above and converts it to a serial digital signal on the IDIGn lines. The sampled, digitized current, $IDIG_n$, from each active channel is used to gauge both overall load current and the relative channel current carried in each leg of the converter. The individual sample currents are summed and divided by the number of active channels. The resulting average current, I_{AVG}, provides a measure of the total load current demand on the converter and the appropriate level of channel current. The average current is then subtracted from the individual channel sample currents. The resulting error current, I_{ER}, is then filtered before it adjusts V_{COMP}. The modified V_{COMP} signal is compared to a sawtooth ramp signal and produces a pulse width which corrects for any unbalance and drives the error current toward zero.

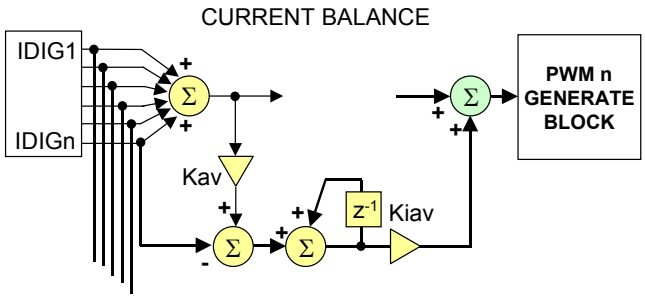


FIGURE 10. CURRENT BALANCE

Loop Compensation

Any closed loop system must be designed to insure stability (prevent oscillation) and provide correct response to external events such as load transients. The output of a buck regulator has an inherent, low pass filter formed by the output inductor(s), output capacitance and their ESRs (Equivalent Series Resistance). Figure 1 shows a typical gain and phase plot of output inductors, capacitors and ESR.

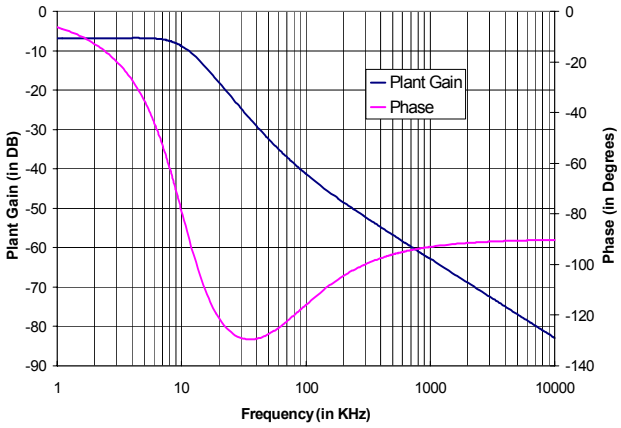


FIGURE 11. FREQUENCY RESPONSE OF THE OUTPUT INDUCTORS AND CAPACITORS

Above the resonant frequency of the output LC filter (10kHz in this case) the gain falls at a rate of 40dB/decade and the phase shift approaches –180 degrees. At a frequency above the F = 1/(2ðC*ESR) = 500kHz in this case) the gain slope changes to –20dB/decade and the phase shift approaches –90 degrees.

In a closed loop control system, the output is subtracted from a reference voltage to produce an error voltage. The error voltage is amplified and fed to the output stage. In a buck regulator the output stage consists of a Pulse Width Modulator (PWM), switching transistors (typically MOSFETs), series inductor(s) and output capacitors. High gain feedback reduces variation in the output due to changes in input voltage, load current and component values. However, high gain at high frequencies can cause excessive over shoot in response to transients (if phase shift > 120 degrees and gain > 0dB) or oscillation (if phase shift > 180 degrees and gain > 0dB). The trade off in designing the loop compensation is to achieve fast response to transients without excessive overshoot or oscillation.

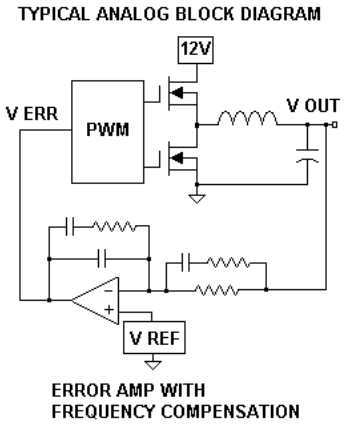


FIGURE 12. TYPICAL ANALOG VOLTAGE LOOP BLOCK DIAGRAM

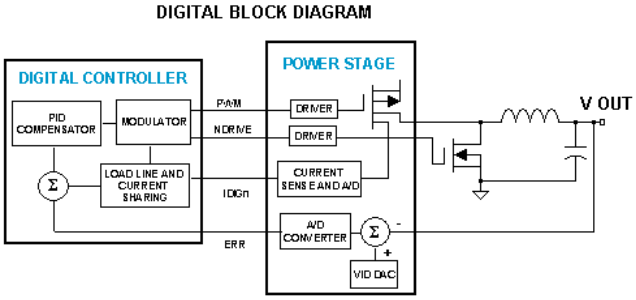


FIGURE 13. DIGITAL CONTROL LOOP BLOCK DIAGRAM

The ISL6580 subtracts a reference from the output voltage to produce an error voltage. It converts the error voltage to a 6 bit digital number and sends it to the ISL6590 controller. The controller processes the error number numerically to provide gain (Proportional), phase lag (Integration) and phase lead (Derivative) functions. This forms the digital PID control.

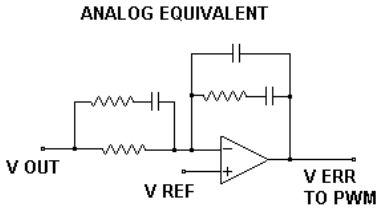


FIGURE 14. TYPICAL ANALOG ERROR AMPLIFIER AND COMPENSATION

Adjusting The Digital PID

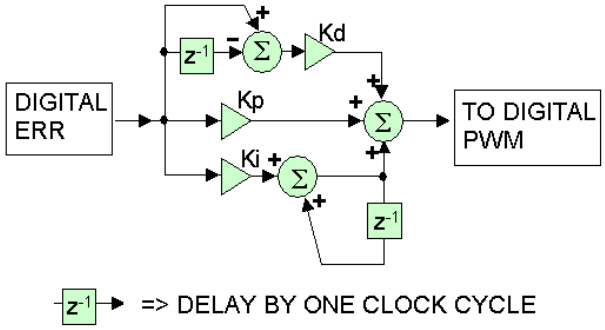


FIGURE 15. DIGITAL PID COMPENSATOR

Frequency response of the digital PID compensator is determined by the Kp, Ki, Kd factors. These factors are stored in nonvolatile memory and are loaded in the controller at power on reset. The system designer sets the PID compensators frequency response using user interface software. The designer enters the frequencies of the desired poles and zeros and user interface software calculates the Kp, Ki and Kd factors. the software will calculate and display the frequency response of the feedback and the closed loop system.

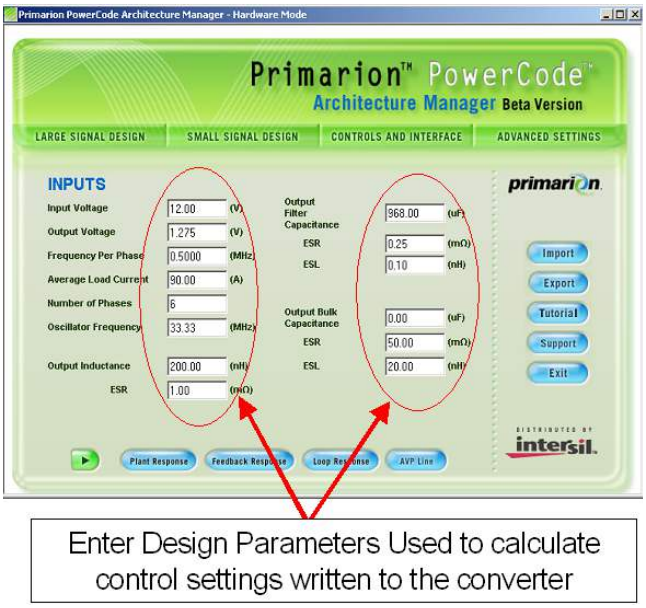


FIGURE 16. DESIGN PARAMETER INPUT WINDOW

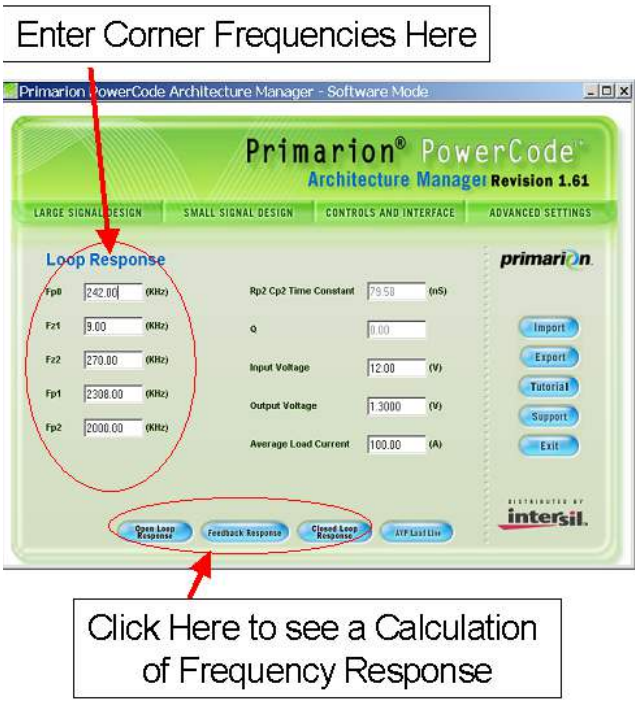


FIGURE 17. SMALL SIGNAL DESIGN WINDOW

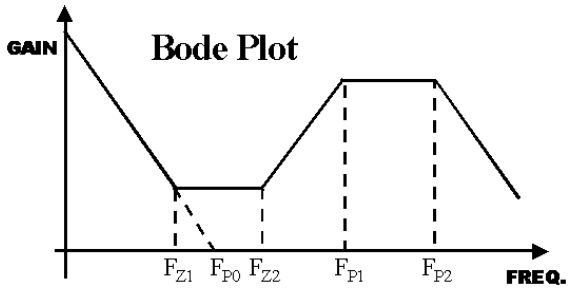


FIGURE 18. BODE PLOT

F_{Z1} = Frequency of first zero

F_{Z2} = Frequency of second zero

F_{P0} = Gain * frequency of first pole (A_{DC}*F_{P0})

F_{P1} = Frequency of second pole

R_{P2} = External Resistor used for third pole

C_{P2} = External Capacitor used for third pole

$F_{P2} = 1 / (2 * ð * R_{P2} * C_{P2})$

The software will calculate the frequency response of the PID controller and the closed loop system as in figures 19 and 20 below.

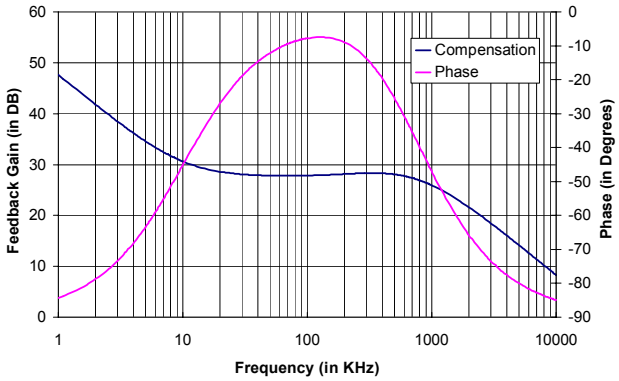


FIGURE 19. PID COMPENSATOR FREQUENCY RESPONSE

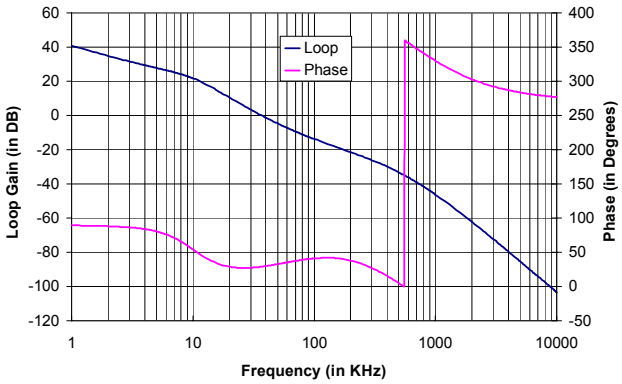


FIGURE 20. FREQUENCY RESPONSE OF THE CLOSED LOOP

Compensation Methodology

Due to the user interface software interface, it is very easy to change the frequency compensation and see the resulting performance on a scope or network analyzer. Transient response is viewed by applying a transient load and monitoring the output voltage with a scope. Frequency response is viewed by placing a small resistor between the output and the feed back network, applying a small sine wave at the input to the feed back network and measuring the amplitude and phase shift of the resulting sine wave on the output. Sweeping the frequency produces plots similar to those above.

Frequency Domain

It is recommended to place the first zero (F_{Z1}) at the resonant frequency of the output inductors and capacitors (F = 1/(2ð÷LC = 10kHz in this case). Then increase F_{Z2} and F_{P0} to maximize DC gain and the frequency at which gain drops below 0dB while keeping the phase margin above 60 degrees. Phase Margin is the difference between 180 degrees and the phase shift of the loop at the frequency where the gain drops below 0dB (cross over frequency). If the loops phase shift reaches 180 degrees and has gain equal to or greater than 0dB, it acts as positive feed back and the loop will oscillate. Even if the loops phase shift is slightly below 180 degrees at the cross over frequency, the loop will respond to transients with overshoot and ringing. Loop phase shift between 90 and 120 degrees at the cross over frequency (Phase margin = 60 to 90 degrees) results in little or no over shoot and ringing. Large phase margins (>90 degrees) result in slower transient response.

Time Domain

It is recommended to place the first zero (F_{Z1}) at the resonant frequency of the output inductors and capacitors (F = 1/(2ð÷LC = 10kHz in this case). Then increase F_{Z2} and F_{P0} to minimize response time over (under) shoot and ringing. The first microseconds of transient response are primarily dependant on the ESR and ESL of the output capacitors. After the affects of ESL and ESR pass the loop must control the response.

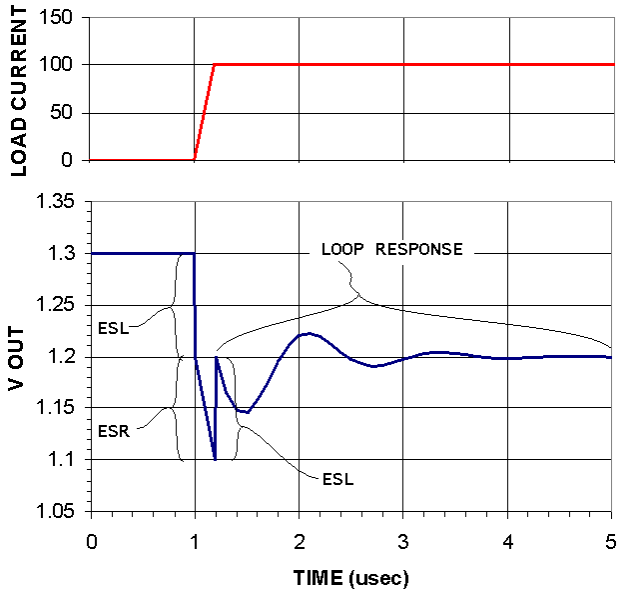


FIGURE 21. TYPICAL RESPONSE TO A LOAD TRANSIENT

Active Transient Response

What is ATR?

In ordinary operation, the ISL6590 and the ISL6580's form a closed-loop system that uses enhanced proportional, integral, differential (PID) control to converge on a target output voltage. The control loop monitors the delivered load current and adjusts the pulse-width modulated impulses accordingly to satisfy the load line. Fast load current transitions, however, may produce brief under- or overshoots in the output voltage. The closed loop may fail to compensate rapidly for these events for several reasons: 1) it has limited bandwidth, 2) it has processing delay, 3) the inductors require time to (dis)charge the output capacitor bank, and 4) the slew rate of the output current may be extremely fast.

Active transient response (ATR) is engaged if the output voltage deviates outside a user-defined voltage window. In this mode, all ISL6580's may be switched simultaneously as an open-loop system.

In ordinary operation, the switching of ISL6580 phases is distributed uniformly in time. An *n*-phase system, for example, has successive phases delayed by *tp*/*n*, where *tp* is the switching period. ATR mode, in addition to the ordinary synchronous switching, may switch all phases asynchronously.

Figure 22 is an illustration of how individual phases operate either independently or simultaneously. ATR improves

transient response by momentarily increasing the maximum current slew rate.

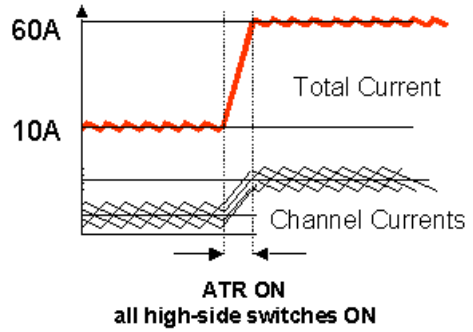


FIGURE 22. ILLUSTRATION OF ATR AND NON-ATR PHASE AND TOTAL CURRENT

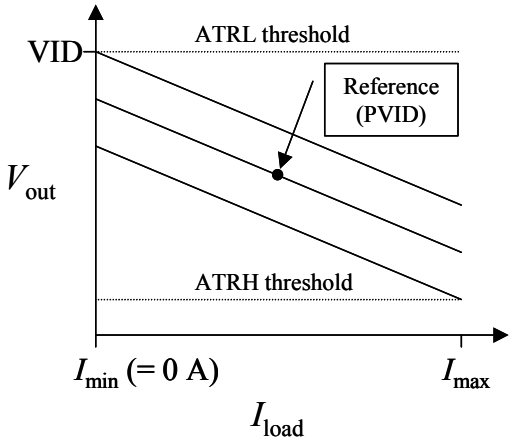


FIGURE 23. BASIC ATR THRESHOLD DEFINITIONS

How ATR Is Enabled and Disabled

ATR is defined using the load line and its specification of DC and transient voltage limits. A sample is shown in Figure 23. The “maximum” V_{OUT} value at no load is commonly the VID. The “maximum” and “minimum” envelopes around “typical” are commonly symmetrical.

One ISL6580 is dedicated to ATR sensing. It maintains an internal reference voltage that is fixed at the midpoint of the “typical” load line excursion (see Figure 23). This reference voltage is labeled PVID. Then independent transient voltage thresholds are defined via the user interface software relative to PVID. The ATRL threshold defines the highest transient overshoot; the ATRH threshold defines the lowest transient undershoot.

If the output voltage rises above the ATRL threshold, then the dedicated ISL6580 sends an ATRL pulse. When the output voltage returns below the ATRL threshold, the ATRL pulse is ended. Similarly, if the output voltage drops below the ATRH threshold, then the dedicated ISL6580 sends an ATRH pulse. The ATRH pulse is ended when the output voltage returns above the ATRH threshold.

When an ATRL or ATRH pulse is received by the ISL6590, two mutually exclusive ATR modes are possible. If an ATRL pulse is received first then ATRL reaction is enabled and ATRH pulses are ignored. Conversely, if an ATRH pulse is received first then ATRH reaction is enabled and ATRL pulses are ignored.

After entering either ATR mode, if neither an ATRL nor an ATRH pulse is received for a short time (<100ns), then ATR mode is exited. Ordinary closed-loop response is resumed.

What ATR Does

Switching of the ISL6580’s by the ISL6590 is typically performed using synchronous complementary PFET and NFET control signals. This push-pull alternation alone cannot provide a rapid response to fast load transitions. When either ATR mode is enabled, fast asynchronous control signals are generated. Furthermore, ATR suppresses the alternating push-pull switching to improve the transient response. The final control signals (named NDRIVE and PWM) sent by the ISL6590 are the combination of these synchronous and asynchronous sources. Three permutations result:

1. If ATR is not engaged, then
   NDRIVE = *NFET* (synchronous)
   PWM = *PFET* (synchronous)
2. If ATRL mode is engaged, then
   NDRIVE = *NFET* (sync) + *ATRL* (async)
   PWM = off
3. If ATRH mode is engaged, then
   NDRIVE = off
   PWM = *PFET* (sync) + *ATRH* (async)

Figure 24 illustrates both ATR modes. Two successive phases are shown in a hypothetical *n*-phase system.

In the first sequence shown, ATRL is received before ATRH. This forces off all PWM signals. The NDRIVE signals are the combination of NFET and ATRL. The asynchronous ATRL is applied simultaneously to the NDRIVE signal of all phases. Note that the ordinary synchronous NFET signals have a long on-time. Therefore, many of the asynchronous ATRL signals are hidden by the synchronous NFET signals. Hidden ATRL signals are colored gray in Figure 24.

In the second sequence shown, ATRH is received before ATRL. This forces off all NDRIVE signals. The PWM signals are the combination of PFET and ATRH. As above, the asynchronous ATRH is applied simultaneously to the PWM signal of all phases. Note that, unlike NFET, the ordinary synchronous PFET signals have a short on-time. Therefore, most of the asynchronous ATRH signals are not hidden by the synchronous PFET signals. Hidden ATRH signals are also colored gray in Figure 24.

Between the two sequences, ATR mode is disabled because ATRL and ATRH signals are absent.

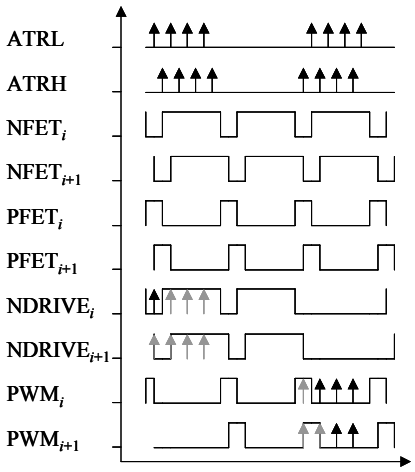


FIGURE 24. COMBINATION OF SYNCHRONOUS (NFET AND PFET) AND ASYNCHRONOUS (ATRL AND ATRH) SIGNALS TO GENERATE EFFECTIVE CONTROL SIGNALS (NDRIVE AND PWM) TO ISL6580'S

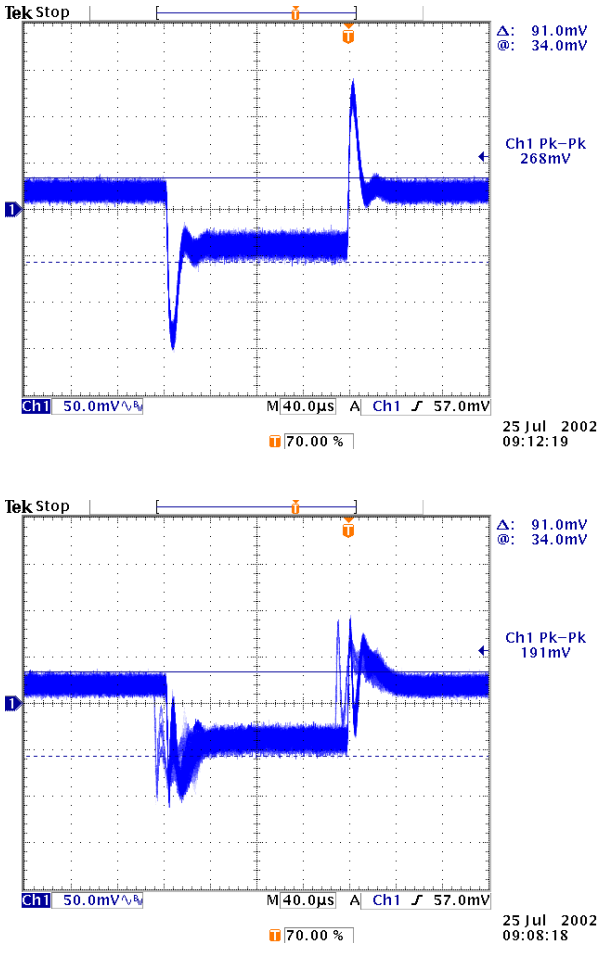


FIGURE 25. SAMPLE OUTPUT VOLTAGE TRANSIENT RESPONSE WITHOUT & WITH ATR ENGAGED

ATR Threshold Definition

The ATRL and ATRH transient voltage thresholds are set with the user interface software and written to the dedicated ISL6580. The voltage offsets are programmed digitally in 7.5mV increments. The ATRL and ATRH offsets may be specified independently.

ATR and VID Stepping

The reference voltage (PVID) used for ATR sensing is updated synchronously with VID stepping. Therefore, the ATR transient voltage thresholds programmed by the user track VID automatically.

ATR Connections

The dedicated ISL6580 requires that the VRM sense leads be connected to its vsense+ and vsense– inputs. This sensed output voltage is compared against PVID and used to generate ATRL and ATRH as necessary. It is highly recommended that both PCB traces be routed as a minimal length pair to minimize differential and common-mode noise pickup. A single-pole low-pass filter at the vsense+ and vsense– inputs is also recommended to further suppress high-frequency pickup noise.

The ATRL and ATRH outputs of the dedicated ISL6580 must be connected to the ATRL and ATRH inputs of the ISL6590. It is highly recommended that both PCB traces be routed as a pair to minimize skew and common-mode noise.

Protection Features

The ISL6580 / ISL6590 have several protection features that shut down the converter to prevent catastrophic and cascade system failures. Output voltages, currents and temperatures are monitored and compared to limits that are set by the designer (with the user interface software). Input Under Voltage (IUVP), Output Under Voltage (OUVP), Output Over Voltage (OOVP) and Over Temperature Sense are detected by each ISL6580. If any of the fault limits are exceeded a fault bit is set in the ISL6580's fault register. The ISL6590 controller polls the fault register continuously via the Back Side Bus. If any of the fault bits are set the converter shuts down. the user interface software reads the fault registers and indicates which type of fault caused the shut down (in the Controls and Interface window). Input power must be cycled off to reset most faults. IUVP is reset by cycling the OUT_EN line. The ISL6590 controller shuts the converter down by setting all PWMs and NDRIVEs signals to ground and switching all MOSFETs OFF.

Over Current Protection

Over Current is handled in two ways. One is Peak Current Limiting ('pulse by pulse' current limiting). If the ISL6580 senses current above the Peak Current limit set with the user interface software, it turns the upper MOSFET off for the remainder of one switching period. This does not shut down the converter.

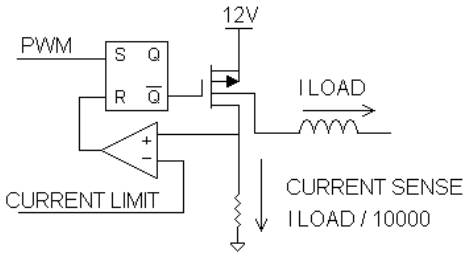


FIGURE 26. BLOCK DIAGRAM OF PEAK CURRENT LIMITING

The second way of responding to a Current Over Load is performed in the ISL6590 controller. If the sum of the average currents in all phases exceeds the Over Current Limit for a prolonged period, the controller is shut down (all MOSFETs are turned off) and input power must be cycled to reset the fault.

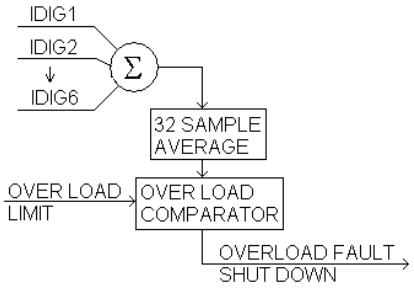


FIGURE 27. OVER LOAD FAULT

The limits for Peak Current and Over Load Current are set with the user interface software. There are 4 steps in the Peak Current limit and the resulting current is calculated (based on the value of R_{SENSE}) and displayed by the user interface software.

OUVP (Output Over Voltage Protection) and OOVP (Output Under Voltage Protection)

ISL6580 monitors the output voltage and sets a bit in its fault register if the output voltage is too high (OOVP) or too low (OUVP).

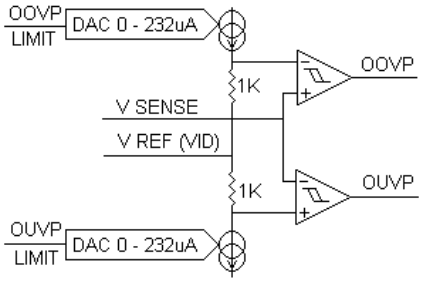


FIGURE 28. OOVP OUVP WINDOW COMPARATOR

Voltage at the VSENP_FILT pin is compared to thresholds above and below normal output voltage (mid point of the load line). The OOVP and OUVP thresholds are set with the user interface software . The range is 0 to 232mV in steps of 7.5mV.

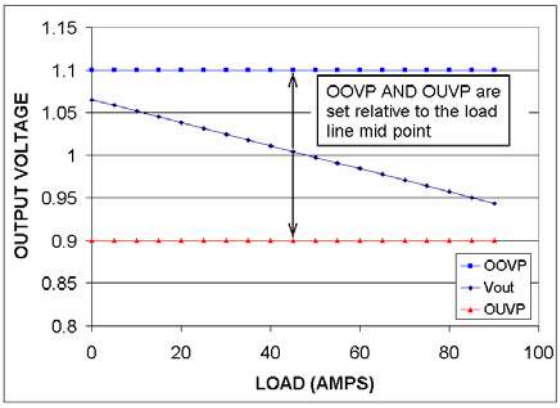


FIGURE 29. OOVP OUVP TRIP LEVELS AND LOAD LINE

If the thresholds are exceeded a bit is set in ISL6580's status register. The status register is read periodically by ISL6590. ISL6590 shuts down the converter until power is cycled.

Temp. Sense (Thermal Shut down)

Each ISL6580 has an on chip, over temperature comparator. It uses an unbalanced differential pair of lateral PNP transistors to sense temperature and detect over temperature. Current in one of the differential pair is 8X the current in the other. As a result, the delta Vbe due to temperature is 8X. Voltage at the bases is offset by DAC controlled current sources. When the Vbe offset reaches the offsets set by the DAC the output switches (with 10×C hysteresis).

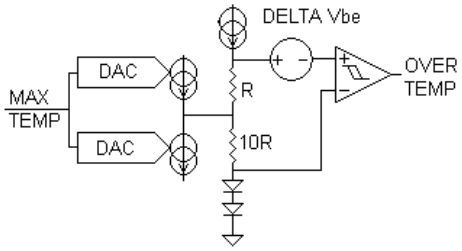


FIGURE 30. OVER TEMPERATURE BLOCK DIAGRAM

The trip point can be adjusted from 85× to 145× in 10×C increments using the user interface software. If any ISL6580 reaches the thermal shut down temperature, a bit is set in its status register, the converter shuts down until power to the ISL6590 is cycled.

IUVP (Input Under Voltage Protection)

Each ISL6580 contains a comparator that monitors V_{CC} and inhibits operation when V_{CC} (12V) is below a fixed threshold. When V_{CC} is turned on, this feature holds the converters output at 0V until V_{CC} exceeds 7.5V. When V_{CC} falls below 7.6V a bit is set in the status register. ISL6590 reads the status register periodically. When this bit is set the converter

is shut down until OUT_EN or power to the ISL6590 is cycled. The threshold has hysteresis to eliminate oscillation. When V_{CC} is low (below 7V), a bit in the status register is set high. As V_{CC} rises from a low value to above 9.1V (nominal) the status bit is set to 0 and a hysteresis switch sets the IUVP threshold to 7.6V (nominal). The converter will operate until V_{CC} falls below 7.6V (see the ISL6580 data sheet for complete specs). The thresholds are referenced to V_{DD} (3.3V) and vary in proportion to V_{DD}.

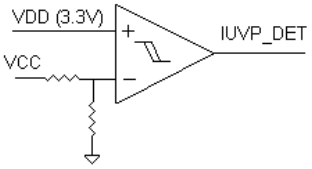


FIGURE 31. INPUT UNDER VOLTAGE PROTECTION

Power On Reset

The ISL6590 controller performs a Power On Reset function internally. It holds all internal logic in a reset state until V_{DD} (3.3V) exceeds a threshold. While in the reset state all PWM and NDRIVE signals are held at ground and all MOSFETs are OFF.

Duty Cycle Limit

The ISL6590 limits the on time of the upper FETs. The system designer can set the maximum ON time with the user interface software. The value is entered as a percentage. If the duty cycle reaches this percentage, the top side FET turns off until the next cycle.

Component Selection and System Flexibility

Inductor Selection System Effects

There are three major system impacts that the phase inductance value impacts. These are transient response, size, and efficiency.

TRANSIENT RESPONSE

Selection of higher phase switching frequency enables selection of lower inductance values because peak current limit protection will not be tripped with the shorter on time. Lower inductance values can yield higher di/dt slopes to the load in the ATR (Active Transient Response) mode of operation in a multiphase system. ATR forces all phases to an ON state at a given point in time producing the following di/dt through the power stage.

$$\frac{di}{dt} = \frac{(Vo\text{-}Vout)Phases}{L} \qquad \text{(EQ. 3)}$$

This di/dt is the power stage current slope capability not the overall system di/dt which is dependent on many other factors including output capacitance and parasitics.

SIZE

In general lower inductance values yield smaller designs for a given current level.

EFFICIENCY

The output inductor can be a significant contributor to system loss. The inductance value will force a trade for system efficiency vs. size and transient response. That is, Physically larger, lower frequency designs will be more efficient and produce slower transient response in the system.

These three system criteria must be considered when selecting or designing the appropriate inductor in a given application.

Inductance selection

The following formulas apply to this section in selecting the appropriate inductance for a given application:

F_S = single phase switching frequency

T_P = switching period

V_{IN} = input voltage

V_{OUT} = output voltage

L = inductance

D = duty cycle

T_{ON} = on time

T_{OFF} = off time

Phases = number of system phases

Saturation Current

The selection process should start with average and peak-to-peak requirements. At maximum load current the peak current should be maintained to <25A to stay within ratings. of the ISL6580.

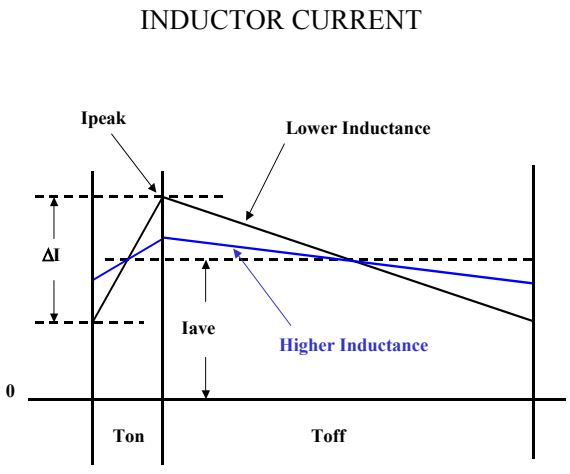


FIGURE 32. AFFECT OF INDUCTANCE ON PEAK CURRENT

$$Ipeak = \frac{Iave}{Phases} + \frac{1}{2}(\Delta I) \text{ where:}$$

$$\Delta I = \frac{(Vin - Vout)Ton}{L} \quad \text{(EQ. 4)}$$

$$Ton = DTp,\ Tp = \frac{1}{F} \qquad D = \frac{Vout}{Vin}$$

All inductors that utilize magnetic material for increased permeability, have a maximum current level at which the inductance dramatically falls. This is known as magnetic saturation. Most inductor vendors will specify the current at which some percentage of inductance has been lost due to saturation. It is important to stay well within the limits of the saturation current of the chosen inductor. It should also be noted that the saturation current reduces at higher temperatures.

di/dt vs Loss

Maximizing the delta I within the inductor to improve di/dt has the effect of increasing peak and RMS currents in the ISL6580, Power FETs, and the inductor itself. The following formulas can be used to calculate the effective RMS current to be used in determining the power loss in these elements:

$$Irms\_ISL6580 = \sqrt{\frac{\left(Ipk^2 + (Ipk)(Itr) + Itr^2\right)D}{3}}$$

$$Irms\_NFET = \sqrt{\frac{\left(Ipk^2 + (Ipk)(Itr) + Itr^2\right)(1-D)}{3}} \quad \text{(EQ. 5)}$$

$$Irms\_Ind = \sqrt{Irms\_ISL6580^2 + Irms\_NFET^2}$$

Operating Frequency

Phase operating frequency has the following relative impacts on the system performance:

1. Size - Higher frequency per phase will minimize the size of the required output inductor while maintaining a given delta current in the inductor. Generally speaking ferrites perform best at higher frequencies (>200kHz). This is due to the fact that the magnetic materials are higher and lower conductivity, which tends to reduce eddy current losses within the core.
2. System Bandwidth – higher switching frequencies allow higher closed loop unity gain frequencies. This is because the main limiting factor in compensation of the voltage loop concerns the Nyquist limitation of the power stage. The voltage loop must be held less than 1/2 the channel switching frequency for a single phased system. Practical designs limit loop bandwidth to < 1/5 of the phase switching frequency.
3. Power loss – In general power loss increases logarithmically with phase frequency as it pertains to the output inductor. Higher frequencies can cause:
4. Hysteresis loss is caused by alternating flux within the core material. Hysteresis loss is a function of the area enclosed by the BH loop and is due to the energy required to move magnetic domains. This loss element decreases logarithmically in most magnetic materials and can be a major contributor at higher frequencies. Inductor vendors work to select materials that suite a specific frequency range.
5. Eddy current loss from the circulating currents within the magnetic materials. Higher switching frequencies produce higher eddy current loss. Eddy current loss can extend to any conductor that is in close proximity to the air gap of a gapped core inductor. Since field strength tends to diminish a rate approximately equal to the inverse square of the distance, conductors should be held to at least 4x the distance of the air gap itself.
6. Copper or winding loss. This is also dependent on the wire size, switching frequency, etc. Skin effect is the tendency of AC currents to migrate to the outer portions of a conductor. This can tend to decrease the effective copper cross sectional area of a conductor at high frequencies and should be considered in selection of inductors with relatively thick conductors.

MOSFET Selection

In the Intersil Digital Multiphase Architecture, a critical component selection is the low side MOSFET. The power dissipation from the low and high side MOSFET is dominated by different factors. Because of the longer duty cycle (Figure 33), the low side MOSFET efficiency is dominated by static on losses. However, the low duty cycle of the high side MOSFET results in the majority of its losses to come from switching of the FET (Figure 34).

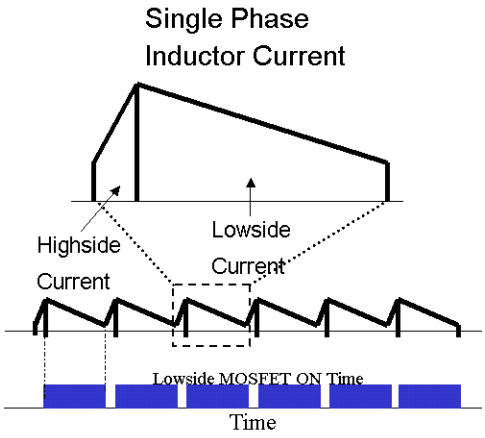


FIGURE 33. HIGH AND LOW SIDE MOSFET DUTY CYCLE

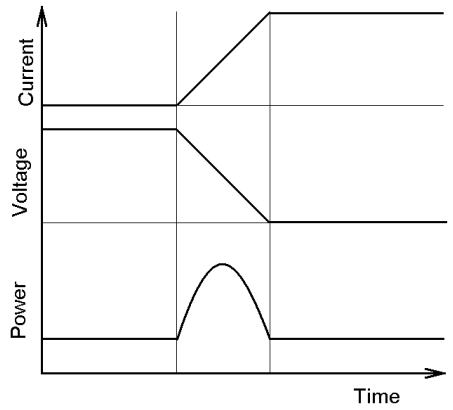


FIGURE 34. POWER DISSIPATION FOR STATIC AND DYNAMIC OPERATION

The key characteristic for the low side MOSFET is the DC Rdson resistance. It is important to get a very low Rdson value for the low side FET. For the high side MOSFET, gate charge requirements are the key characteristic. Large gate charge and gate resistance increases switching losses. Because the high side MOSFET is integrated within the ISL6580, a very low gate resistance of less then 300mW is present. In a discrete high side MOSFET solution, a typical total gate resistance from the gate driver and including the internal silicon gate resistance is 1.5 to 2W. The integrated MOSFET in the ISL6580 is optimized for high switching efficiency with a low gate capacitance.

Understanding the turn on and turn off event for a MOSFET is important in understanding how to interpret a data sheet and for troubleshooting methods for the low side MOSFET in particular.

Switching of the MOSFET

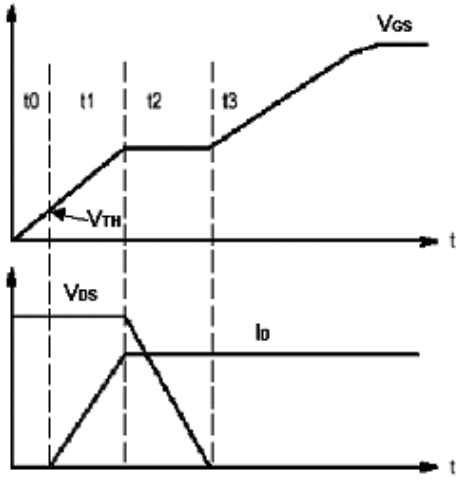


FIGURE 35. MOSFET TURN ON CURVES

The MOSFET is driven by the applied gate to source voltage. When the gate voltage is initially applied, the voltage potential begins to ramp across the gate to the source, but no current flows until the intrinsic threshold voltage level is achieved (Figure 35). During time t1, the gate to source capacitance (C_{GS}) charges and the drain to source current (I_{DS}) and gate to source voltage (V_{GS}) continue to ramp. The slope of the current is directly related to the gate voltage rise time and the forward transconductance of the device as follows:

$$\frac{dI_C}{dt} = gm\frac{dV_{DS}}{dt} \quad \text{(EQ. 6)}$$

where:

IC = Drain Current

gm = Forward Transconductance

V_{DS} = Drain to Source Voltage

The gate to source voltage ramp during this time is:

$$\frac{dV_{DS}}{dt} = \frac{V_{GG} - V_{plateau}}{R_G - C_{iss}} \quad \text{(EQ. 7)}$$

$$V_{plateau} = V_{TH} + \frac{I_C}{gm} \quad \text{(EQ. 8)}$$

where:

V_{DS} = Drain to Source Voltage

V_{GG} = Gate Supply Voltage

R_G = Gate Resistance

Ciss = Constant Input Capacitance

V_{TH} = Threshold Voltage

I_C = Collector Current

gm = Forward Transconductance

Substituting equation 7 into equation 6 gives:

$$\frac{dI_C}{dt} = gm\left(\frac{V_{GG} - V_{plateau}}{R_G - C_{ies}}\right) \quad \text{(EQ. 9)}$$

Once time t2 is reached, C_{GS} has been fully charged. IDS plateaus and V_{DS} begins to ramp down. During time t2, the gate to drain capacitance (C_{GD}), also known as the Miller capacitance, begins to charge. Once the Miller capacitance is fully charged, V_{GS} rises until it reaches the voltage level of the gate supply.

The turn off of the MOSFET is fundamentally the same as the turn on in reverse order (Figure 36). V_{GS} reduces to the level required to maintain the drain current (beginning of t4). At that point, V_{DS} begins to rise at a rate of:

$$\frac{dV_{DS}}{dt} = gm\frac{V_{plateau}}{R_G C_{rss}} \quad \text{(EQ. 10)}$$

Where:

Crss = Transfer Capacitance

V_{DS} eventually reaches the rail voltage. Because of the high dv/dt value during this period, V_{DS} often will rise beyond the bus voltage for a short period of time. This overshoot is from the inductive voltage kickback of the choke inductance and parasitics of the traces. When V_{DS} first reaches the rail voltage, C_{DG} is fully discharged. The drain current starts to decay at the rate of:

$$\frac{dI_D}{dt} = gm\left(\frac{V_{plateau}}{R_G C_{iss}}\right) \quad \text{(EQ. 11)}$$

Eventually, the current reaches zero and the switching event ends.

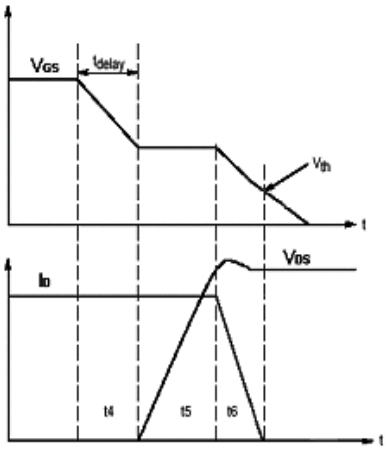


FIGURE 36. MOSFET TURN OFF CURVES

Efficiency of the MOSFETs

The equations below provide a rough estimate for power dissipation of the upper and lower MOSFETs. These equations do not take into account the reverse-recovery of the lower MOSFETs body diode or a snubber circuit used in this regard.

$$P_{UPPER} = \frac{Io^2 \times Rds(on) \times Vout}{Vin} + \frac{Io^2 \times Vin \times Tsw \times Fsw}{2} \quad \text{(EQ.12)}$$

$$P_{LOWER} = \frac{Io^2 \times Rds(on) \times (Vin - Vout)}{Vin} \quad \text{(EQ.13)}$$

Pupper = Power loss in upper MOSFET

Plower = Power loss in lower MOSFET

Io = Average Current

Rds(on) = On resistance for the particular MOSFET at the appropriate gate voltage and temperature of operation

V_{OUT} = Output Voltage

V_{IN} = Input Voltage

Fsw = Frequency of operation per phase

Tsw = On/Off Switch Time

Junction Temperature Evaluation

With power loss in a transistor comes dissipation of that power in the form of heat. The higher the power loss, the higher the parts junction temperature will be. A basic thermal model is seen in Figure 37. Through the data of the MOSFET used, the thermal resistivity from junction to case can be determined. With a measurement of the case of the MOSFET during operation, the FETs junction temperature can be calculated.

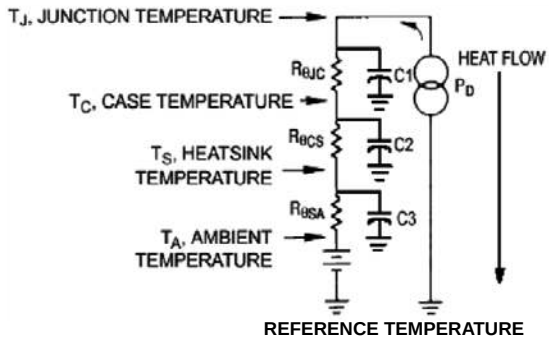


FIGURE 37. THERMAL RESISTIVITY MODELING

The formula used for calculating junction temperature is:

$T_J = P_D * R_{\theta JC} + T_C$

P_D =Power dissipation = voltage across the transistor (V_{DS}) * current through the device (I_D)

$R_{\theta JC}$ = 10µs pulse rated junction to case thermal resistance. This value can be found by using data sheets for the individual transistors as well as thermal resistance data of the specific package.

T_c = Case Temperature

If the junction temperature rises above specification, the transistor could fail. Also, high junction temperatures during operation can cause reliability issues. In the same sense, if the junction temperature difference between on and ambient off conditions is significant, temperature cycling can be a reliability issue as well.

Effective heat flux from the power transistor to ambient is critical to ensure reliability. The main trade-off for effective

heat flux designed into the system is die and heat sink size. The larger the die size, the higher the part costs but more effective heat flux occurs. A smaller die size can be used with a larger heat sink added. Of course increasing the switching speed of the device and/or reducing the frequency of operation of the transistor will reduce power dissipation, but both of these are typically defined directly from the application.

If there is a high thermal increase in a MOSFET, a cost analysis should be performed to consider a larger die size, a larger heat sink, or parallel MOSFETs to share the current.

MOSFET Transistor Selection

When selecting the appropriate low side MOSFET to put in the power circuitry, there are some basic characteristics that need to be considered.

- N type or P type MOSFET
- For the low side MOSFET component, an N polarity MOSFET is always used.
- Current Rating
- At least 3X the peak current input should be select for the current rating.
- Voltage Rating

The input voltage for computing multiphase power supply for the chip set is a 12V DC nominal. Standard MOSFET voltage rating for the low side FET ranges between 20V-30V depending on the switching speed of the switch node and the noise of the input rail. This increased voltage level is used to take into account inductive voltage kickback and transient voltage inputs.

Inductive Switching

The ISL6580 Integrated Power Stage is a High Side FET/driver combination with external synchronous rectifier that provides high current at high switching frequency. Schematic of Figure 38 shows a typical synchronous buck converter application using the ISL6580.

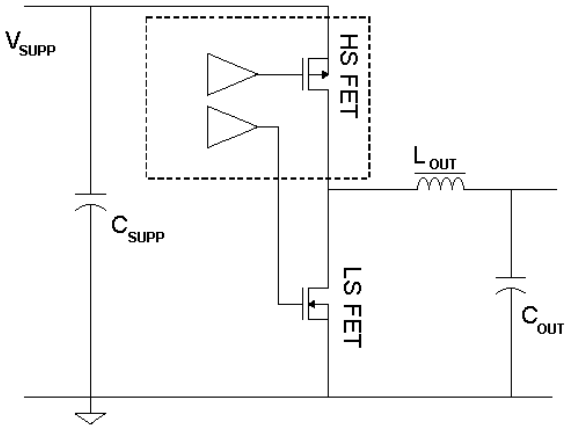


FIGURE 38. SYNCHRONOUS BUCK CONVERTER USING ISL6580

Package and board level interconnects of individual components in the high current loops give rise to series RLC circuits. Fast switching of large currents in these loops will generate large voltage transients that may exceed maximum device ratings. Specifically, at the turn off phase of the high side switch, the sudden disruption in the loop current will generate fast transient ringing at the high side switch exposing the high side switch to large voltages that can exceed the rated break down voltage for that device. Figure 39 shows the high frequency equivalent circuit at the turn-off of the high side switch before the turn-on of the low side switch. Included in this schematic are the relevant parasitic effects of various components and interconnects.

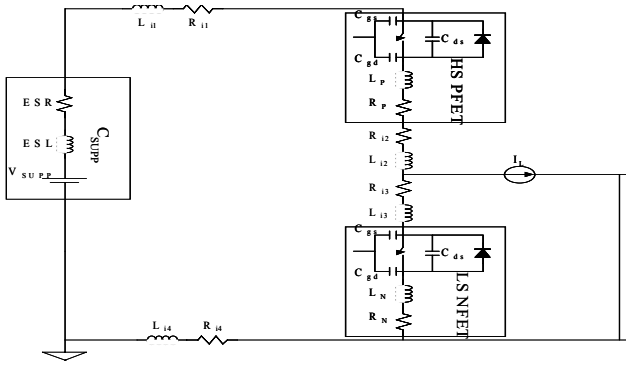


FIGURE 39. HIGH FREQUENCY EQUIVALENT CIRCUIT OF THE HIGH SIDE SWITCH TURN OFF LOOP

This application note discusses the use of external Schottky diodes in order to limit the amplitude of transient voltage spikes across the drain to source of the high side switch device.

Clamping Using Schottky Diodes

The simplest approach to protect the High Side FET from inductive switching is to limit loop inductance. This can be achieved by proper layout of the high current loops and careful selection of the components in this loop. The goal is to minimize overall loop inductance. This inductance includes HSFET bonding inductance, the external NFET inductance, the power supply decoupling capacitance's ESL, and interconnect inductances between these components. While good layout of the PCB must be always practiced, component selection is often compromised by other factors such as pricing or physical dimensions. For example it is possible that a single NFET with an inductance of up to 8nH is selected for the low side switch.

In such situations where a high inductance FET or special layout considerations result in large loop inductance, placement of a Schottky diode from the switch node to ground will clamp the negative ringing and limit the voltage across drain to source

of the High Side FET. Figure 40 shows the waveform at the switch node with and without a Schottky diode.

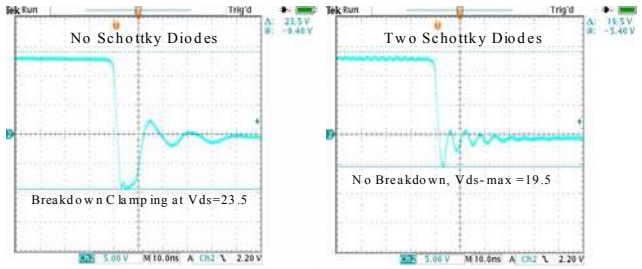


FIGURE 40. EFFECT OF ADDING TWO SCHOTTKY DIODES ON THE VDS OF THE HIGH SIDE SWITCH

Note that the Schottky diode provides a parallel path to the body diode of the NFET for current flow. It is best to place the Schottky diode as close as possible to the switch node of the High Side FET on one pin and to the ground return of the power supply decoupling capacitors on the other pin (as shown in Figure 41). This way during clamping the inductance of the Schottky diode is in parallel with the inductances of interconnects as well as the low side NFET therefore minimizing the overall inductance.

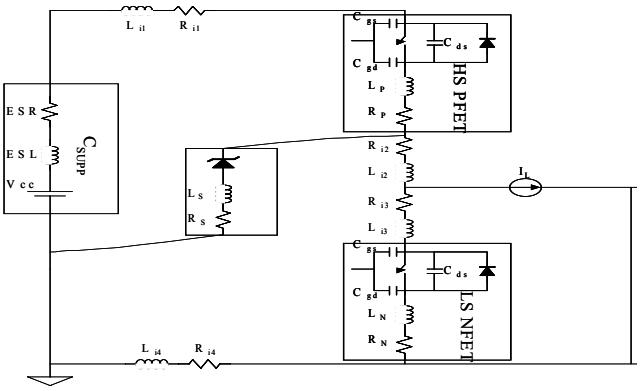


FIGURE 41. PROPER SCHOTTKY PLACEMENT PARALLELS LOW SIDE SWITCH AND ROUTING PARASITIC EFFECTS

Schottky Selection

The most important characteristic of a Schottky diode selected for clamping of the negative fly-back voltage is its inductance. Axial leaded diodes typically exhibit larger inductances. Leadless packages have low inductances in the 2-5nH range. Physically smaller diodes are also preferable because of their potentially lower inductance in addition to printed circuit board space concerns.

The power dissipation in the Schottky diode is small and limited to the non-overlap time, when the HS PFET is turned off and before the LS NFET is turned on. Even during this period, the body diode of the LS NFET starts conducting shortly after the HS PFET is turned off and will share in conducting the current. It is still necessary to ensure that a Schottky diode is selected that can handle the peak current for a short period during each switching cycle.

Selection of R_{SENSE}

When selecting the resistor value for R_{SENSE}, several characteristics have to be considered. They include:

1. Size of Csample (6.2pF). Internal to the ISL6590.
2. # of steps (Steps = 64)
3. Ratio (M = 9,900) of transistors used for current mirror and main current path in the high side MOSFET.
4. Reference Voltage (V_{REF} = 1.25V)
5. Input Voltage (V_{IN})
6. Output Voltage (V_{OUT})
7. Output Inductance (Lout)

An easy to use reference equation for calculating an appropriate resistor when considering these values is:

$$Rsense := \frac{1}{\left[8\cdot 10^{-10}\cdot F\cdot\left(V_{in}-V_{out}\right)\right]}\cdot\sqrt{2}\cdot\left[4.9\cdot 10^{-6}\cdot F\cdot V\cdot\left(V_{in}-V_{out}\right)\cdot L_{out}\right]^{\left(\frac{1}{2}\right)} \quad \text{(EQ.14)}$$

This equation takes into account the resolution of the A/D converter vs. the slew rate of the current divider between R_{SENSE} and Csample/Cesd.

For peak current limit, rather then relying on peak current sampling, the power stage taps the I_{SENSE} line and connects directly to a comparator. The comparator turns off the highside MOSFET if the peak current through it reaches its limit real time at any point. The MOSFET is shut down until the next clock cycle. The the user interface software can program the voltage trip level (V_{trip}) across the sense resistor (R_{SENSE}) where a peak current limit trip (I_{trip}) occurs (Equation 15).

$$I_{trip} := \frac{V_{trip}}{R_{sense}}\cdot M \quad \text{(EQ. 15)}$$

If 1V were selected, the peak current limit of (I_{trip}) would be:

$$I_{trip} := \frac{1V}{392\cdot\Omega}\cdot 9900 \quad \text{(EQ. 16)}$$

$$I_{trip} = 25.255A$$

Overload protection restricts the total average output current of the power supply. The average current is predicted by taking peak current samples each clock cycle. With good current balancing, this can be translated to total current output. To predict the average current for each power stage with a peak current sample, an offset down must be assumed. This current offset (Ios) is calculated from the output inductance value, input voltage, output voltage, sense resistor value, and number of phases in the system. When I_{SENSE} peak current sample is taken, Ios is subtracted from

it. This provides a predicted average current per power stage (Figure 42). If any individual power stage reaches this over current protection level, the VRM shuts down and reports an over current fault condition. This protection feature can be disabled or enabled via the the user interface software. The user interface software also allows programming of the total average output current level where the fault condition trips.

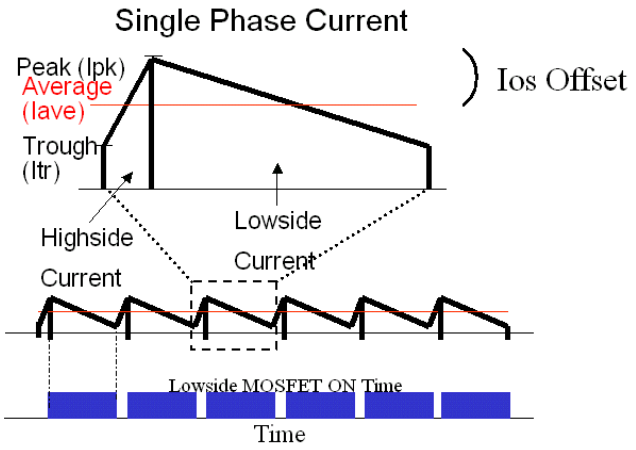


FIGURE 42. AVERAGE CURRENT PREDICTED FROM PEAK CURRENT SAMPLE MINUS IOS OFFSET

INPUT AND OUTPUT CAPACITOR SELECTION

The VRM requires capacitors at the input as well as the output to limit the fluctuation in voltage with a change in other conditions of the system. These changes include events such as load variations, VID stepping, start-up and shutdown.

Input Capacitors

VRM INPUT CAPACITOR:

The VRM is configured as a multi-phase buck converter. By its nature, a buck converter draws current from the input source in pulses, as shown in Figure 43 In the absence of an input capacitor, the high-frequency current pulses would lead to glitches and ringing at the input voltage with every current transition. The VRM specification also places an upper limit on the slew rate of the input current. A capacitor bank at the input to the VRM provides the pulsed charge to the VRM and draws an average DC current from the input supply. As shown in Figure 43, the input capacitor results in a much lower slew rate of the VRM input current than that of the high-side current of individual channels in the VRM.

The value of the input capacitor is determined from the maximum channel current and the highest switching frequency of the power stage. The input capacitor to the VRM is implemented using electrolytic capacitors. The ESR and ESL of the input capacitor are not critical concerns because the input current has low magnitude and tight regulation is not required.

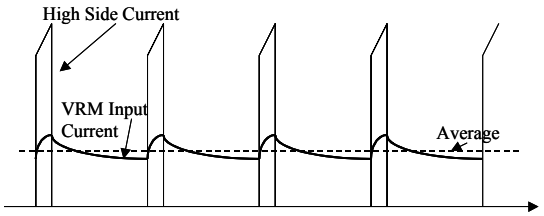


FIGURE 43. INPUT CAPACITOR FILTERS OUT THE INPUT CURRENT REQUIREMENT OF THE VRM AND LIMITS THE SLEW RATE OF THE INPUT CURRENT

POWER IC V_{CC} CAPACITOR:

A bank of input capacitors is also needed at the supply terminals of each Power IC. The high-side FET in the buck converter is integrated into the Power IC. The low-side FET is an external part. The package inductance of the Power IC and the low-side FET as well as the path inductance between the two parts are parasitic elements in the power stage. A large current slews through the parasitic inductance each time the high side or the low-side FET is switched. This results in high-voltage spikes and ringing at the switch node, V_{CC} pad and the ground pad. Under extreme circumstances, the voltage spike may exceed the breakdown voltage of the high side or the low-side FET. Furthermore, the Power IC has low-voltage analog and digital circuits that are isolated from the power stage. Extreme swings of the high-side FET voltage beyond the nominal values may exceed the limits of the isolation and result in the undesired effects of latch-up, substrate current and loss of synchronization with the digital controller. Power supply stabilizing capacitors should be placed between the V_{CC} and ground planes at the site of each Power IC. Ceramic capacitors that have low ESR and ESL are well suited for this application. Similar to Figure 43, the ceramic capacitors at each Power IC eliminate the need for the high-current pulses to flow from the connector input pins to the site of each Power IC, thus reducing on-board power dissipation

Output Capacitors

The choice of the output capacitor depends on the desired output voltage ripple, switching frequency of the power stage and the transient voltage excursions. A combination of OSCON and ceramic capacitors is used to form the output capacitor bank.

Steady State Ripple

The fundamental ripple of a buck converter is ideally determined by the value of the output inductor and the output capacitor. The fundamental ripple of a multi-phase buck converter operating at a switching frequency of several hundred kilohertz can be shown to be negligible. However, as the switching frequency increases, the

contributions from the ESR and the ESL of the output capacitor can be substantial, as expressed below:

$$V \quad \frac{V_{in}}{L} ESL \quad \frac{V_{in} \quad V_{out} \; V_{out}}{V_{in} f_{sw} L} ESR \qquad \text{(EQ. 17)}$$

where DV is the output voltage ripple, V_{IN} is the input voltage, V_{out} is the output voltage, f_{sw} is the power stage switching frequency, and L is the effective output inductance. The contributions of ESR and ESL of the output capacitor to the output voltage ripple are illustrated in Figure 44.

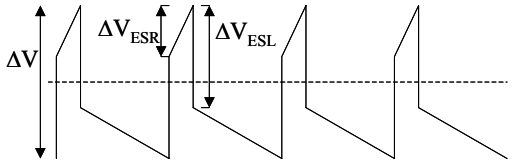


FIGURE 44. CONTRIBUTIONS OF ESR AND ESL OF OUTPUT CAPACITOR TO OUTPUT VOLTAGE RIPPLE

For instance, a 4-phase VRM operating from a 12V input at 500kHz with 400nH inductance per phase and delivering 1.4V output will approximately have a fundamental ripple of 25 mV when the output capacitor has an effective ESR and ESL or 0.5mW and 0.1nH respectively. Even though OSCON capacitors are much better than ordinary electrolytic capacitors, their ESR and ESL values are high enough to result in substantial steady-state ripple. Consequently several OSCON capacitors are connected in parallel at the output to minimize the ESL and ESR effects.

Transient Response

The choice of output capacitance also impacts the transient performance of the voltage regulator. Immediately following a load current step, the output capacitor bank provides charge to the load until the feedback loop catches up. As the capacitor charge drains (low-high load step) or accumulates (high-low load step), the output voltage also varies accordingly. Considering that it is easier to charge or discharge low capacitance, higher capacitance values are desired to minimize the excursion of the load voltage. It is possible to choose the number of OSCON capacitors that will provide a transient response with negligible voltage overshoot or droop. Systems that have feedback loops with higher crossover frequency require smaller output capacitance.

Start-Up

It is well established that several OSCON capacitors can be connected in parallel to improve the voltage ripple and transient voltage excursion. However, this results in an area penalty to accommodate the capacitor count on the board. In addition, the inrush current requirement at start-up goes up with an increase in the effective output capacitance value. The state control on the VRM has a soft-start mechanism that ensures that the output voltage does not overshoot beyond the set point at start-up. However, the lowest regulated output voltage of the system is around 0.7V and the system operates in an open loop manner until the error voltage is within the span of the voltage A/D converter. During this time, the duty cycle of the PWM signal expands at a rate determined by the compensator. Systems with high output capacitance take more time to raise the output voltage to the minimum voltage necessary for regulation. The current supported by each channel increases in proportion to the increase in duty cycle. The VRM has an in-built over-current protection mechanism that detects conditions of high-current flow through the entire system as well as individual channels. Beyond a threshold level, the inrush current can be interpreted as an overload condition, causing the system to shut down. It is possible to avoid this condition by reducing the pulse-by-pulse trip level. However, this mode of operation is not recommended because it deteriorates the transient performance of the system during a low to high load current step. A better approach is to avoid overpopulating the output stage with OSCON capacitors.

As an alternative to using several OSCON capacitors, ceramic capacitors are normally connected in parallel with the output OSCON capacitors to improve the high-frequency response of the system. Ceramic capacitors have much lower ESR and ESL compared to OSCONs. This enables them to absorb short-duration phenomena such as glitches better than OSCONs. When the switching frequency of the power stage exceeds 500kHz, more ceramic capacitors are needed to limit the transient glitches.

Max Gate Drive

Excessive RMS current in the lower gate drive pins can reduce the reliability of ISL6580. Gate drive current depends on V_{DRIVE}, switching frequency and the capacitance of the lower side FET. Below is a graph of the maximum reliable gate capacitance as a function of switching frequency and V_{DRIVE}. Gate capacitance is usually listed in the MOSFET data sheet as Ciss. If Ciss is not specified it can be

estimated from the total gate charge divided by the drive voltage (V_{DRIVE}).

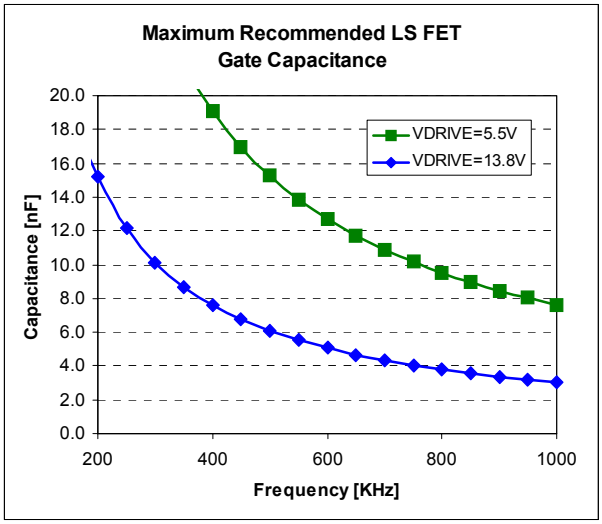


FIGURE 45. MAXIMUM GATE CAPACITANCE

Bias Supply Power On Sequence

Incorrect power-up sequencing can result in malfunction or damage to the ISL6580.

V_{CC} = 12V

V_{DD} = 3.3V

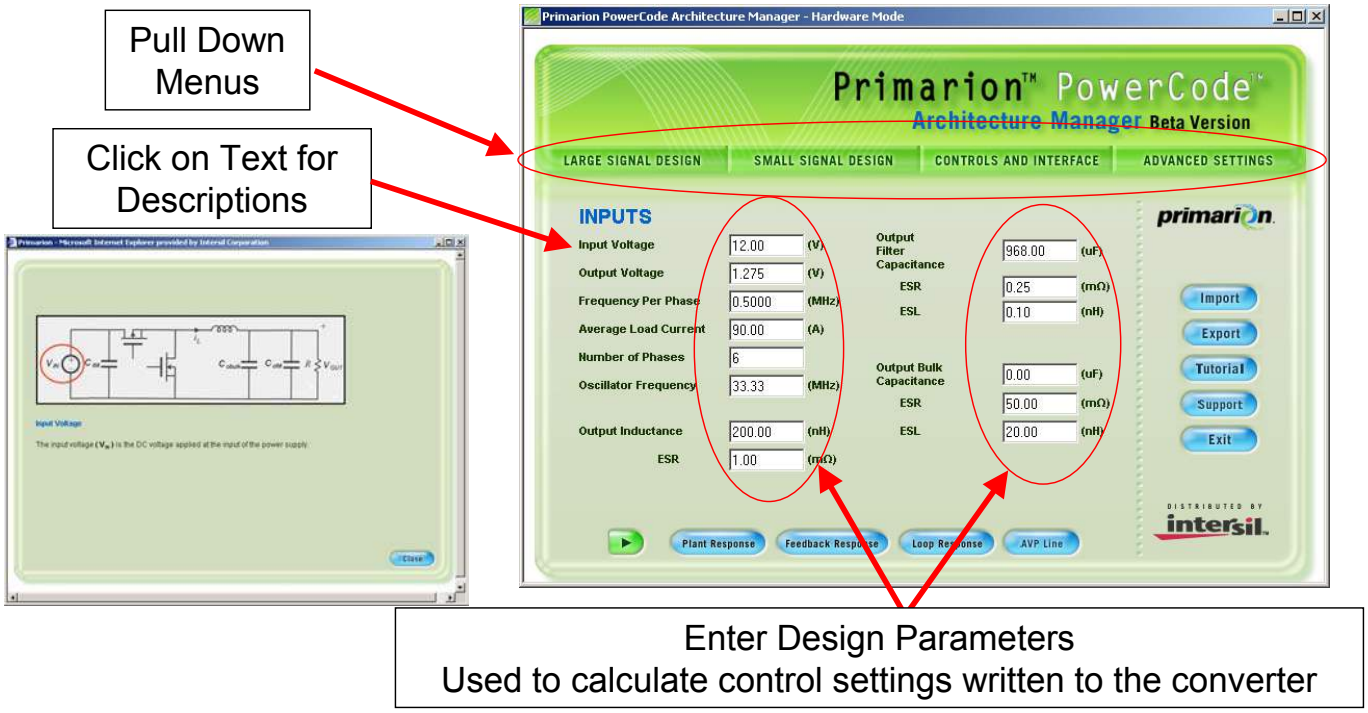
V_{REF} = 2.5V

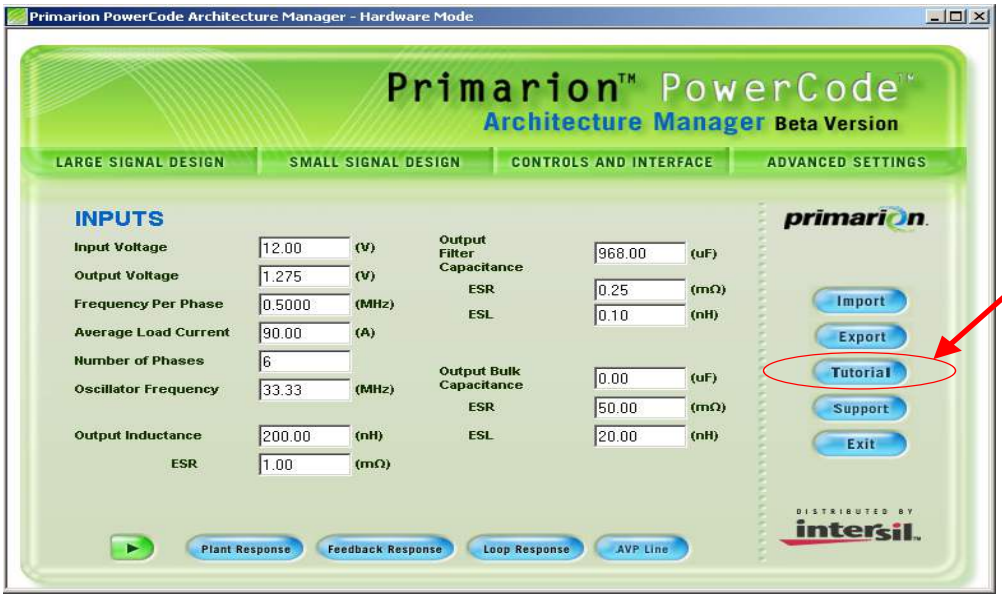
V_{DRIVE} = 5V or 12V

- V_{DD} and V_{CC} should be brought up first, they are independent of one another. If there is any flexibility it is preferred to power V_{DD} up first but it is not critical and there are no ill effects.
- V_{REF} must be powered up after or simultaneously with V_{DD}. ***V_{REF} must not exceed V_{DD} at any time***.
- V_{DRIVE} must be powered up after or simultaneously with V_{CC}. ***V_{DRIVE} must not exceed V_{CC} at any time***.
- Exceptions to this sequence (for example during testing) should be studied on a case by case and may be possible by applying certain current limits.

User Interface Software

The configuration of the ISL6590 controller and the ISL6580 power stages can be adjusted using Primarion® PowerCode(tm) user interface software (provided by Intersil and our partner Primarion). Below are screen shots showing data entry points, pull down menus and buttons for help and a tutorial. the user interface allows the designer to adjust the load line, frequency response, ATR and protection modes.

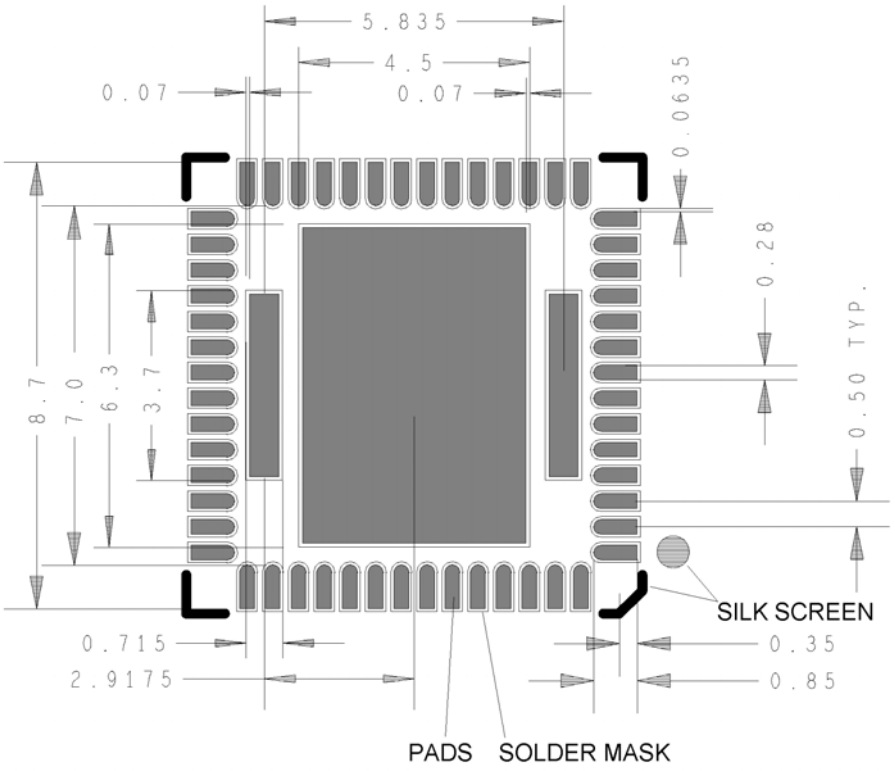




Click on the Tutorial button for Instructions for use of PowerCode and control of ISL6580 / ISL6590

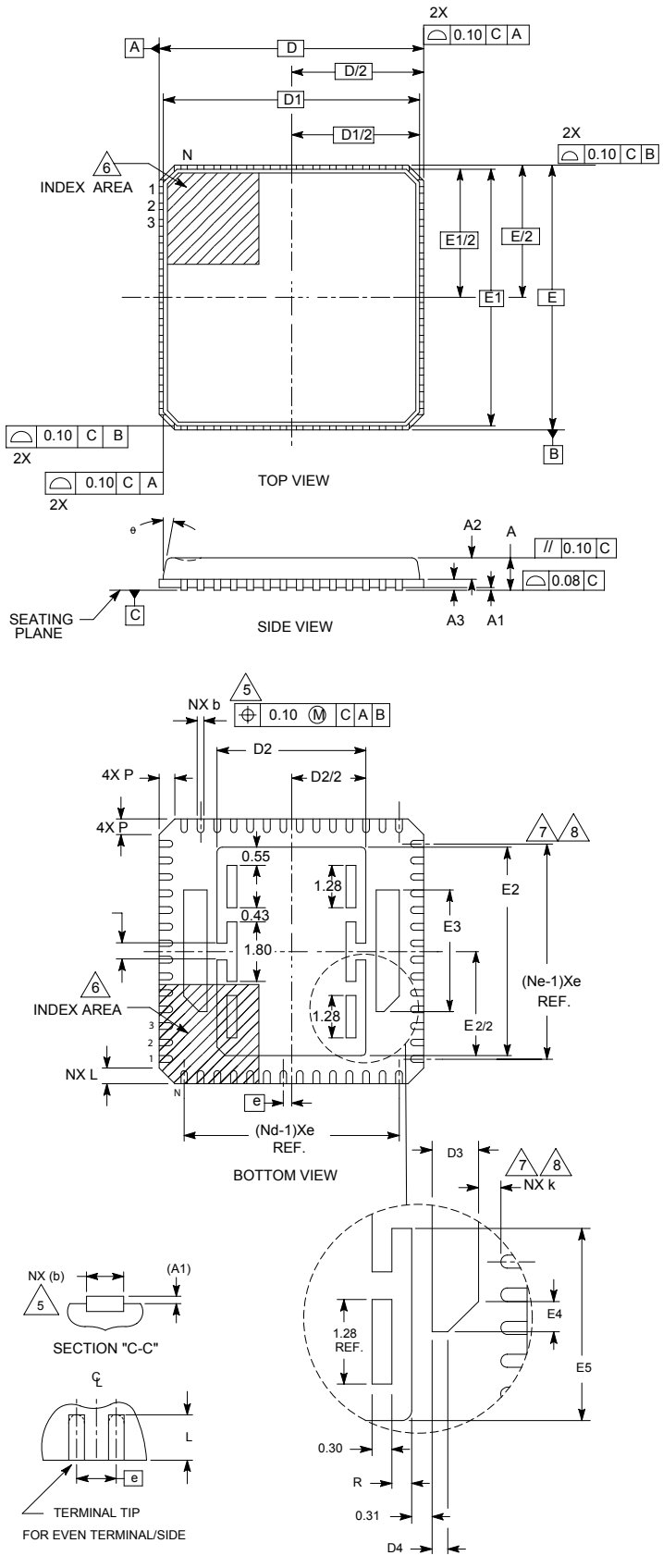
Suggested PC Board Footprint

The drawing below is for reference only. Pad and solder mask geometries should be optimized for specific PCB manufacturing and assembly processes. It is recommended that the center (VCC) pad is rectangular instead of duplicating the outline of the center pad (VCC) on the device.



Second Source Information			
Primarion		Intersil	
Part #	Package	Part #	Package
PX3510	56 Pin QFN	ISL6580	56 Pin QFN

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L56.8x8C

56 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
(Customized with Three Exposed Pads)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	-	0.85	0.90	-
A1	0.00	0.01	0.05	-
A2	-	0.65	0.70	-
A3		0.20 REF		-
b	0.18	0.23	0.30	5, 8
D		8.00 BSC		-
D1		7.75 BSC		-
D2	4.35	4.50	4.65	7, 8
D3	0.55	0.70	0.85	
D4	0.07	0.23	0.38	7, 8
E		8.00 BSC		-
E1		7.75 BSC		-
E2	6.15	6.30	6.45	7, 8
E3	3.52	3.67	3.82	7, 8
E4	0.32	0.47	0.62	7, 8
E5	2.75	2.90	3.05	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
R	0.20	0.30	0.45	-
S	0.35	0.50	0.65	8
L	0.30	0.40	0.50	8
N		56		2
Nd		14		3
Ne		14		3
P	0.24	0.42	0.60	-
θ	-	-	12	-

Rev. 0 02/03

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm & 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2, D3, D4 and E2, E3, E4 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.