

## Evaluating the [ADN4654/ADN4655/ADN4656](#) 5 kV RMS, Dual-Channel, LVDS Gigabit Isolators

### FEATURES

- Isolated ground planes (logic side and bus side)
- Convenient connections through SMA terminals
- 3.3 V or 2.5 V power on Side 1 ( $V_{IN1}$  and  $V_{DD1}$ ) and Side 2 ( $V_{IN2}$  and  $V_{DD2}$ )
- Ground on Side 1 ( $GND_1$ ) and ground on Side 2 ( $GND_2$ )
- LVDS input signals:  $D_{IN1+}$ ,  $D_{IN1-}$ ,  $D_{IN2+}$ ,  $D_{IN2-}$
- LVDS output signals:  $D_{OUT1+}$ ,  $D_{OUT1-}$ ,  $D_{OUT2+}$ ,  $D_{OUT2-}$
- Jumper-selectable power supply of 3.3 V or 2.5 V
- Termination resistors on all LVDS drivers and receivers

### EVALUATION KIT CONTENTS

EVAL-ADN4654EB1Z, EVAL-ADN4655EB1Z, or  
EVAL-ADN4656EB1Z

### DOCUMENTS NEEDED

[ADN4654/ADN4655/ADN4656](#) data sheet

### EQUIPMENT NEEDED

Signal generator  
Oscilloscope

### EVALUATION BOARD PHOTOGRAPH

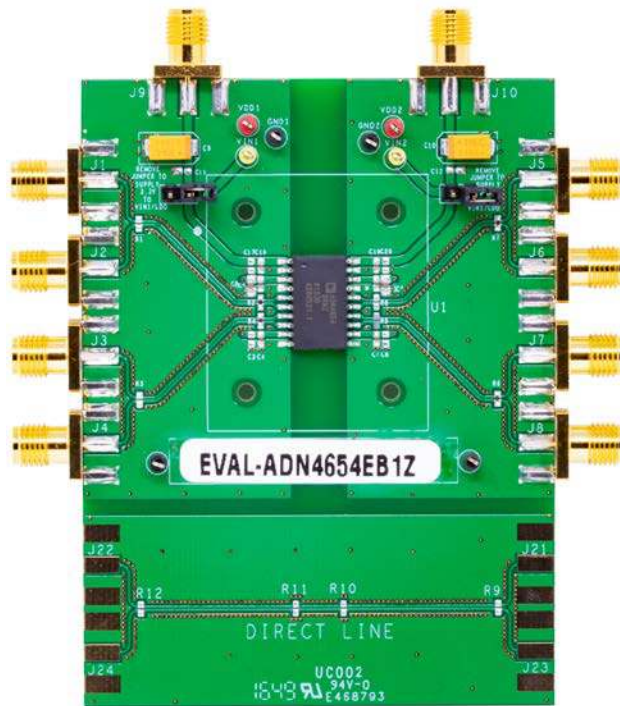


Figure 1.

### GENERAL DESCRIPTION

The EVAL-ADN4654EB1Z, the EVAL-ADN4655EB1Z, and the EVAL-ADN4656EB1Z allow quick and easy evaluation of the [ADN4654/ADN4655/ADN4656](#) low voltage, differential signaling (LVDS) isolators without the need for external components. The [ADN4654/ADN4655/ADN4656](#) employ Analog Devices, Inc., *iCoupler*® technology to combine a 2-channel isolator with an LVDS receiver and driver into a single, 20-lead wide body SOIC package. The devices are capable of running at data rates of up to 1.1 Gbps with low jitter.

The evaluation boards have separate ground and power planes for each side of the isolator. This separation enables the evaluation of the [ADN4654/ADN4655/ADN4656](#) with galvanic isolation

between both sides of the device. Jumper-selectable power supplies at 3.3 V or 2.5 V are required on each side of the [ADN4654/ADN4655/ADN4656](#) device. Using an on-chip, low dropout (LDO) regulator, 2.5 V can be provided from an external 3.3 V power supply.

Complete information about the [ADN4654/ADN4655/ADN4656](#) is available in the [ADN4654/ADN4655/ADN4656](#) data sheet. Consult this data sheet in conjunction with this user guide when using the evaluation boards.

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**REVISION HISTORY**

**6/2019—Rev. A to Rev. B**

Added ADN4656 and EVAL-ADN4656EB1Z..... Universal  
 Changes to Setting Up the Evaluation Board Section ..... 3  
 Changes to Table 3..... 4  
 Changes to Figure 5..... 5  
 Changes to Figure 6..... 6  
 Added Figure 7; Renumbered Sequentially ..... 6  
 Added Table 6; Renumbered Sequentially ..... 10

**11/2018—Revision 0: Initial Version**

**1/2019—Rev. 0 to Rev. A**

Added ADN4655 and EVAL-ADN4655EB1Z..... Universal  
 Changes to Figure 1 ..... 1  
 Changes to Setting Up the Evaluation Board Section ..... 3  
 Changes to Table 2 Title..... 4  
 Added Table 3; Renumbered Sequentially ..... 4  
 Added Figure 6; Renumbered Sequentially ..... 6  
 Changes to Table 4 Title ..... 9  
 Added Table 5 ..... 9

## EVALUATION BOARD CONFIGURATION

### SETTING UP THE EVALUATION BOARD

On the EVAL-ADN4654EB1Z/EVAL-ADN4655EB1Z/EVAL-ADN4656EB1Z, power supplies are configured using Jumper P4 and Jumper P7 (see Table 1) and connected to the J9 and J10 subminiature Type A (SMA) connectors (see Table 2). A 3.3 V power supply can be applied to Side 1 and/or Side 2 of the [ADN4654/ADN4655/ADN4656](#) by removing Jumper P4 (Side 1) and Jumper P7 (Side 2). If a 2.5 V supply is connected to the board, the relevant jumper must be inserted (P4 for Side 1 and P7 for Side 2). At 300 MHz with a load resistance of 100  $\Omega$ , the maximum operating current from each power supply is 80 mA.

When using a 3.3 V power supply,  $V_{IN1}$  and  $V_{DD1}$  (Pin 1 and Pin 3 on the [ADN4654/ADN4655/ADN4656](#)) are bypassed to  $GND_1$  using 1  $\mu\text{F}$  capacitors.  $V_{IN2}$  and  $V_{DD2}$  (Pin 20 and Pin 18 on the [ADN4654/ADN4655/ADN4656](#)) are bypassed to  $GND_2$  using 1  $\mu\text{F}$  capacitors. When using a 2.5 V power supply,  $V_{IN1}$  or  $V_{IN2}$  is connected directly to  $V_{DD1}$  or  $V_{DD2}$  by shorting Jumper P4 or Jumper P7, respectively. Both  $V_{DD1}$  pins (Pin 3 and Pin 9) are also bypassed to  $GND_1$  with 0.1  $\mu\text{F}$  capacitors. Both  $V_{DD2}$  pins (Pin 12 and Pin 18) are also bypassed to  $GND_2$  with 0.1  $\mu\text{F}$  capacitors.

An example operation of the EVAL-ADN4654EB1Z is shown in Figure 4 (EVAL-ADN4655EB1Z and EVAL-ADN4656EB1Z output signals are similar). SMA connectors reveal all LVDS inputs and outputs for the EVAL-ADN4654EB1Z, the EVAL-ADN4655EB1Z, and the EVAL-ADN4656EB1Z (see Table 3). To evaluate Channel 1 on the EVAL-ADN4654EB1Z or the EVAL-ADN4655EB1Z, connect a signal generator to the board using the J1 connector and J2 connector and set up a 300 MHz square wave clock with an amplitude of 350 mV and an offset of 1.2 V. Connect the oscilloscope directly to the J5 connector and J6 connector to perform timing measurements, including propagation delay, skew, and jitter. Subtract the effect of printed circuit board (PCB) traces from the connectors to the device by measuring the direct line between J22/J24 and J21/J23. Refer to Table 3 for the connectors to use to evaluate Channel 1 on the EVAL-ADN4656EB1Z.

A plot of the oscilloscope connected via the J5 connector and J6 connector is shown in Figure 2. Channel 3 (green) and Channel 4 (purple) show the J5 connector and J6 connector separately (single-ended) with the differential signal (orange). Operation of the second isolated LVDS channel with the signal generator (same input signal conditions as Channel 1) and oscilloscope connected to the appropriate connectors is shown in Table 3.

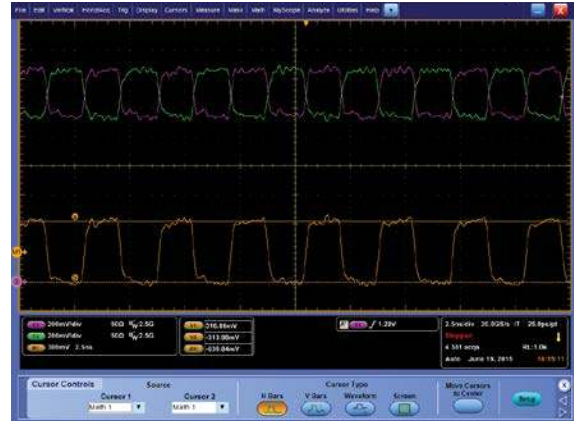


Figure 2.  $D_{OUT1-}$  and  $D_{OUT1+}$  with a 300 MHz Clock, Single-Ended and Differential

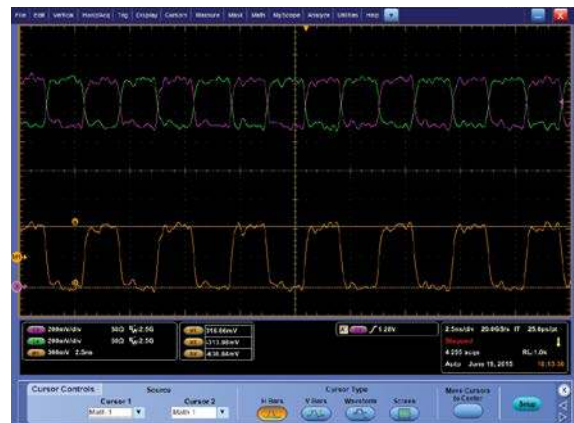


Figure 3.  $D_{OUT2-}$  and  $D_{OUT2+}$  with a 300 MHz Clock, Single-Ended and Differential

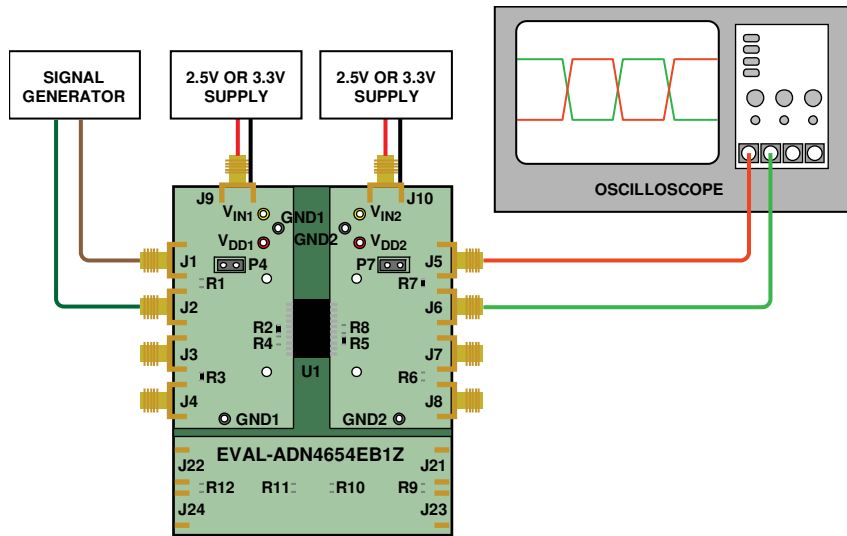


Figure 4. Basic LVDS Isolator Evaluation Board Operation for the EVAL-ADN4654EB1Z

Table 1. Jumper Configuration for EVAL-ADN4654EB1Z, EVAL-ADN4655EB1Z, and EVAL-ADN4656EB1Z

Jumper	Position	Description
P4	Open	3.3 V power supply connected to Connector J9 for $V_{IN1}$
	Closed	2.5 V power supply connected to Connector J9, $V_{IN1}$ shorted to $V_{DD1}$
P7	Open	3.3 V power supply connected to Connector J10 for $V_{IN2}$
	Closed	2.5 V power supply connected to Connector J10, $V_{IN2}$ shorted to $V_{DD2}$

Table 2. Connector Descriptions for EVAL-ADN4654EB1Z, EVAL-ADN4655EB1Z, and EVAL-ADN4656EB1Z

Connector	Description
Side 1	
J9	Power supply, Side 1, 3.3 V (Jumper P4 open) or 2.5 V (Jumper P4 closed)
J22	Connects to Connector J21 (test trace for calibration)
J24	Connects to Connector J23 (test trace for calibration)
Side 2	
J10	Power supply, Side 2, 3.3 V (Jumper P7 open) or 2.5 V (Jumper P7 closed)
J21	Connects to Connector J22 (test trace for calibration)
J23	Connects to Connector J24 (test trace for calibration)

Table 3. I/O Connector Descriptions for EVAL-ADN4654EB1Z, EVAL-ADN4655EB1Z, and EVAL-ADN4656EB1Z

Connector	EVAL-ADN4654EB1Z Description	EVAL-ADN4655EB1Z Description	EVAL-ADN4656EB1Z Description
J1	$D_{IN1+}$ , noninverted LVDS input for Channel 1	$D_{IN1+}$ , noninverted LVDS input for Channel 1	$D_{OUT1+}$ , noninverted LVDS output for Channel 1
J2	$D_{IN1-}$ , inverted LVDS input for Channel 1	$D_{IN1-}$ , inverted LVDS input for Channel 1	$D_{OUT1-}$ , inverted LVDS output for Channel 1
J3	$D_{IN2+}$ , noninverted LVDS input for Channel 2	$D_{OUT2+}$ , noninverted LVDS output for Channel 2	$D_{IN2+}$ , noninverted LVDS input for Channel 2
J4	$D_{IN2-}$ , inverted LVDS input for Channel 2	$D_{OUT2-}$ , inverted LVDS output for Channel 2	$D_{IN2-}$ , inverted LVDS input for Channel 2
J5	$D_{OUT1+}$ , noninverted LVDS output for Channel 1	$D_{OUT1+}$ , noninverted LVDS output for Channel 1	$D_{IN1+}$ , noninverted LVDS input for Channel 1
J6	$D_{OUT1-}$ , inverted LVDS output for Channel 1	$D_{OUT1-}$ , inverted LVDS output for Channel 1	$D_{IN1-}$ , inverted LVDS input for Channel 1
J7	$D_{OUT2+}$ , noninverted LVDS output for Channel 2	$D_{IN2+}$ , noninverted LVDS input for Channel 2	$D_{OUT2+}$ , noninverted LVDS output for Channel 2
J8	$D_{OUT2-}$ , inverted LVDS output for Channel 2	$D_{IN2-}$ , inverted LVDS input for Channel 2	$D_{OUT2-}$ , inverted LVDS output for Channel 2

EVALUATION BOARD SCHEMATICS AND ARTWORK

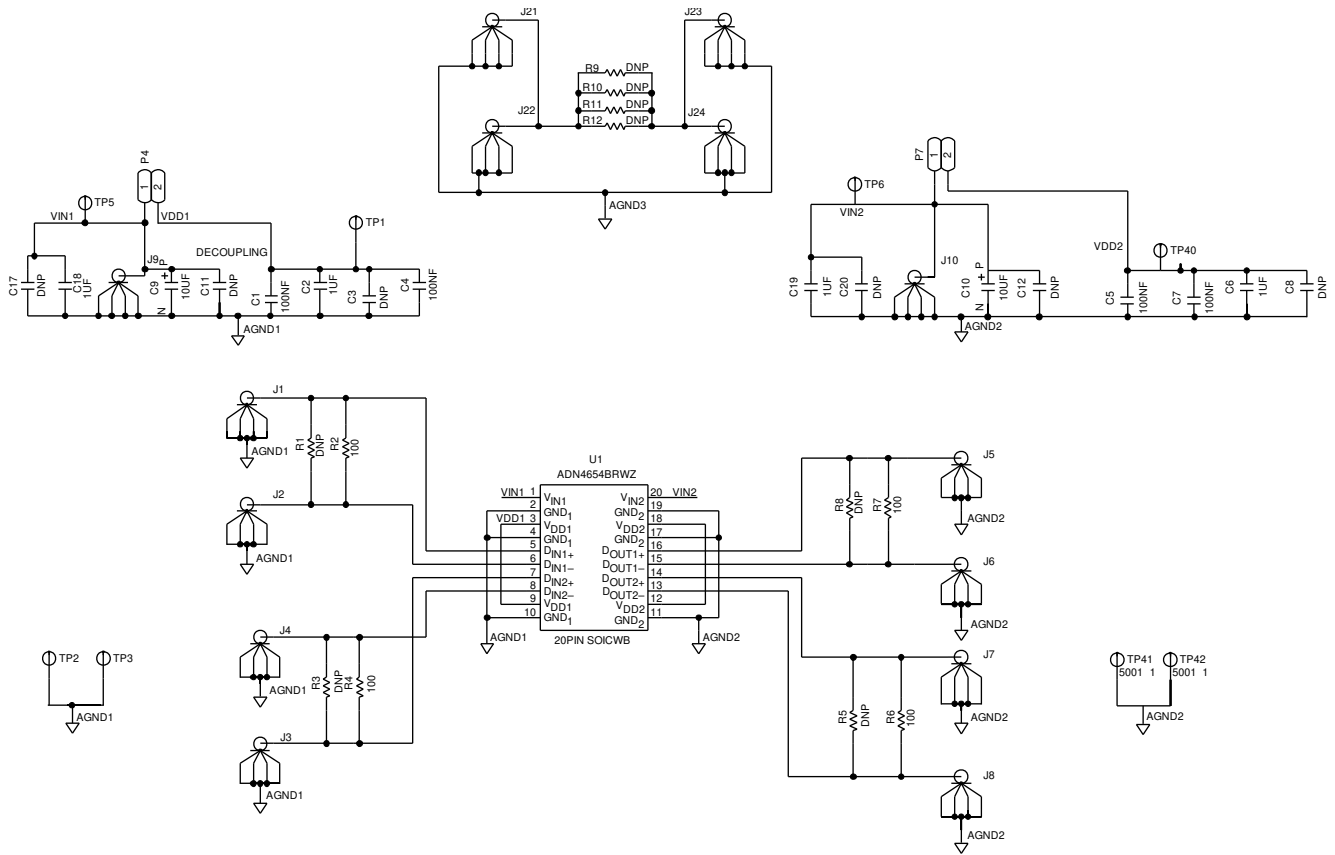


Figure 5. EVAL-ADN4654EB1Z Schematic

17014-005

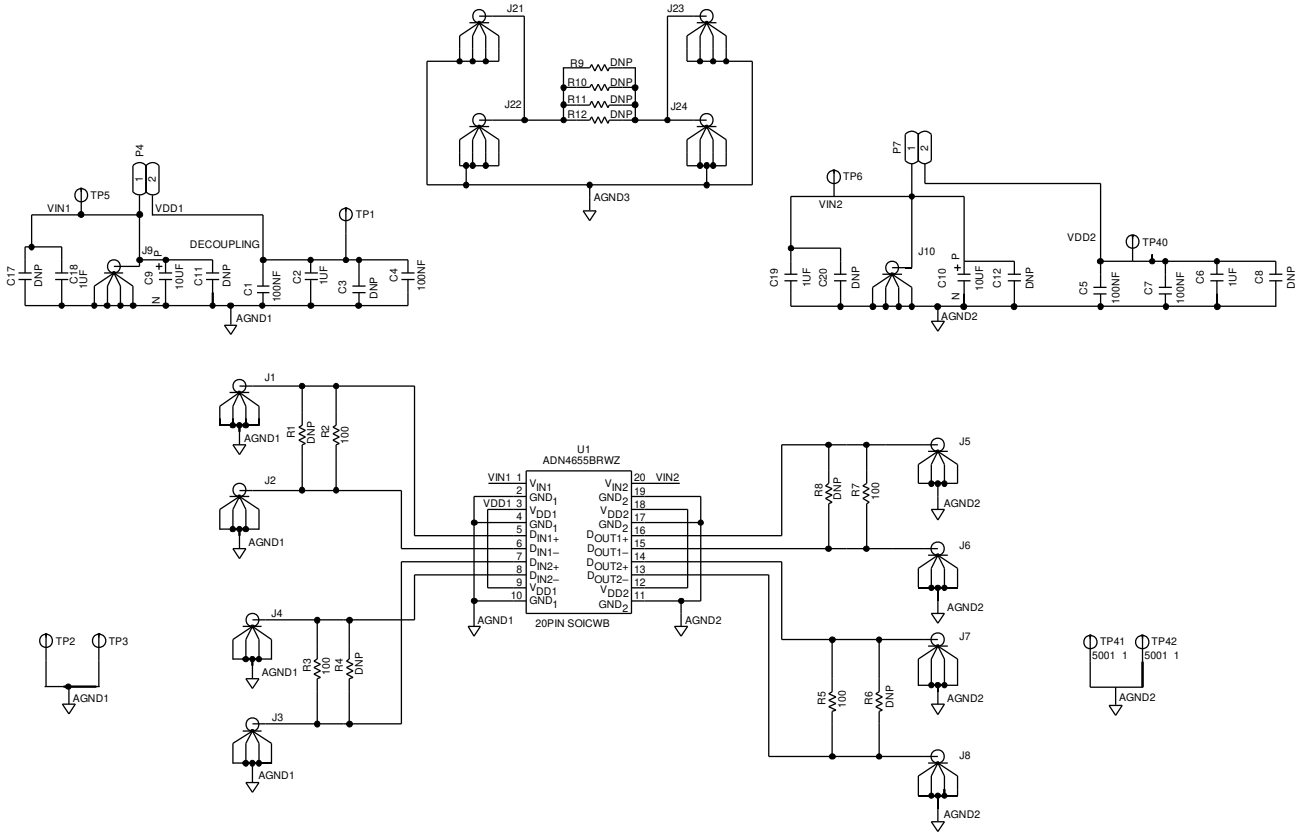


Figure 6. EVAL-ADN4655EB1Z Schematic

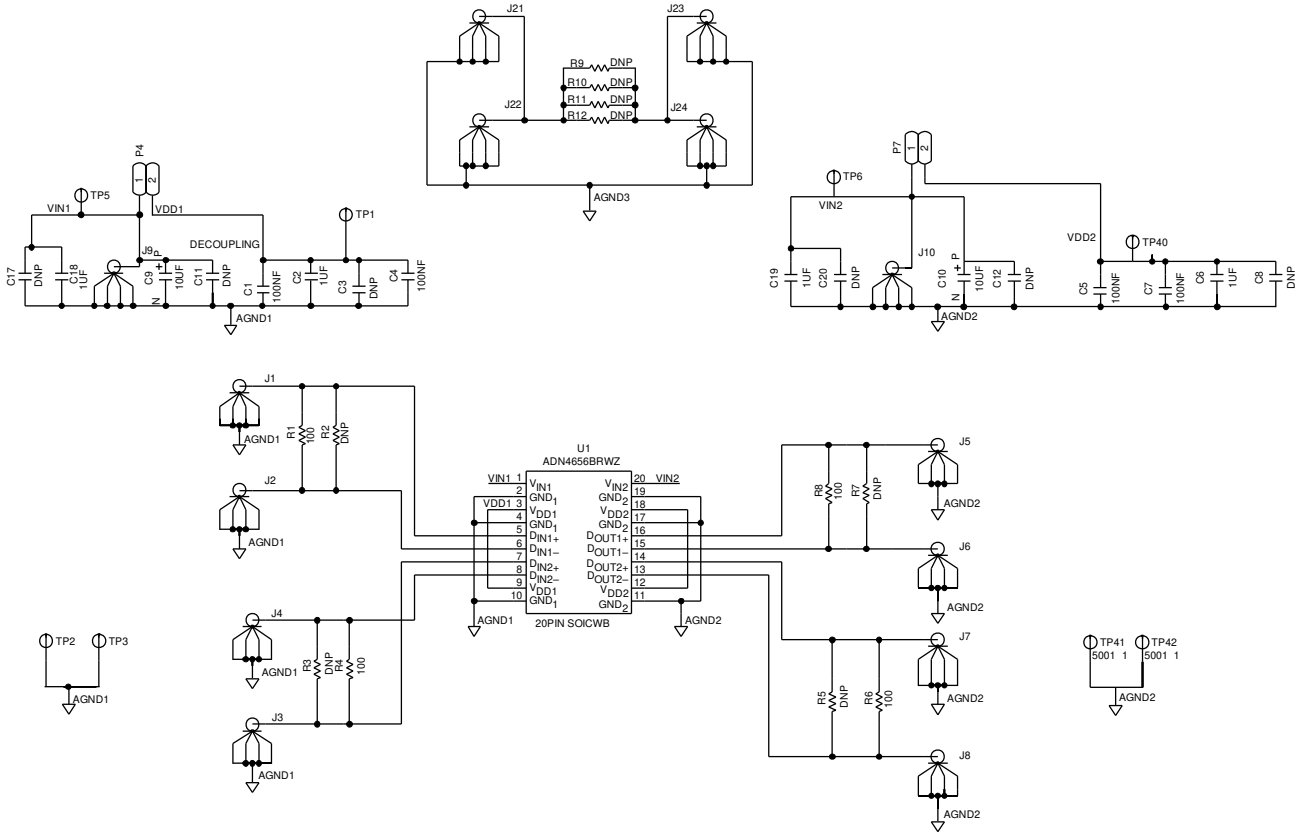


Figure 7. EVAL-ADN4656EB1Z Schematic

17014-005

17014-205

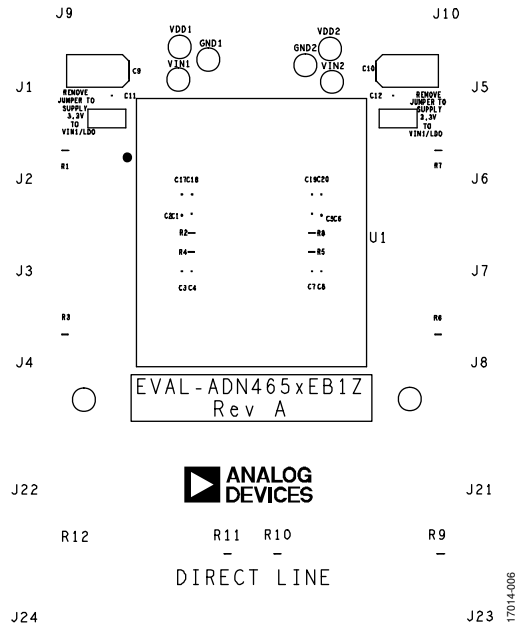


Figure 8. EVAL-ADN4654EB1Z/EVAL-ADN4655EB1Z/EVAL-ADN4656EB1Z Silkscreen

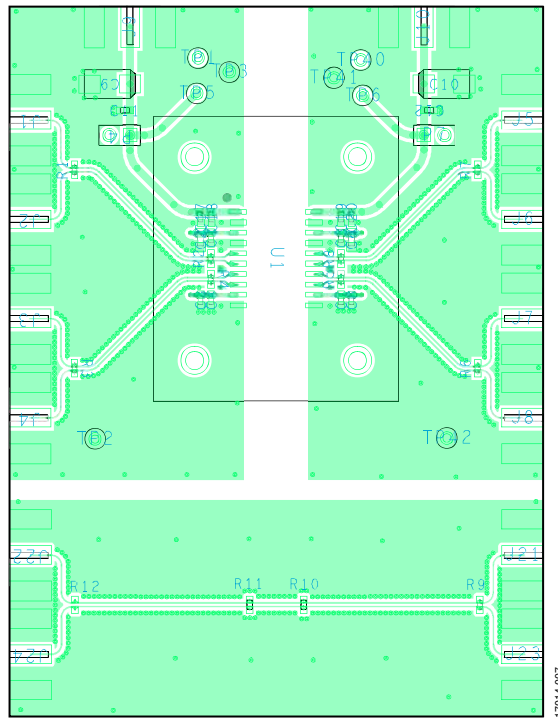


Figure 9. EVAL-ADN4654EB1Z/EVAL-ADN4655EB1Z/EVAL-ADN4656EB1Z Component Side

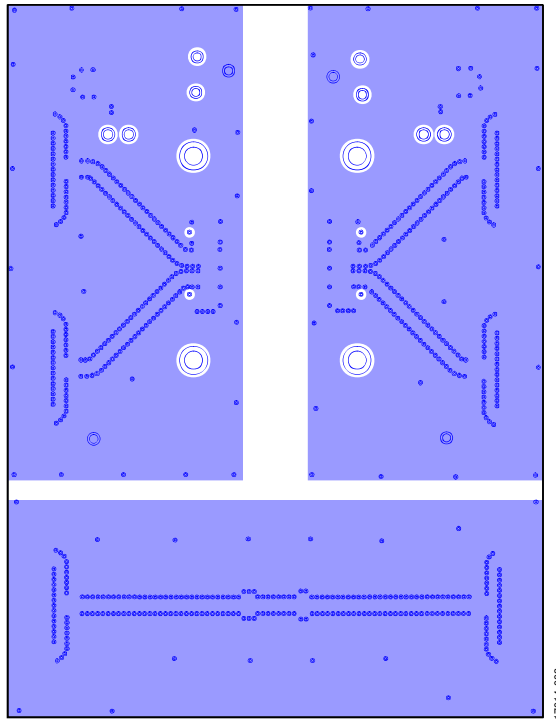


Figure 10. EVAL-ADN4654EB1Z/EVAL-ADN4655EB1Z/EVAL-ADN4656EB1Z Inner Layer 2, Ground

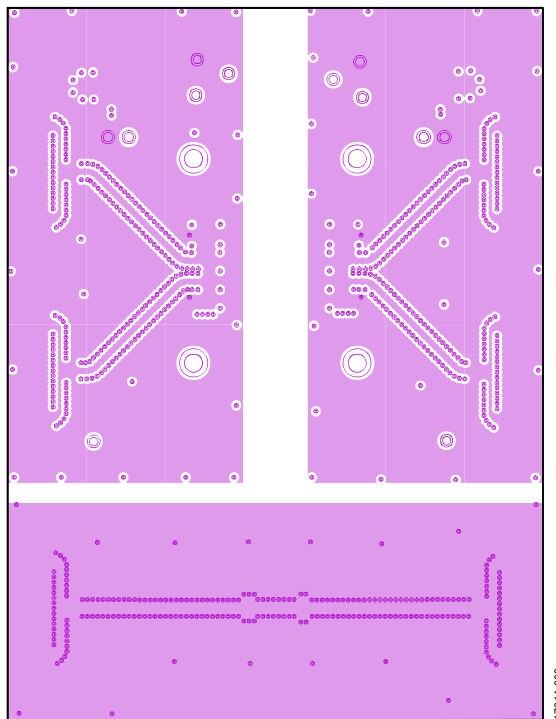


Figure 11. EVAL-ADN4654EB1Z/EVAL-ADN4655EB1Z/EVAL-ADN4656EB1Z Inner Layer 3, Power



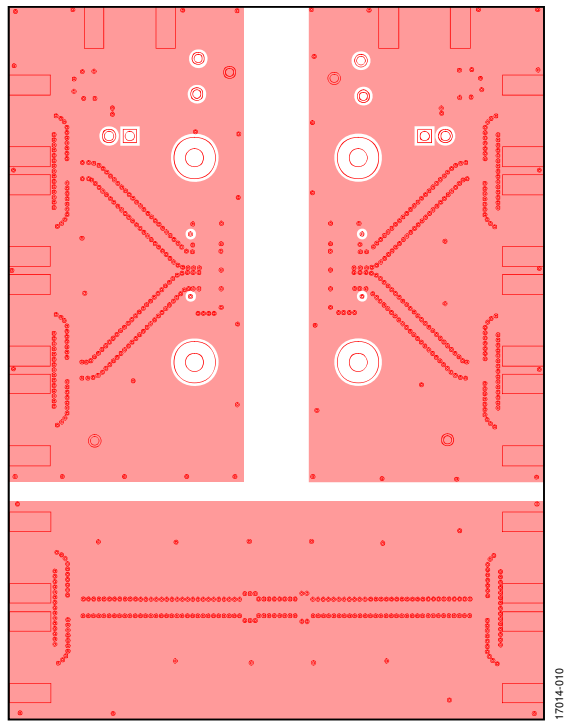


Figure 12. EVAL-ADN4654EB1Z/EVAL-ADN4655EB1Z/EVAL-ADN4656EB1Z Solder Side

## ORDERING INFORMATION

## BILL OF MATERIALS

Table 4. EVAL-ADN4654EB1Z Bill of Materials

Quantity	Reference Designator	Description	Manufacturer	Part Number
4	C1, C4, C5, C7	Capacitors, 100 nF, 0402	Multicomp	MC0402X104K100CT
2	C2, C6	Capacitors, 1 $\mu$ F, 0603	Multicomp	MC0603X105K100CT
6	C3, C8, C11, C12, C17, C20	Capacitors, 0402	Not fitted	Not applicable
2	C9, C10	Capacitors, tantalum, 10 $\mu$ F, Case C	AVX	TAJC106K016RNJ
2	C18, C19	Capacitors, 1 $\mu$ F, 0402	Multicomp	MC0402X105K6R3CT
10	J1 to J10	Connectors, SMA, edge	Johnson	142-0701-801
4	J21 to J24	Connectors, SMA, edge	Not fitted	Not applicable
2	P4, P7	2-pin, header and jumper	TE Connectivity	826926-2 and 3M/969102-0000-DA
8	R1, R3, R5, R8 to R12	Resistors, 0402	Not fitted	Not applicable
4	R2, R4, R6, R7	Resistors, 100 $\Omega$ , 0402	Multicomp	MCMR04X1000FTL
2	TP1, TP40	Test points, yellow	Vero	20-313140
4	TP2, TP3, TP41, TP42	Test points, black	Vero	20-2137
2	TP5, TP6	Test points, red	Vero	20-313137
1	U1	<a href="#">ADN4654</a> LVDS gigabit isolator	Analog Devices	<a href="#">ADN4654BRWZ</a>

Table 5. EVAL-ADN4655EB1Z Bill of Materials

Quantity	Reference Designator	Description	Manufacturer	Part Number
4	C1, C4, C5, C7	Capacitors, 100 nF, 0402	Multicomp	MC0402X104K100CT
2	C2, C6	Capacitors, 1 $\mu$ F, 0603	Multicomp	MC0603X105K100CT
6	C3, C8, C11, C12, C17, C20	Capacitors, 0402	Not fitted	Not applicable
2	C9, C10	Capacitors, tantalum, 10 $\mu$ F, Case C	AVX	TAJC106K016RNJ
2	C18, C19	Capacitors, 1 $\mu$ F, 0402	Multicomp	MC0402X105K6R3CT
10	J1 to J10	Connectors, SMA, edge	Johnson	142-0701-801
4	J21 to J24	Connectors, SMA, edge	Not fitted	Not applicable
2	P4, P7	2-pin, header and jumper	TE Connectivity	826926-2 and 3M/969102-0000-DA
8	R1, R4, R6, R8 to R12	Resistors, 0402	Not fitted	Not applicable
4	R2, R3, R5, R7	Resistors, 100 $\Omega$ , 0402	Multicomp	MCMR04X1000FTL
2	TP1, TP40	Test points, yellow	Vero	20-313140
4	TP2, TP3, TP41, TP42	Test points, black	Vero	20-2137
2	TP5, TP6	Test points, red	Vero	20-313137
1	U1	<a href="#">ADN4655</a> LVDS gigabit isolator	Analog Devices	<a href="#">ADN4655BRWZ</a>

Table 6. EVAL-ADN4656EB1Z Bill of Materials

Quantity	Reference Designator	Description	Manufacturer	Part Number
4	C1, C4, C5, C7	Capacitors, 100 nF, 0402	Multicomp	MC0402X104K100CT
2	C2, C6	Capacitors, 1 $\mu$ F, 0603	Multicomp	MC0603X105K100CT
6	C3, C8, C11, C12, C17, C20	Capacitors, 0402	Not fitted	Not applicable
2	C9, C10	Capacitors, tantalum, 10 $\mu$ F, Case C	AVX	TAJC106K016RNJ
2	C18, C19	Capacitors, 1 $\mu$ F, 0402	Multicomp	MC0402X105K6R3CT
10	J1 to J10	Connectors, SMA, edge	Johnson	142-0701-801
4	J21 to J24	Connectors, SMA, edge	Not fitted	Not applicable
2	P4, P7	2-pin, header and jumper	TE Connectivity	826926-2 and 3M/969102-0000-DA
8	R2, R3, R5, R7, R9 to R12	Resistors, 0402	Not fitted	Not applicable
4	R1, R4, R6, R8	Resistors, 100 $\Omega$ , 0402	Multicomp	MCMR04X1000FTL
2	TP1, TP40	Test points, yellow	Vero	20-313140
4	TP2, TP3, TP41, TP42	Test points, black	Vero	20-2137
2	TP5, TP6	Test points, red	Vero	20-313137
1	U1	<a href="#">ADN4656</a> LVDS gigabit isolator	Analog Devices	<a href="#">ADN4656BRWZ</a>

## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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UG17014-0-6/19(B)



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