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TI Precision Designs: TIPD115 Verified Design

18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise

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Circuit Description

This design is for an 18-bit data acquisition block at 1MSPS throughput optimized for the lowest distortion and noise performance. The circuit is realized with an 18-bit successive-approximation-resistor (SAR) analog-to-digital converter (ADC), a fully differential input driver and a high precision reference and reference driver. The design details the process for optimizing the precision front end drive circuit as well as the reference circuit to achieve excellent dynamic performance with the ADS8881 while consuming low power.

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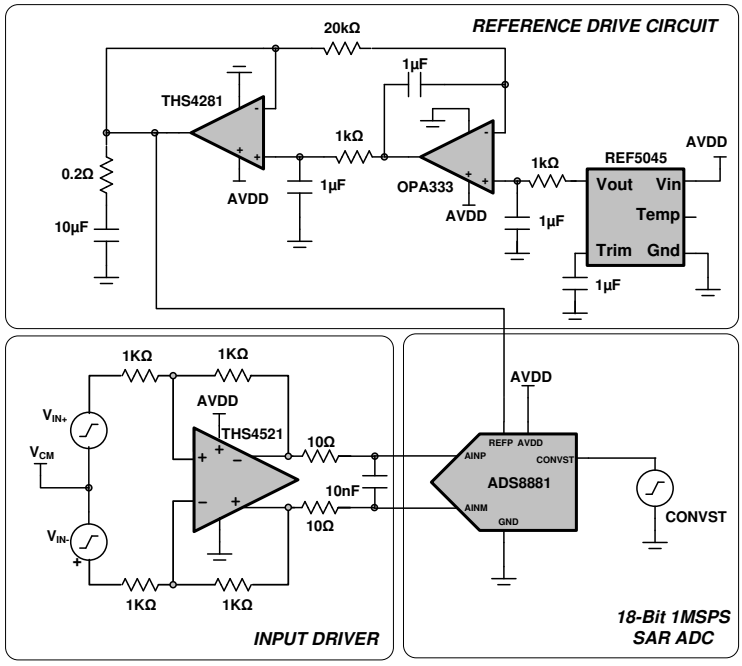

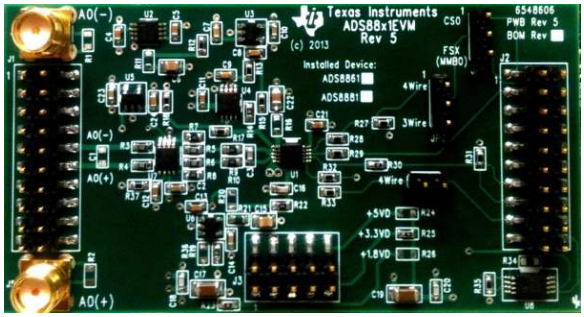

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1 Design Summary

The primary objective is to design a lowest distortion and noise data acquisition block with low power consumption using the 18-bit ADS8881 at a throughput of 1MSPS for a 10 kHz full-scale pure sine wave input. The design requirements for this block design are:

- System Supply Voltage: 5 V dc
- ADC Supply Voltage: 3.3 V dc
- ADC Sampling Rate: 1MSPS
- ADC Reference Voltage (VREF): 4.5 V dc
- ADC Input Signal: A differential input signal with amplitude of V_{pk} = 4.315 V (-0.4 dBFS to avoid clipping) and frequency, f_{IN} = 10 kHz are applied to each differential input of the ADC

The design goals and performance are summarized in Table 1.

Table 1: Comparison of design goals, simulation and measured performance

Parameter	Goal	Simulated	Measured
Total Power	< 40 mW	NA	39.4 mW
Signal to Noise Ratio (SNR)	> 98 dB	NA	98.74 dB
Total Harmonic Distortion (THD)	< -110 dB	NA	-110.04 dB
Effective Number of Bits (ENOB)	16	NA	16.05
Integral Non-Linearity (INL)	< ±1.5 LSB	NA	< ±1.5 LSB

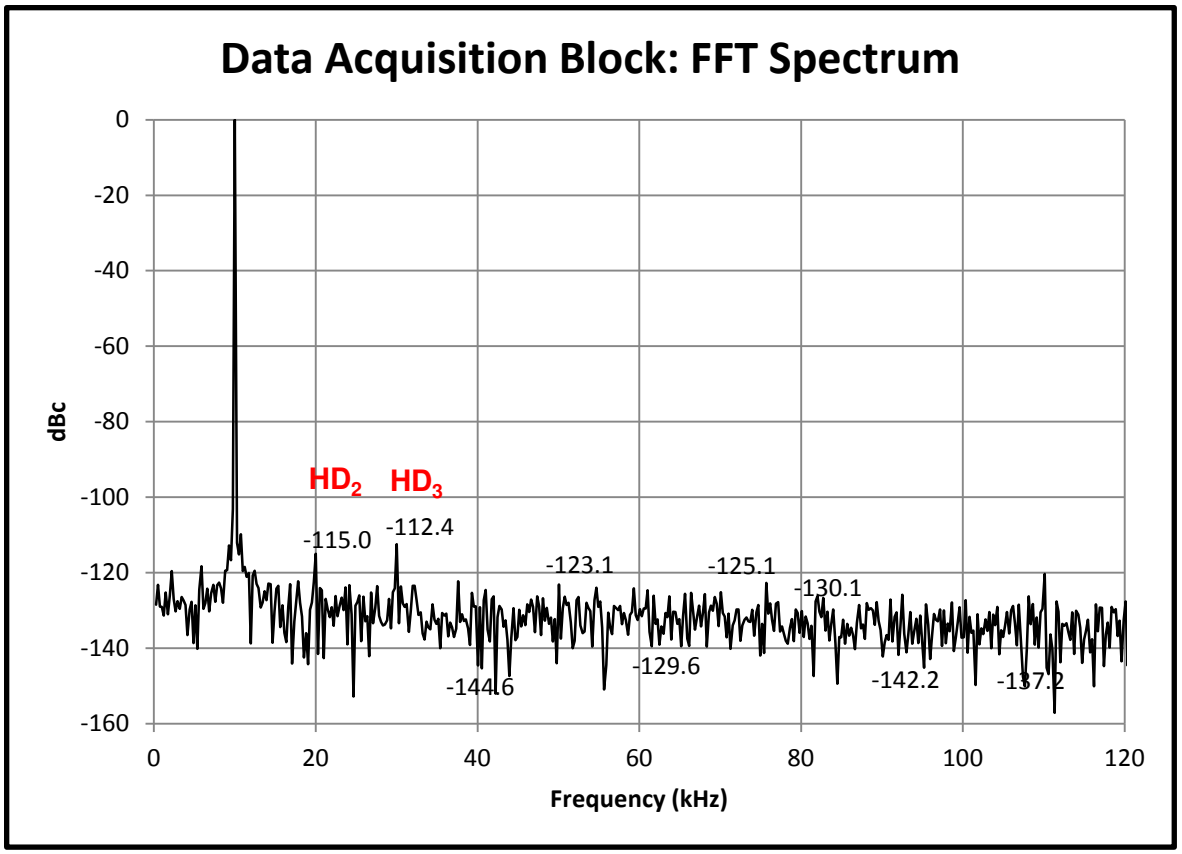

Figure 1: Measurement Result for FFT of the Data Acquisition Block

2 Theory of Operation

The two primary design considerations to maximize the performance of a high-resolution SAR ADC are the input driver and the reference driver design. The overall system block diagram is shown in Figure 2. The block-diagram comprises of the critical analog circuit blocks, the input driver, anti-aliasing filter and the reference driver. Each analog circuit block should be carefully designed based on the ADC performance specifications in order to maximize the distortion and noise performance of the data acquisition system while consuming low power. The diagram includes the most important specifications for each individual analog block.

This design systematically approaches the design of each analog circuit block to achieve a 16-bit low noise and distortion data acquisition system for a 10 kHz sinusoidal input signal. The first step in the design requires an understanding of the requirement of extremely low distortion input driver amplifier. This will help in the decision of an appropriate input driver configuration and selection of an input amplifier to meet the system requirements. The next important step is the design of the anti-aliasing RC-filer to attenuate ADC kick-back noise while maintaining the amplifier stability. The final design challenge is to design a high precision reference driver circuit, which would provide the required value V_{REF} with low offset, drift and noise contributions.

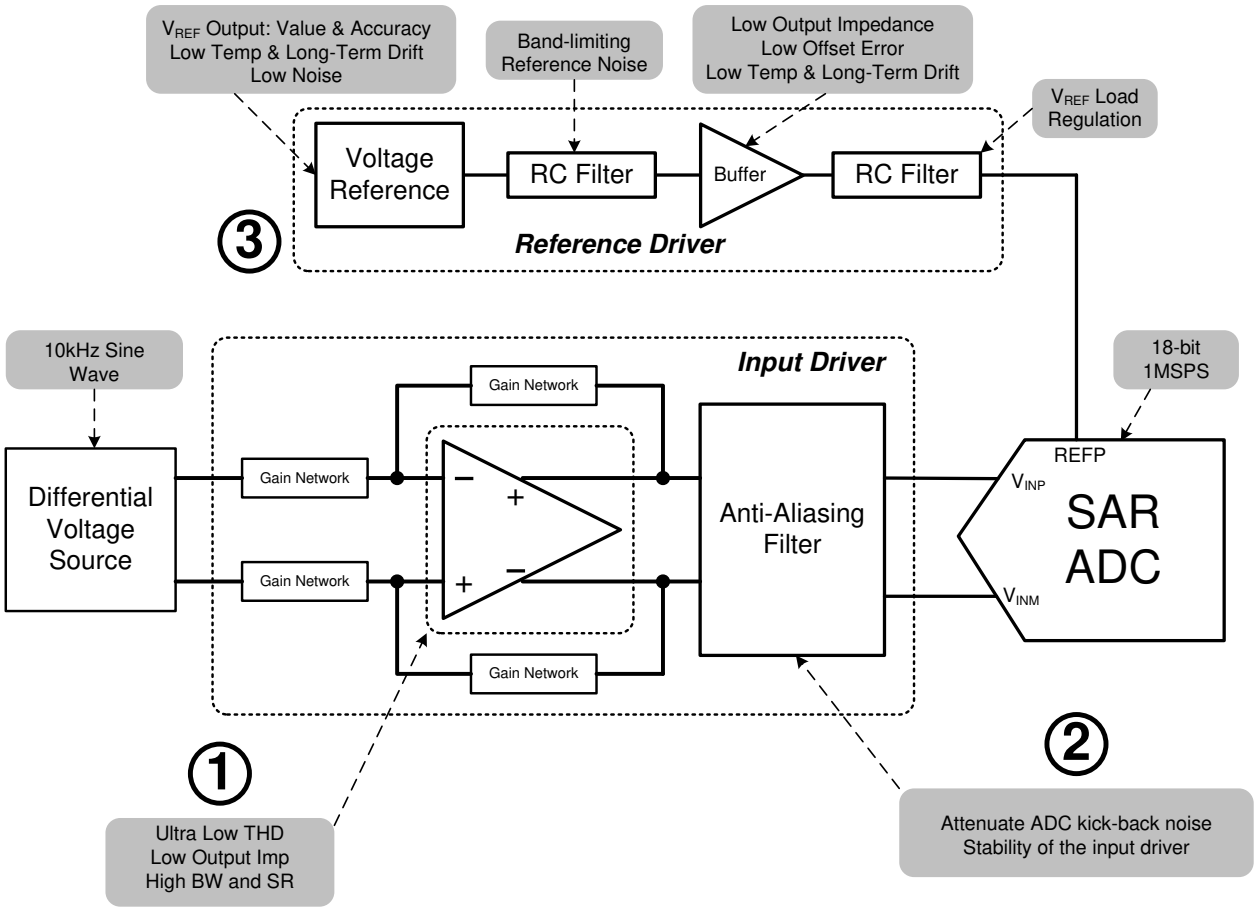

Figure 2: Block Diagram Highlighting Primary Design Criteria for this DAQ Block

2.1 Understanding ADC Dynamic Performance

The input driver circuit for an ADC consists of two parts: driving amplifier and a fly wheel RC filter. The amplifier can be used for signal conditioning of the input voltage and its high input impedance and low output impedance provides a buffer between the signal source and the ADC input. The RC filter helps to attenuate the kick-back noise from the switched-capacitor input stage of the ADC as well as acts as an anti-aliasing filter to band-limit the wideband noise contributed by the front-end circuit.

The main ac specifications under consideration for this design are SNR, THD, SINAD and ENOB. Essentially, all these parameters are different ways of quantifying the noise and distortion performance of an ADC based on a Fast-Fourier Transform (FFT) analysis. A typical FFT plot for an ADC is shown in Figure 3.

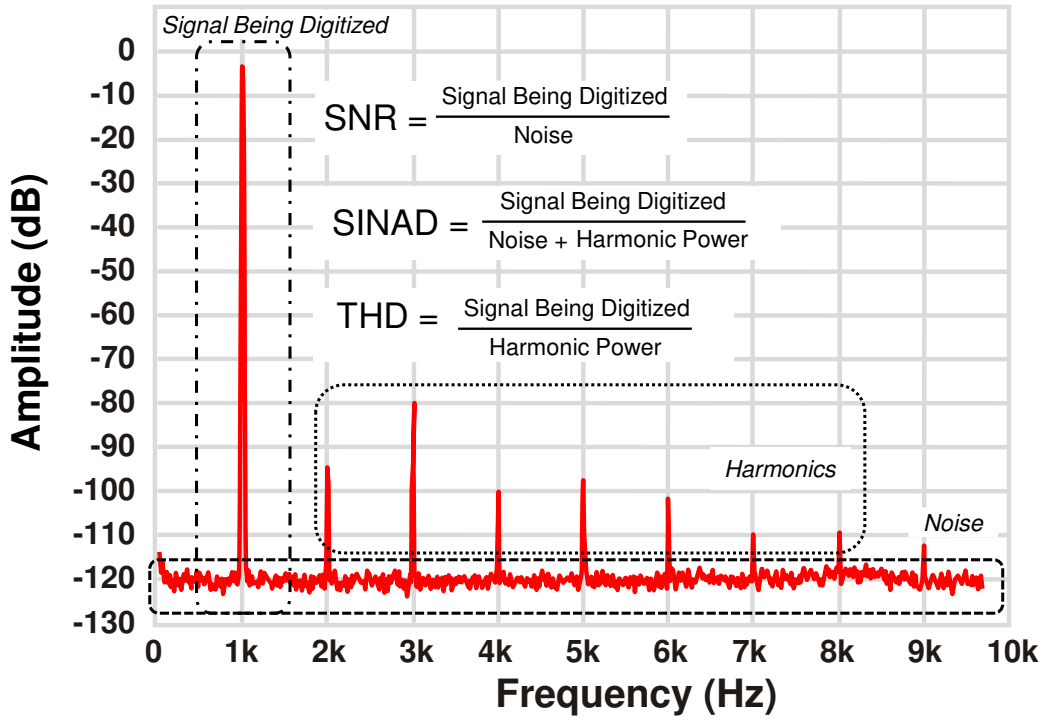

Figure 3: AC Specifications of an ADC

2.1.1 Signal-to-Noise Ratio (SNR)

SNR provides insight into the total noise of the system. The total noise of the data acquisition system is the root-sum-square (rss) of the front-end amplifier noise ($V_{n\_AMP\_RMS}$) and the ADC noise ($V_{n\_ADC\_RMS}$). The ADC noise includes the quantization noise as well as the noise contributed by ADC internal circuitry. The total noise contributions from all these sources, denoted as $V_{n\_TOT\_RMS}$ are referred to the input of the ADC for calculating total SNR of the system (SNR_{SYS}).

$$V_{n\_TOT\_RMS} = \sqrt{V_{n\_AMP\_RMS}^2 + V_{n\_ADC\_RMS}^2} \quad (1)$$

$$SNR_{SYS} = \frac{V_{SIG\_RMS}}{V_{n\_TOT\_RMS}} \quad (2)$$

2.1.2 Total Harmonic Distortion (THD)

THD is defined as the ratio of the rss of all harmonic components (generally 9 harmonics are used) to the power of the fundamental signal frequency. It is generally specified with an input signal near full-scale (FS), but in this design the input is kept 0.4dB below FS to prevent clipping. If the root-mean-square (rms) value of input signal is denoted as V_{SIG_RMS} and the power in n^{th} harmonic is denoted by $V_{HAR\_n\_RMS}$, then the total harmonic distortion ($V_{HAR\_TOT\_RMS}$) and THD can be calculated as:

$$V_{HAR\_TOT\_RMS} = \sqrt{V_{HAR\_1\_RMS}^2 + V_{HAR\_2\_RMS}^2 + \ldots\ldots + V_{HAR\_9\_RMS}^2} \tag{3}$$

$$THD = \frac{V_{SIG\_RMS}}{V_{HAR\_TOT\_RMS}} \tag{4}$$

2.1.3 Signal-to-Noise-and-Distortion Ratio (SINAD)

SINAD combines the effect of distortion and noise to provide a cumulative measure of the overall dynamic performance of the system.

$$SINAD_{SYS} = \frac{V_{SIG\_RMS}}{\sqrt{V_{n\_TOT\_RMS}^2 + V_{HAR\_TOT\_RMS}^2}} \tag{5}$$

2.1.4 Effective Number of Bits (ENOB)

ENOB is an effective measurement of the quality of a digitized signal from an ADC by specifying the number of bits above the noise floor. For an ideal N-bit ADC with only quantization noise, the SNR (in dB) can be calculated as:

$$SNR = 6.02 \times N + 1.76 \tag{6}$$

$$N = \frac{SNR - 1.76}{6.02} \tag{7}$$

This definition for ENOB can be extrapolated to indicate the overall dynamic performance of a data acquisition system by substituting SNR with $SINAD_{SYS}$ from equation

$$ENOB = \frac{SINAD_{SYS} - 1.76}{6.02} \tag{8}$$

Therefore, in order to maximize the performance of a high precision ADC, it is important to keep both the distortion and noise contribution from the front-end circuit at an extremely low-level. Based on equation 8, the minimum THD and SNR requirements to achieve an ENOB 16-bit data acquisition system are calculated in Figure 4.

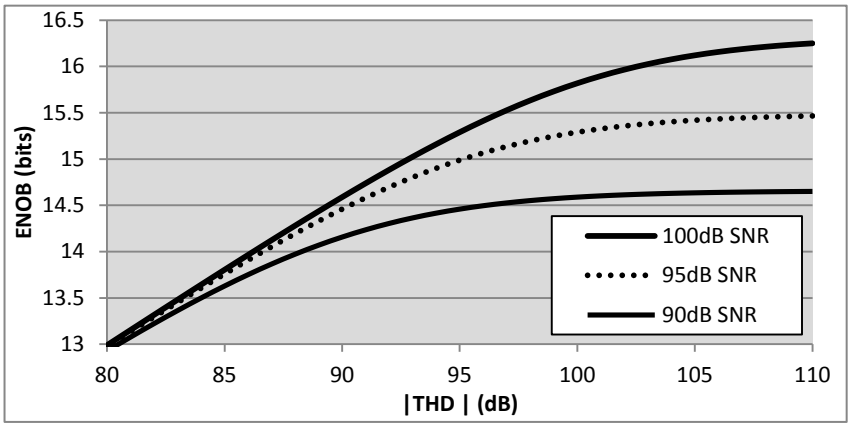

Figure 4: ENOB versus THD and SNR

2.2 Low Distortion Input Driver Design

In designing a very low distortion data acquisition block it is important to understand the sources of non-linearity. Both the ADC and the input driver introduce non-linearity in a data acquisition block. To achieve the lowest distortion, the input driver for a high performance SAR ADC needs to have a distortion that is negligible against the ADC distortion. This requires the input driver distortion to be 10dB lower than the ADC THD. This stringent requirement ensures that overall THD of the system is not degraded by more than -0.5 dB.

$$THD_{AMP} < THD_{ADC} - 10\,dB \tag{9}$$

It is therefore important to choose an amplifier that meets the above criteria to avoid the system THD from being limited by the input driver. The amplifier non-linearity in a feedback system is dependent on the available loop gain. The block diagram modeling the non-linearity is shown in Figure 5 below.

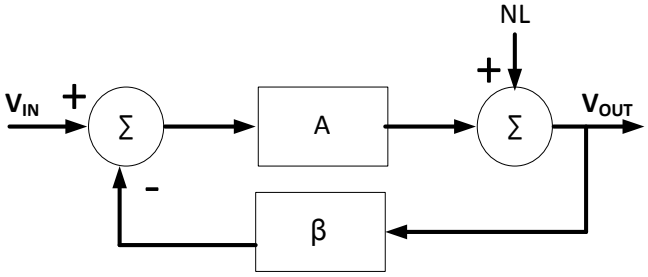

Figure 5: Non Linearity in a Feedback System

$$V_{out} = \frac{Vin \times A}{1 + A\beta} + \frac{NL}{1 + A\beta} \tag{10}$$

The non-linearity (NL) in the above feedback system is divided by the loop gain (Aβ). The open loop gain (A) of the amplifier is a function of frequency and typically degrades at -20dB/decade. This reduction of open loop gain at higher frequencies causes the THD to degrade at high frequencies. To maintain a low THD at higher frequencies it is therefore important to choose an amplifier with high gain bandwidth product (GBW). This will ensure that there is sufficient loop gain available at higher input frequencies to maintain the minimum required THD specification.

Most amplifier datasheet specify THD+N as a measured specification. It is important to understand that in some amplifiers the noise dominates the THD+N specification. However, you can calculate just the THD specification of the amplifier based on the 2nd and 3rd harmonic distortion (HD_2 and HD_3 respectively) using Equation 11.

$$THD(dB) = 10\log\left(10^{\frac{HD2}{10}} + 10^{\frac{HD3}{10}}\right) \tag{11}$$

The distortion from the input driver however is not limited to the amplifier distortion specification but also the amplifier configuration. The input driver can be configured either in an inverting or a non-inverting configuration as shown in the Figure 6.

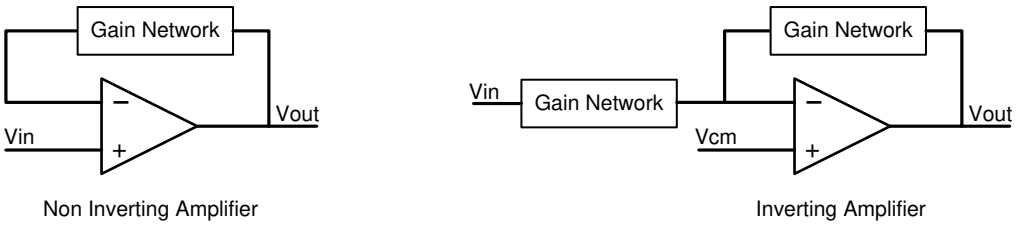

Figure 6: Non-Inverting and Inverting Amplifier Configurations

The common mode of the input driver in a non-inverting configuration follows the input signal. This adds a constraint on the input amplifier to have rail-to-rail inputs to allow full scale input signals. Furthermore, the movement of the common mode of the input amplifier introduces additional common mode dependent distortion at the output of the amplifier. In comparison, in the inverting configuration the common mode is fixed and thus does not require rail-to-rail inputs and also does not introduce any additional common mode dependent distortion. Therefore, in this design the input driver amplifier is configured in an inverting amplifier configuration. This architectural choice helps improve the THD performance of the system significantly. However, it does bring other trade-offs which will be explained later.

2.3 Low Distortion Anti-Aliasing Filter Design

The conversion of analog to digital signals requires sampling an input at a constant rate. If the input contains high frequency content higher than half the sampling rate, the high frequency content would be folded back into the low frequency spectrum and digitized. This is called aliasing. Therefore an anti-aliasing filter is required to remove this harmonic content. An anti-alias filter is designed as a low pass filter with its corner frequency being equal to the sampling rate. Designing the anti-aliasing filter corner frequency at the sampling rate ensures that the input signal attenuation is kept to a maximum of 1dB while filtering high frequency content from folding back. The anti-alias filter also helps limit the bandwidth and noise at the output of the input driver amplifier.

The inputs of the SAR ADC are shown in Figure 7 introduce transient distortion during the acquisition period. The input driver is not an ideal source with zero ohms of output impedance and infinite current drive and thus the anti-alias filter helps with a few important design requirements. The capacitor C_{FLT} helps to reduce the kick-back noise at the ADC input and provides a charge bucket to quickly charge the input capacitor C_{SH} during the sampling process. The value of the capacitor C_{FLT} should be chosen such that when switch SW_{SAMP} closes, the voltage droop (ΔV_{FLT}) on C_{FLT} is less than 5% of the input voltage.

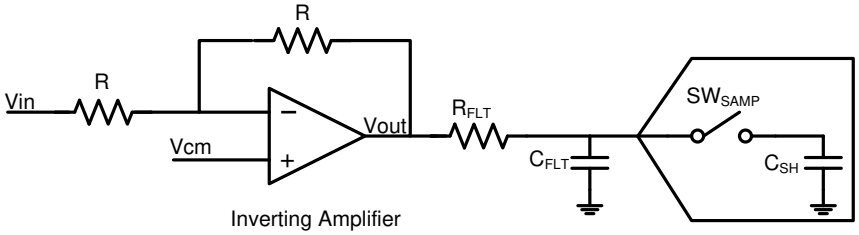

Figure 7: Simplified Schematic of Single Ended Input Sampling Stage

Charge required for ADC sampling capacitor, $Q_{IN} = C_{SH} \times V_{REF}$

Charge supplied by filter cap, $Q_{FLT} = C_{FLT} \times \Delta V_{FLT} \leq C_{FLT} \times (0.05 \times V_{REF})$

By the principle of charge conservation:

$$\begin{aligned} Q_{IN} &= Q_{FLT} \\ C_{FLT} \times (0.05 \times V_{REF}) &\geq C_{SH} \times V_{REF} \end{aligned} \quad (12)$$

$$C_{FLT} \geq 20 \times C_{SH} \quad (13)$$

At this point, it is important to understand the trade-offs involved in selecting the values of C_{FLT} and R_{FLT}. If the value of C_{FLT} is high, it provides better attenuation against the kick-back noise when the sampling switch closes. However, C_{FLT} cannot be made arbitrarily high because it degrades the phase margin of the driving amplifier, thus making it unstable. The series resistor R_{FLT} acts as an isolation resistor, which helps to stabilize the driving amplifier. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but degrades ac performance and should be balanced with the amplifier stability to ensure that the distortion does not exceed the required specifications. The distortion happens due to the non-linear input impedance of the ADC and it increases with source impedance, input signal frequency and amplitude. It is important to keep the anti-aliasing resistor (R_{FLT}) much lower than the switch resistance. A resistance of 20 times lower than the switching resistor is preferred.

$$R_{FLT} < \frac{R_{SWITCH}}{20} \tag{14}$$

The minimum value for R_{FLT} is dependent on the output impedance of the amplifier based on stability considerations. If the output impedance of the driving amplifier is equal to R_O, its stability can be analyzed by evaluating the effect of R_{FLT} and C_{FLT} on the amplifier's open-loop response. The combination of R_O, R_{FLT} and C_{FLT} introduces one pole, f_P (equation 15) and one zero, f_Z (equation 16) in the amplifier's open-loop response, for which the corner frequencies are given below:

$$f_P = \frac{1}{2\pi(R_O + R_{FLT})C_{FLT}} \tag{15}$$

$$f_Z = \frac{1}{2\pi R_{FLT} C_{FLT}} \tag{16}$$

In order to ensure that the phase change from the zero negates the phase change that the pole initiates, it is important that the frequency distance between the pole and zero must be less than or equal to one decade.

$$\log\left(\frac{f_Z}{f_P}\right) \leq 1 \tag{17}$$

Using equations (15) and (16), the minimum value for RFLT can be derived as:

$$R_{FLT} \geq \frac{R_0}{9} \tag{18}$$

In the interest of stability, the effects of f_Z must occur at a frequency lower than the closed-loop gain bandwidth of the amplifier (f_{CL}). This is because for stability of the amplifier circuit, the closure rate between the open and closed loop gain curves should not be greater than 20db/decade. In order to account for the fabrication process variations associated with the amplifier's performance, a good practice is to choose f_Z such that closed-loop gain bandwidth of the amplifier, f_{CL} is at least twice the frequency of the zero.

$$\frac{f_{CL}}{f_Z} \geq 2 \tag{19}$$

For a fully differential amplifier combined with a fully differential SAR ADC the anti-aliasing filter is typically designed as a differential filter as shown in Figure 8.

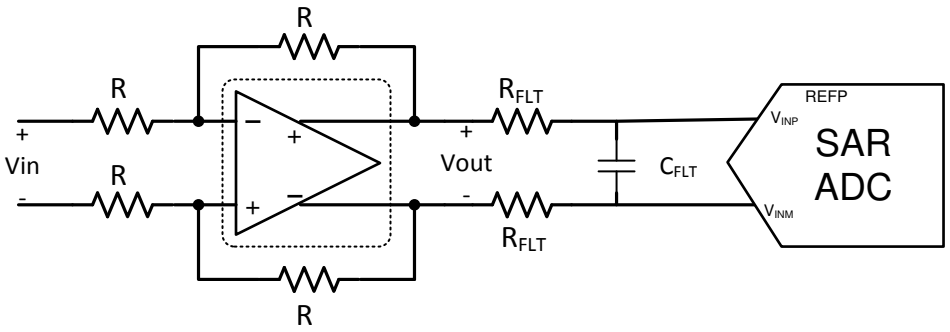

Figure 8: Fully Differential Anti-Aliasing Filter

The anti-aliasing filter bandwidth for a fully differential system can then be calculated using equation 20. It is important to note that for a fully differential filter the effective capacitance is twice for the RC Filter.

$$BW_{FLT} = \frac{1}{2\pi \times R_{FLT} \times (2 \times C_{FLT})} \tag{20}$$

2.4 System Noise Analysis

A high-performance 18-bit, 1MSPS SAR ADC has a typical SNR specification of 99dB for a 10 kHz input signal and V_{REF} = 5V. In order to maintain the superior dynamic performance of this ADC, the effect of noise from the front-end circuit has been analyzed in this section. This analysis will provide a bound for the maximum noise which the input driver circuit can have without degrading the system SNR. Based on the maximum noise and appropriate input amplifier and feedback resistors can be chosen for the design.

The input driver in an inverting configuration requires input and feedback resistors compared to the non-inverting configuration. This architectural choice has significant impact on the noise analysis. If we consider the circuit in Figure 9, which is an amplifier in an inverting configuration with two resistors, we can calculate the noise separately from each of the resistors and the op amp voltage noise. Each source has its own contribution to the noise at the amplifier output. Noise referred to the input (RTI) is simply the noise referred to the output (RTO) divided by the noise gain of the amplifier. Only considering the voltage noise and not current noise the RTI Noise can be calculated as:

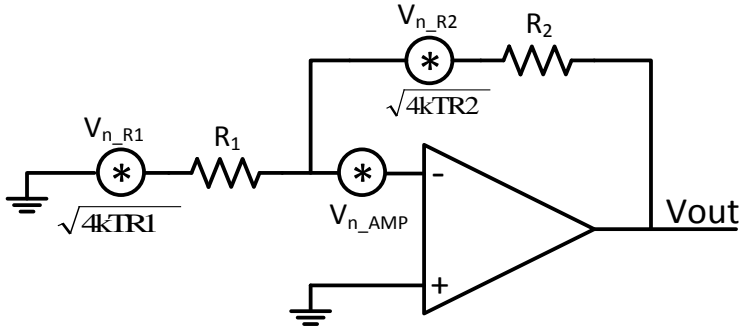

Figure 9: Noise Contribution in an Inverting Amplifier

$$NG = 1 + \frac{R_2}{R_1} \tag{21}$$

$$V_{n\_AMP\_RTI\_RMS} = \sqrt{1.57 \times BW_{FLT}} \times \sqrt{{V_{n\_AMP}}^2 + 4kTR_1\left[\frac{R_2}{R_1 + R_2}\right]^2 + 4kTR_2\left[\frac{R_1}{R_1 + R_2}\right]^2} \tag{22}$$

$$V_{n\_AMP\_RTO\_RMS} = NG \times V_{n\_AMP\_RTI\_RMS}$$

To calculate the RMS noise, the voltage noise density needs to be integrated over the anti-aliasing filter bandwidth. For an RC-filter, effective bandwidth is equal to $\frac{\pi}{2}$ (1.57) times the 3-dB cut-off frequency. It can be observed that the thermal noise of the resistor contributes significantly to RTO noise. In an inverting configuration the input amplifier is in a noise gain (NG) of 2. In this scenario the noise expressions in an inverting gain of -1 can be simplified as:

$$\begin{aligned} V_{n\_AMP\_RTI\_RMS} &= \sqrt{1.57 \times BW_{FLT}} \times \sqrt{{V_{n\_AMP}}^2 + 4kT\frac{R}{2}} \\ V_{n\_AMP\_RTO\_RMS} &= 2 \times \sqrt{1.57 \times BW_{FLT}} \times \sqrt{{V_{n\_AMP}}^2 + 4kT\frac{R}{2}} \end{aligned} \tag{23}$$

In comparison to the single ended amplifier the fully differential amplifiers have feedback resistors on each input as shown in Figure 10. The noise in a fully differential amplifier can be calculated as considering two single ended amplifiers configured in an inverting configuration as shown in Figure 10. Both the single ended amplifiers are identical and thus using law of superposition the noise of the fully differential amplifier is calculated in expression 24.

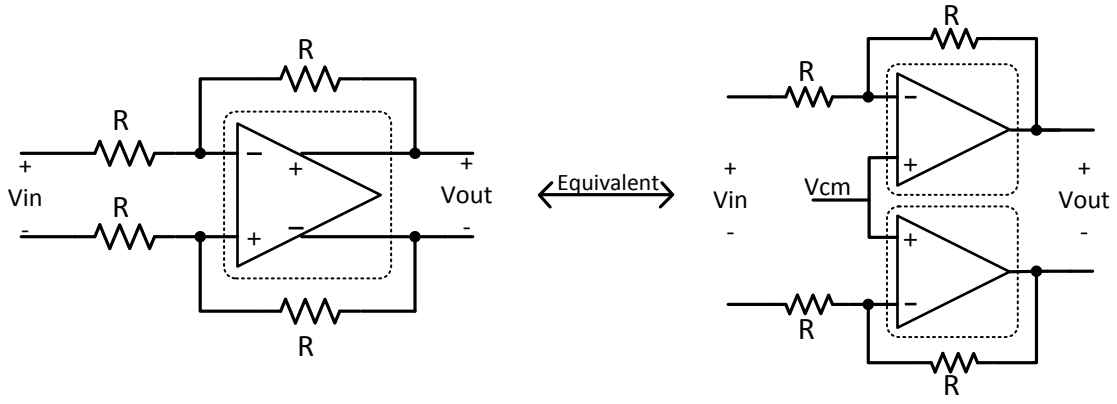

Figure 10: Fully Differential Amplifier Configuration

$$V_{n\_DIFF\_AMP\_RTO\_RMS} = \sqrt{\left(V_{n\_AMP\_RTO\_RMS}\right)^2 + \left(V_{n\_AMP\_RTO\_RMS}\right)^2}$$
$$V_{n\_DIFF\_AMP\_RTO\_RMS} = \sqrt{2} \times \left(V_{n\_AMP\_RTO\_RMS}\right) \quad (24)$$
$$V_{n\_DIFF\_AMP\_RTO\_RMS} = 2 \times \sqrt{1.57 \times BW_{FLT}} \times \sqrt{2 * V_{n\_AMP}{}^2 + 4kTR}$$

According to the expression in equation 24 above, it is important to choose low resistor values for the feedback of the amplifier for achieving low noise and high SNR from the amplifier. However, choosing a low resistor values will increase the system power and also require amplifiers with high output current drive. Thus it is important to make the appropriate choice to trade-off between system noise and power.

Now considering an ADC with an input dynamic range of V_{FSR}, the input referred noise can be calculated from the specified value of SNR in the datasheet by using equation below:

$$V_{n\_ADC\_RMS} = \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\frac{SNR(dB)}{20}} \quad (25)$$

Hence, the total noise contribution from the total data acquisition system can be calculated as:

$$V_{n\_TOT\_RMS} = \sqrt{V^2_{n\_DIFF\_AMP\_RTO\_RMS} + V^2_{n\_ADC\_RMS}} \quad (26)$$

To achieve a minimum SNR from the complete DAQ block (SNR_{SYS}), the maximum total rms noise from the DAQ block needs to meet the requirement in equation 27 (combining equation 2 and 26).

$$\sqrt{V^2_{n\_DIFF\_AMP\_RTO\_RMS} + V^2_{n\_ADC\_RMS}} < \frac{V_{FSR}}{2\sqrt{2} \times 10^{\frac{SNR_{SYS}}{20}}} \quad (27)$$

2.5 Reference Driver Design

External voltage reference circuits are used with ADCs without internal references. They provide low drift and very accurate voltages for ADC reference input. However, the output broadband noise of the references is of the order of few 100µVRMS, which degrades the noise and linearity performance of precision ADCs for which the typical noise is of the order of tens of µVRMS. Hence, in order to optimize the ADC performance, it is critical to appropriately filter and buffer the output of the voltage reference.

The basic circuit diagram for the reference driver circuit for precision ADCs is shown in Figure 11.

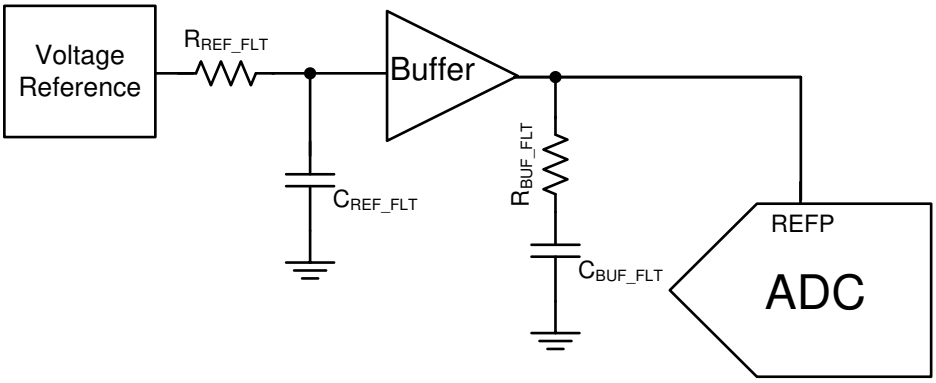

Figure 11: Simplified Schematic of Reference Driver Circuit

The reference noise can be categorized into peak-to-peak low frequency flicker or 1/f noise (V_{1/f_REF_pp}) from 0.1Hz to 10Hz and higher frequency broadband noise, generally specified as a noise spectral density ($e_{n\_REF\_RMS}$) over a wide frequency range. The broadband output noise from the reference circuit can be band-limited by the 3-dB cut-off frequency (f_{REF_3dB}) of an RC-filter at its output. So, the primary objective for the filter design is to keep the bandwidth low enough such that the integrated noise from the reference does not degrade the performance of the ADC. Hence, the total integrated noise from the reference ($V_{n\_REF\_RMS}$) should be kept at least 3 times less than the ADC noise to prevent any noise degradation in the system performance:

$$V_{n\_REF\_RMS} \leq \frac{V_{n\_ADC\_RMS}}{3} \tag{28}$$

The value of $V_{n\_REF\_RMS}$ can be calculated by the root sum square (rss) of the flicker noise and broadband noise density as shown below:

$$V_{n\_REF\_RMS} = \sqrt{\left(\frac{V_{1/f\_REF\_pp}}{6.6}\right)^2 + e_{n\_REF\_RMS}^2 \times \frac{\pi}{2} \times f_{REF\_3dB}} \tag{29}$$

Combining 28 and 29, we get:

$$\sqrt{\left(\frac{V_{1/f\_REF\_pp}}{6.6}\right)^2 + e_{n\_REF\_RMS}^2 \times \frac{\pi}{2} \times f_{REF\_3dB}} \leq \frac{1}{3} \times \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\frac{SNR(dB)}{20}} \tag{30}$$

The variation in the broadband noise density of the voltage reference ranges from 100 nV/√Hz to 1000 nV/√Hz depending on the reference type and power consumption. In general, the reference noise is inversely proportional to its quiescent current (I_{Q_REF}). Since broadband noise density is not always included in voltage reference datasheets, an approximation of the noise density for band-gap reference circuits is provided in equation 31:

$$e_{n\_REF\_RMS} \approx \frac{10000nV}{\sqrt{Hz}} \times \frac{1}{\sqrt{2 \times I_{Q\_REF}(\text{in } \mu A)}} \tag{31}$$

The above formula has been derived on the basis of the measured characteristic between the output noise density and quiescent current of several TI reference circuits, as shown in Figure 12.

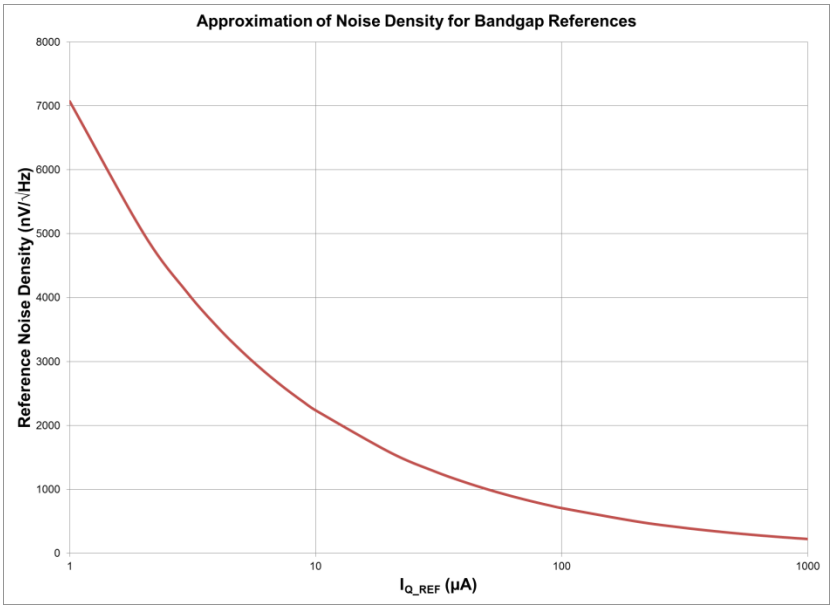

Figure 12: Characteristic Curve of Reference Noise vs. Current

On combining equations 29, 30, 31, the value of f_{REF_3dB} can be derived as:

$$f_{REF\_3dB} \leq \frac{2 \times I_{Q\_REF}(\mu A)}{\left(10000\ nV/\sqrt{Hz}\right)^2} \times \frac{2}{\pi} \times \left[\frac{1}{9} \times \frac{V_{FSR}^2}{8} \times 10^{-\frac{SNR(dB)}{10}} - \left(\frac{V_{1/f\_REF\_pp}}{6.6}\right)^2\right] \tag{32}$$

The value of the capacitor for the RC-filter should be kept higher than 100nF to keep its thermal noise lower than 0.2 μV_{RMS}. Using the selected value for C_{REF_FLT} and f_{REF_3dB}, the value of R_{REF_FLT} can be calculated using equation

$$R_{REF\_FLT} = \frac{1}{2\pi f_{REF\_3dB} \times C_{REF\_FLT}} \tag{33}$$

Once the noise of the reference block has been band-limited, the next important step is to ensure the reference can drive the dynamic load posed by the ADC reference input. The reference buffer must regulate the voltage such that ΔVREF stays within 1LSB error at the start of each conversion. This necessitates the use of a capacitor (C_{BUF_FLT}) along with a buffer to drive the ADC reference pin. The calculations to determine the size of C_{BUF_FLT} are given below

Difference in V_{REF} between conversions: $\Delta V_{REF} \leq \frac{V_{REF}}{2^N}$

If charge consumed during each conversion is QREF, then:

$$C_{BUF\_FLT} = \frac{Q_{REF}}{\Delta V_{REF}} \geq \frac{Q_{REF} \times 2^N}{V_{REF}} \tag{34}$$

The average value of Q_{REF} can be calculated from the maximum ADC conversion time (T_{CONV_MAX}) and the average value of reference input current (I_{REF}) specified in ADC datasheets as below:

$$Q_{REF} = I_{REF} \times T_{CONV\_MAX} \tag{35}$$

On combining equations 34 and 35, the minimum value of C_{BUF_FLT} can be obtained:

$$C_{BUF\_FLT} \geq \frac{I_{REF} \times T_{CONV\_MAX} \times 2^N}{V_{REF}} \tag{36}$$

The capacitor values derived from this equation are high enough to make the driving amplifier unstable, so it is recommended to use a series resistor, R_{BUF_FLT} to isolate the amplifier output and make it stable. The value of R_{BUF_FLT} is dependent on the output impedance of the driving amplifier as well as on the signal frequency. Typical values of R_{BUF_FLT} range between 0.1Ω to 2Ω and the exact value can be found by using SPICE simulations. It should be noted that higher values of R_{BUF_FLT} cause high voltage spikes at the reference pin which affects the conversion accuracy.

After designing the appropriate passive filter for band-limiting the noise of the reference circuit, it is important to select an appropriate amplifier for using as a reference buffer. The key specifications to be considered when selecting an appropriate amplifier for reference buffer are:

Output Impedance: The output impedance for a reference buffer should be kept as low as possible. This is because the ADC draws current from the reference pin during conversion and the resultant drop in reference voltage is directly proportional to the output impedance of the driving buffer. It also helps to keep the amplifier stable while driving a large capacitive load (C_{BUF_FLT}).

Input Offset: The input offset error of the buffer amplifier should be as low as possible to ensure that the reference voltage driving the ADC is very accurate.

Offset Drift: The offset temperature drift of the reference buffer should be extremely low to make sure that the reference voltage for the ADC does not change significantly over the operating temperature range. For similar reasons, it is also important to keep a low long-term time drift for the buffer amplifier.

3 Component Selection

3.1 ADC Selection

This TI design has been optimized for low distortion and noise using TI's high resolution, 18-bit 1MSPS SAR ADC, ADS8881 at its maximum sampling rate for a full-scale differential sine wave input at 10 kHz. The ADS8881 is a true differential SAR ADC designed for low voltage operation from 2.7 V–3.6 V AVDD and 1.65 V–3.6 V DVDD. The ADS8881 has excellent dynamic performance while consuming very low power. The power dissipation is 5.5mW (typical) at 1MSPS and can be further scaled down linearly for applications requiring low throughput.

3.2 Input Driver: Amplifier Selection

The primary goal for this design is to achieve a DAQ block with the lowest distortion and noise. The most important consideration for achieving this system specification is to select a full differential amplifier with low distortion (THD) for driving the inputs of the SAR ADC. This design is specified for a full scale sinusoidal signal, the op amp should support rail-to-rail output (RRO) swing. The other key specifications in order to meet the performance goals for this application are slew rate, output current drive, and low power.

The THS4521 is a very low power, fully differential op amp with rail-to-rail output and an input common mode range that includes the negative rail. The amplifier is designed for low-power data acquisition systems where power dissipation is a critical parameter. The amplifier provides exceptional ac performance that meets the very low distortion and high slew rate required from the input driver.

3.3 Input Driver: RC Filter Passive Component Selection

The critical passive components for this design are the resistors (R_{FLT}) and capacitor (C_{FLT}) for the RC-filter at the input of the ADC. The tolerance of the resistor was chosen to be 0.1%, but when this was not possible due to reasonable cost or availability, the tolerance was chosen to be 1%.

The design of the low distortion anti-aliasing filter is important to maintain the very low THD and noise requirement from the analog front end. The distortion due to the non-linear input impedance of the ADC increases with source impedance. It is therefore important to keep the anti-aliasing resistor (R_{FLT}) much lower than the switch resistance as explained in section 2.3. The switch resistance of the ADS8881 is 220Ω therefore the maximum R_{FLT} can be calculated below as

$$R_{FLT} < \frac{R_{SWITCH}}{20}$$
$$R_{FLT} < 11\Omega \quad (37)$$

The value for the resistor RFLT needs also to maintain the stability of the driving amplifier and is dependent on the output impedance of the driving amplifier, as explained in equation. The output impedance of THS4521 is dependent on the frequency of operation.

Using equation, the minimum value for resistance R_{FLT} can be calculated as:

$$R_{FLT} \geq \frac{80}{9} \approx 9\Omega \quad (38)$$

Therefore in this design the R_{FLT} is chosen to be **10Ω** to meet both the minimum and maximum requirements described above. Higher anti-aliasing resistor value can be chosen however this will results in additional distortion.

The input capacitance of ADS8881 is 59pF, therefore according to equation:

$$C_{FLT} \geq 20 \times C_{SH}$$
$$C_{FLT} \geq 1.18nF \quad (39)$$

In general it is beneficial to design a RC filter with bandwidth as low as possible to filter out amplifier noise. However, the practical limitation on the choosing large ceramic C0G capacitor due to cost imposes a maximum value on the capacitor value selection. In this design the selected value of capacitance for the differential input of the ADC is **10nF**. Based on the RC values, the bandwidth of the anti-aliasing filter can be calculated using equation 20 as:

Table 2: Bandwidth Calculation of the Anti-Aliasing Filter

R_{FLT}	10 Ω
C_{FLT}	10 nF
BW_{FLT}	800 kHz

This solution is designed to achieve the lowest distortion and noise while conserving power. Therefore the feedback resistors in the inverting gain of -1 configuration are chosen to be 1 kΩ. The choice of 1 kΩ resistor and the anti-alias filter bandwidth imposes a maximum amplifier noise requirement to meet the minimum system SNR (SNR_{SYS}) specification. The calculations on maximum amplifier noise based on theory described in Section 2.4 are highlighted using parameters defined in Table 3.

Table 3: Parameter for Amplifier Noise Calculation

Required SNR_{SYSTEM}	98 dB
V_{FSR}	4.315 V
ADC SNR	99 dB
BW_{FLT}	800 kHz
R	1000 Ω

$$V_{n\_TOT\_RMS} = \frac{V_{FSR}}{2\sqrt{2} \times 10^{\frac{SNR_{SYSTEM}}{20}}} = \frac{4.315}{2\sqrt{2} \times 10^{\frac{98}{20}}} = 38\mu V \quad (40)$$

$$V_{n\_ADC\_RMS} = \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\frac{SNR(dB)}{20}} = 34\mu V \quad (41)$$

Therefore to meet the required SNR for the system the maximum rms noise from the amplifier can be calculated using equation 26. The maximum voltage noise density of the amplifier can be calculated using equation 27.

$$V_{n\_DIFF\_AMP\_RTO\_RMS} < \sqrt{V^2_{n\_TOT\_RMS} - V^2_{n\_ADC\_RMS}} < 17\mu V \quad (42)$$

$$V_{n\_DIFF\_AMP\_RTO\_RMS} = 2 \times \sqrt{1.57 \times BW_{FLT}} \times \sqrt{2 * V_{n\_AMP}{}^2 + 4kTR} < 17\mu V$$
$$V_{n\_DIFF\_AMP\_RTO\_RMS} < 4.52 \frac{nV}{\sqrt{Hz}} \quad (43)$$

Based on the above calculation the amplifier voltage noise needs to have less than the 4.52 nV/√Hz. For a fully differential amplifier this requirement translates to a maximum voltage noise density of 6.4 nV/√Hz. This is because fully differential amplifier datasheets specify noise for a fully differential signal path. It is important to understand that to achieve ENOB of 16-bit the input driver needs to meet the minimum THD and noise specification. Thus the selected amplifier, THS4521 meets these minimum requirements based on the calculation above. Summary of key specification of the THS4521 are shown in Table 4.

Table 4: Key Parameters for the THS4521

Parameter	Datasheet Specification
THD @ 10kHz	-132 dBc
Fully Differential Voltage Noise Density	4.6 nV/√Hz
Iout	55 mA
Bandwidth	145 MHz
Iq	1.14 mA/ch

3.4 Reference Driver: Passive Components Selection

The external reference used to drive the ADS8881 in this design is the REF5045 from TI. This reference has been selected because it provides the highest possible reference voltage of 4.5V in a system with only a 5V supply. As mentioned in the datasheet of REF5045, it requires a capacitance of 10µF at the V_{OUT} pin for stability purposes. A series resistor of 0.2Ω is used with the 10µF capacitor for proper power-up of the reference.

As explained in Sec. 2.5, the noise from the reference should be bandwidth limited by designing a low-pass RC filter at the reference output. According to equation 31, the 3-dB bandwidth of this filter should be such that:

$$f_{REF\_3dB} \le \left[\frac{(V_{REF})^2}{\pi \times 2^{2N+2}} \times \frac{I_{Q\_REF}(\text{in } \mu A)}{10^{-10}\, V^2} \right] = \left[\frac{(4.5)^2}{\pi \times 2^{2\times 18+2}} \times \frac{1000}{10^{-10}} \right]$$
$$f_{REF\_3dB} \le 234.5\, KHz \quad (44)$$

The value of capacitor C_{REF_FLT} has been selected as 1 µF to keep the thermal noise of the capacitor at a low value. Hence, the value of R_{REF_FLT} can be calculated using equation 15 as:

$$R_{REF\_FLT} \ge \frac{1}{2\pi \times 234.5 \times 10^3 \times 10^{-9}} = 678.7\Omega \quad (45)$$

The value of R_{REF_FLT} has been selected as **1 kΩ** for this design.

The next important passive element in reference design is the capacitor C_{BUF_FLT}, which helps to regulate the voltage at the ADC reference pin under load conditions. According to ADS8881 datasheet, the average current drawn into the reference pin (I_{REF}) is equal to 200 µA and for a maximum throughput of 1MSPS, T_{CONV_MAX} is equal to 710ns. Hence, according to equation 35, the value of C_{BUF_FLT} can be calculated as:

$$C_{BUF\_FLT} \geq \frac{200 \times 10^{-6} \times 710 \times 10^{-9} \times 2^{18}}{4.5} = 8.27\mu F \quad (46)$$

The value of C_{BUF_FLT} has been selected as **10 µF** for this design.

3.5 Reference Driver: Amplifier Selection

As explained in Sec. 2.3, the key amplifier specifications to be considered to design a reference buffer for a high-precision ADC are **low offset, low drift, wide bandwidth and low output impedance**. While it is possible to pick an amplifier, which sufficiently meets all these requirements, it comes at a cost of excessive power consumption. For example, the OPA350 is a 38MHz bandwidth amplifier with a maximum offset of 0.5mV and low offset drift of 4µV/ºC, but it consumes a quiescent current of 5.2mA, which is extremely high for this design. This is due to the fact that from an amplifier design perspective, offset and drift are dc specifications while bandwidth, low output impedance and high capacitive drive capability are high frequency specifications. Thus, achieving all the performance in one amplifier requires power. However, a more efficient design to meet the low power budget is to use a composite reference buffer, which utilizes an amplifier with superior high frequency specifications in the feedback loop of a dc precision amplifier to get the overall performance at much lower power consumption.

In this design, the reference buffer is designed using two amplifiers – THS4281 and OPA333 in composite double feedback architecture as shown in Figure 13.

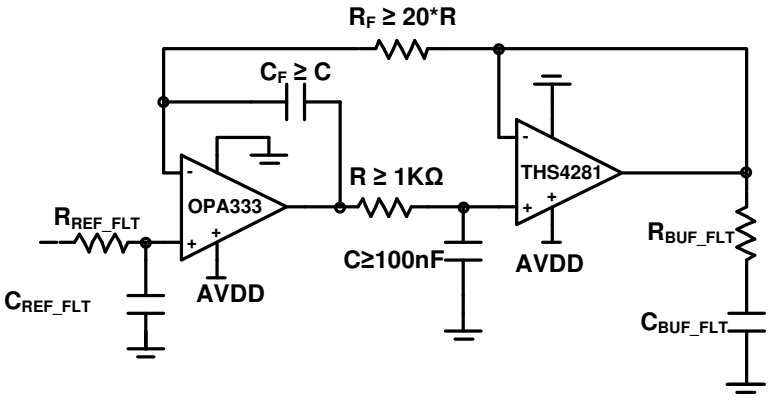

Figure 13: Schematic of Reference Buffer Circuit

The THS4281 has a wide 3-dB bandwidth of 90MHz at a gain of 1 and output impedance of 1Ω for 1MHz operation, with a maximum quiescent current of only 1mA. This makes it ideal for driving the high capacitor C_{BUF_FLT} and regulating the voltage at the ADC reference input. However, the THS4281 suffers from poor offset (2.5mV max.) and drift (7µV/ºC max.) specifications. In order to improve the DC specifications of the reference buffer, the OPA333 is used as a dc correcting amplifier. The OPA333 is a zero-drift (0.05µV/ºC max.) and low offset (10µV max.) amplifier with a maximum quiescent current of only 25µA. Thus, for similar performance related to reference accuracy and load-regulation, this two amplifier approach provides almost 5X power savings compared to a single amplifier buffer.

In this reference buffer design, the noise specifications of the dc amplifier (OPA333) are not very important because it gets heavily filtered by the low frequency RC-filter at its output. The value of C is chosen to be greater than 100nF to keep the capacitor thermal noise to be less than $0.2\mu V_{RMS}$ and the value of R is selected greater than 1 kΩ to avoid any stability issues due to high capacitive loading.

This amplifier uses a dual feedback in this design, out of which one feedback is active during dc operation and the other feedback is active during higher frequency ac operations. Figure 14 displays the dc model of the circuit where RF appears as a short and CF appears as an open. This feedback connects the output of THS4281 directly to the inputs of OPA333, which then corrects for its offset and drift. The value of RF should be at least 20 times greater than R to avoid any stability issues.

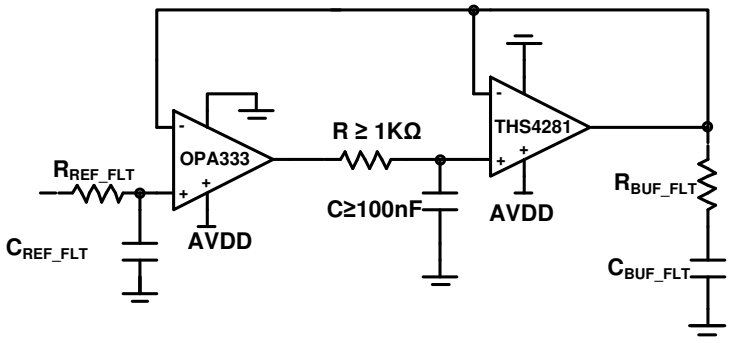

Figure 14: DC Equivalent Schematic of Reference Buffer

The active feedback connection during higher frequency operation is shown in Figure 15. At such frequencies of operation, RF acts as open connection; CF acts as a short and the two amplifiers are connected as isolated unity-gain buffers. The value of CF should be equal to or greater than C to avoid any stability issues.

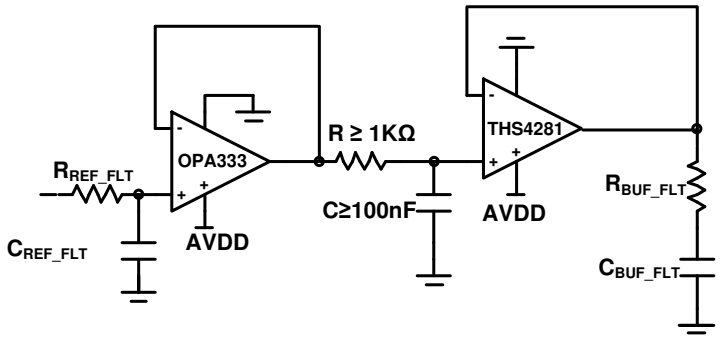

Figure 15: High Frequency Equivalent Schematic of Reference Buffer

4 Simulation

The TINA-TI™ schematic shown in Figure 16 shows the final design and selected components as explained in the previous sections.

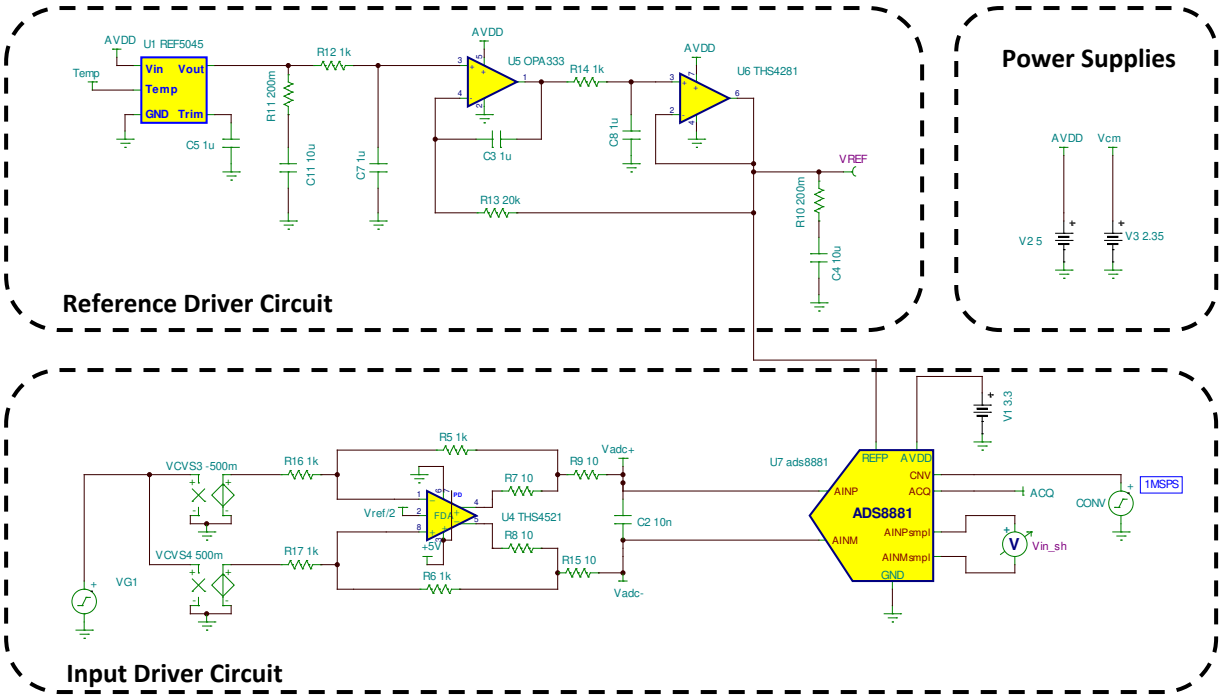

Figure 16: TINA-TI™ – Schematic Showing Complete Data Acquisition Block

The circuit in Figure 16 was simulated to perform a transient simulation using a 10 kHz sine wave signal to check that the ADC inputs are settling to sufficient accuracy before the start of every conversion. The same circuit is also used to simulate accurate settling of reference input voltage at the beginning of each conversion. The simulation details and results are provided in the subsequent sections.

4.1 Stability of Input Driver Amplifier

The TINA-TI™ schematic used to check the stability of the input drivers is shown in Figure 17.

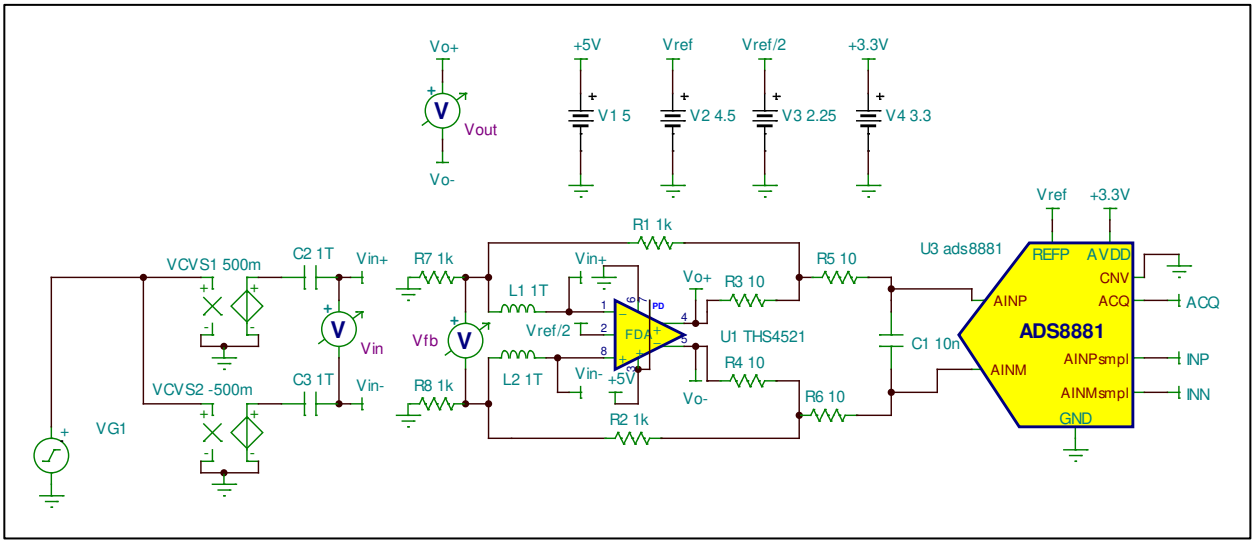

Figure 17: TINA-TI™ – Schematic for Checking Input Driver Stability

A large inductor of value 1 TH is connected in the feedback loop of the amplifier, so it behaves like an open-loop configuration at frequencies higher than dc. The circuit has been simplified by considering only half-circuit of the differential input structure [(2)]. In order to load the amplifier output appropriately, the ADC is connected with “CNV” pin tie to GND so that it is always sampling the input signal. The ac magnitude & phase response for this circuit is shown in Figure 18.

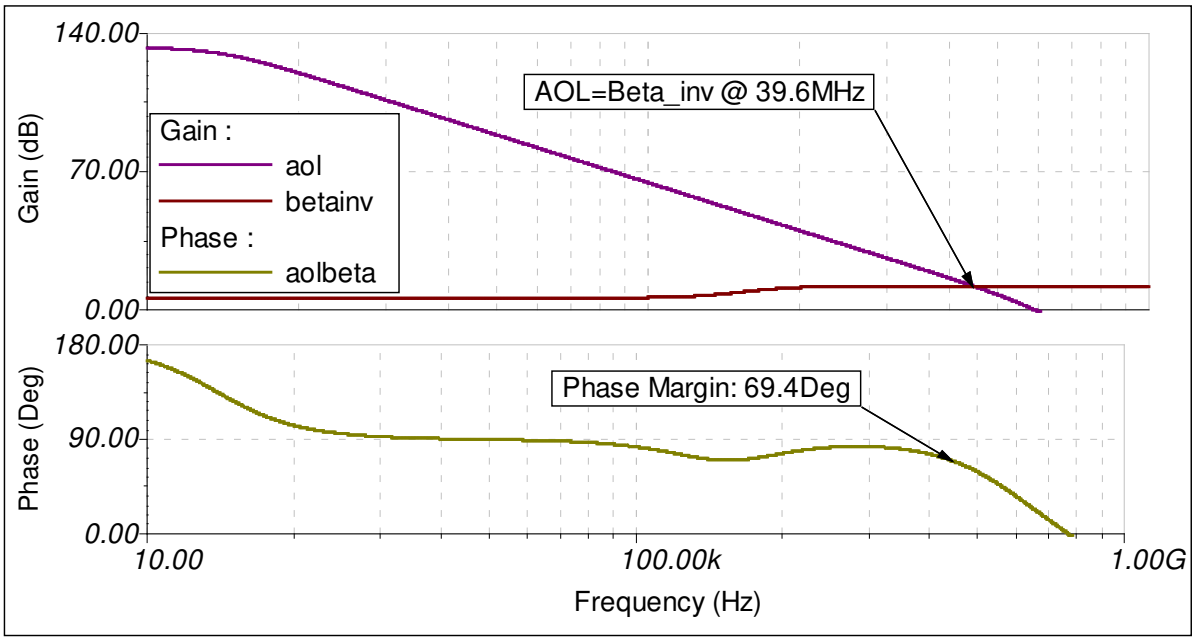

Figure 18: TINA-TI™ Schematic Result - AC Magnitude & Phase Plot for Input Drivers

The resulting phase margin of 69.4º at the 0-dB cross-over frequency of 39.6MHz validates the stability of the input drivers for this design.

4.2 Noise of Input Driver Amplifier

The TINA-TI™ schematic used to simulate the integrated rms noise of the input driver is shown in Figure 19. Ideally to calculate the RTO noise from the input driver, the voltage noise density curve needs to be integrated to infinity. For a realistic approximation of the referred to the output rms noise; integration to a decade beyond the bandwidth of the system is sufficient. Figure 20 shows the simulated integrated noise from the fully differential amplifier input driver referred to output is 13.45 µVRMS which meets the design requirements.

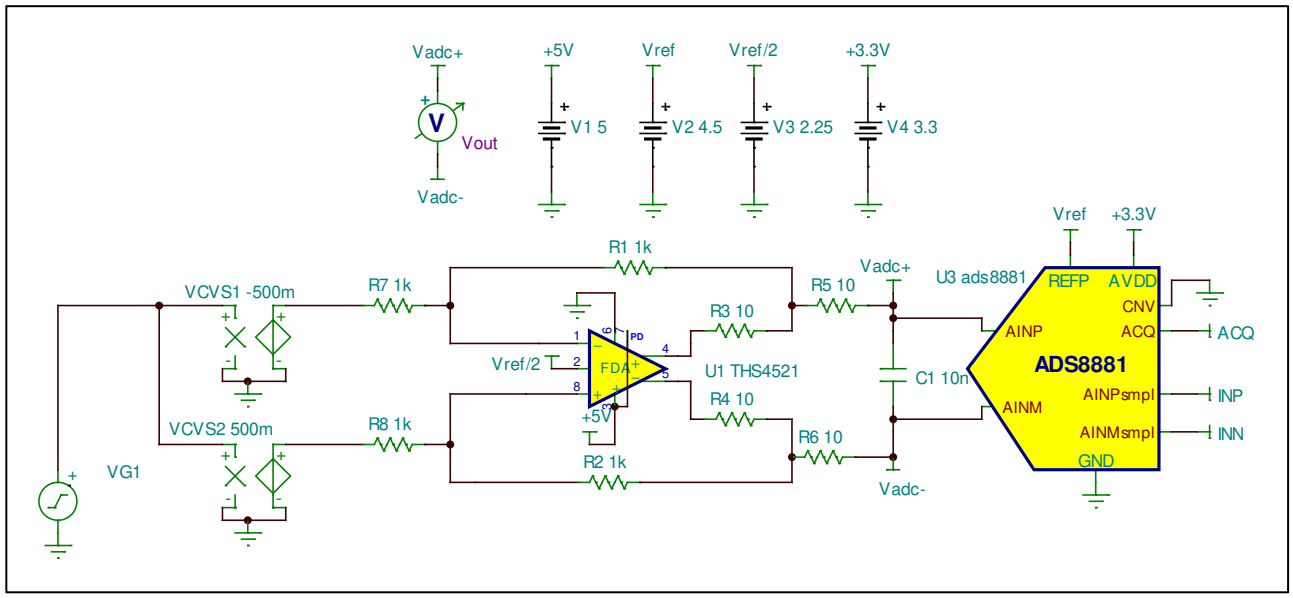

Figure 19: TINA-TI™ – Schematic for Checking Input Driver Noise

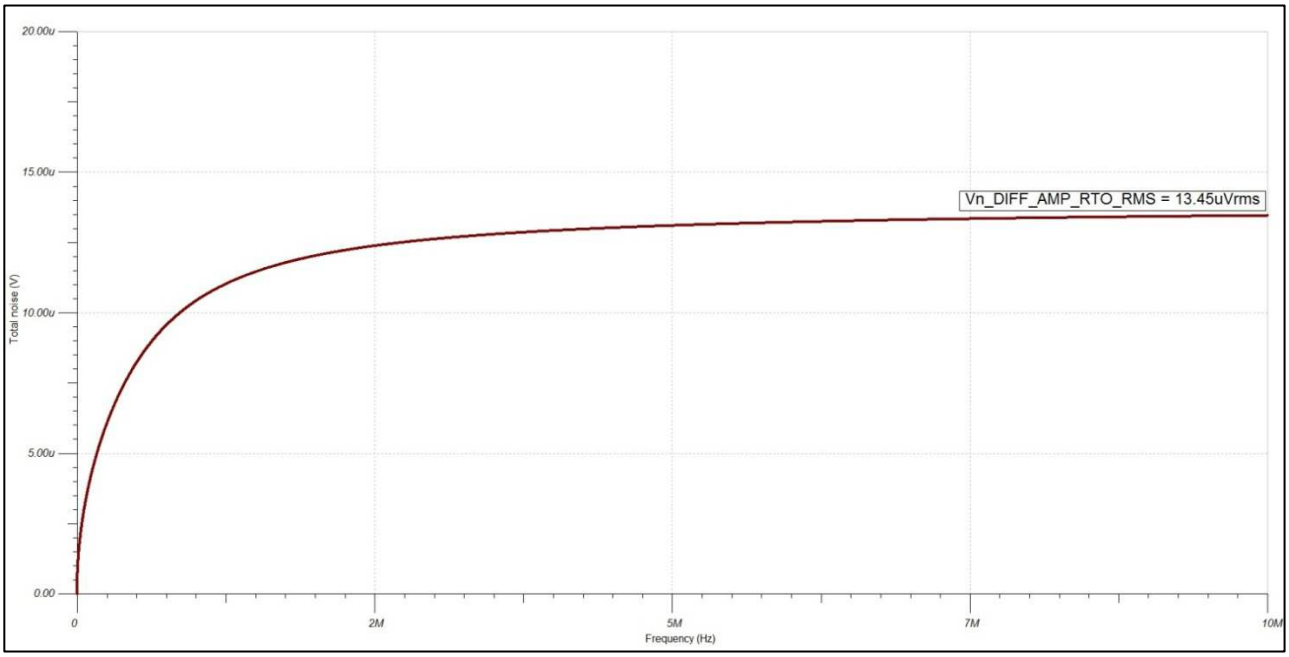

Figure 20: TINA-TI™ Schematic Result – Integrated Fully Differential Amplifier RMS Noise

4.3 Transient Simulation of ADC Input Circuit

The TINA-TI™ schematic shown in Figure 16 is used to check the accurate settling of the sine-wave signal at the inputs of the ADC during sampling phase. The simulated time-domain response for the circuit is shown in Figure 21. The transient plot on the top shows one cycle of a 10 kHz sine-wave with an amplitude of ±4.63V applied at the differential inputs of the ADS8881. The signal "Vin" represents the actual input signal at the differential inputs of the ADC and the signal "Vin_sh" shows the output of the ADC's input sample-and-hold circuit, as explained in Section 4. The lower plot shows the same waveform zoomed in on time scale for more details. The curves are collated together to show that the sampled signal accurately tracks the input signals during sampling and stays on hold when the ADC is converting.

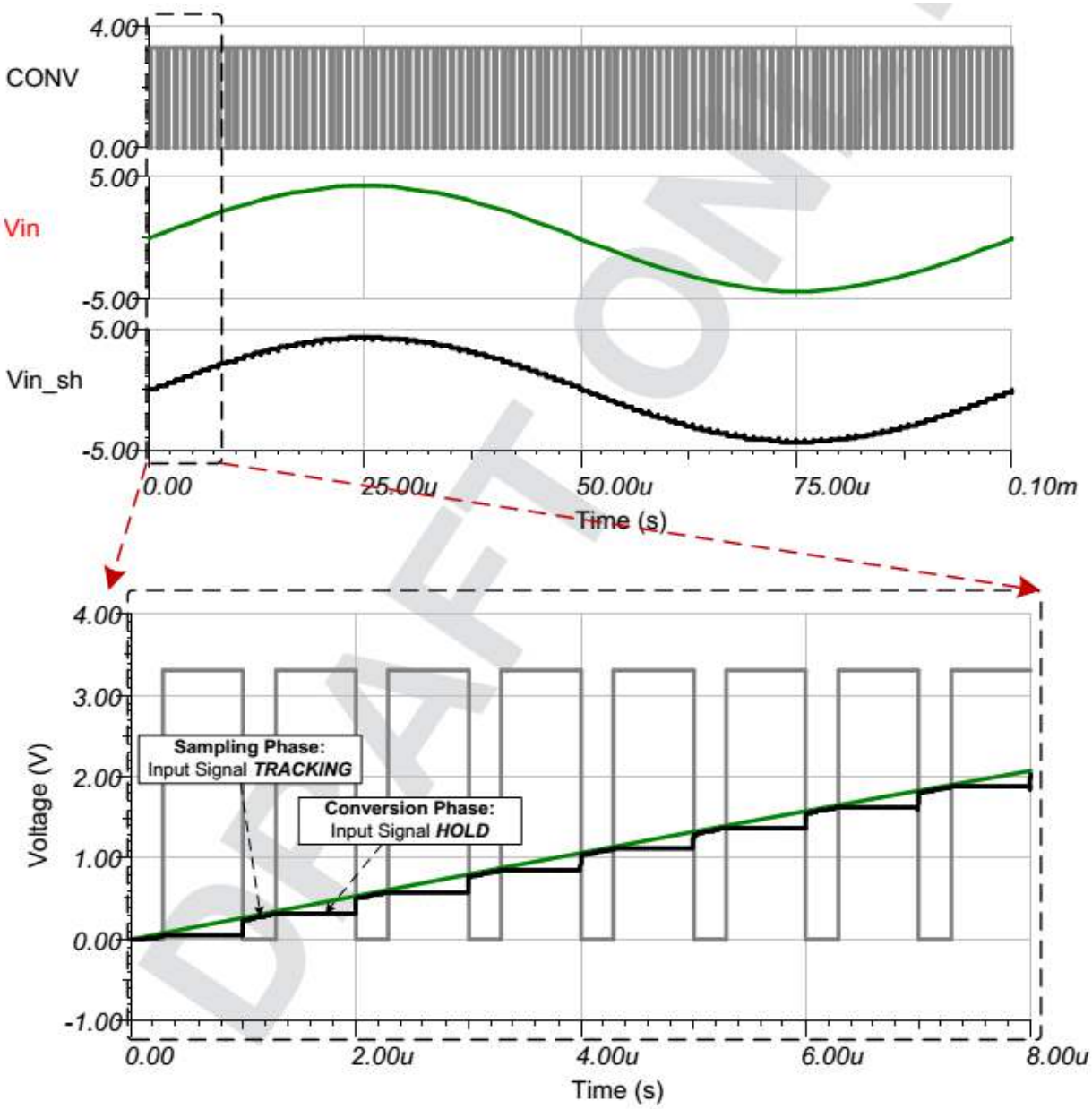

Figure 21: TINA-TI™ Schematic Result – Digitization of Input Sine-Wave Showing ADC Sample & Hold

4.4 Settling Response of ADC Reference Input

The TINA-TI™ schematic shown in Figure 16 is used to check the settling of the reference buffer output, driving the REFP pin of the ADS8881. As explained in Section 2.3, the voltage at the reference pin should settle to less than the LSB of the ADC for maintaining the overall system performance. The size of the LSB for the ADS8881 using VREF = 4.5V is equal to 34.3µV. According to the transient simulation plot shown in Figure 22, the error in the voltage at the REFP pin between two successive conversions is ΔVREF = 0.3µV, which is significantly less than the size of LSB. This validates that the reference voltage has settled to sufficient accuracy to maintain the performance of this design.

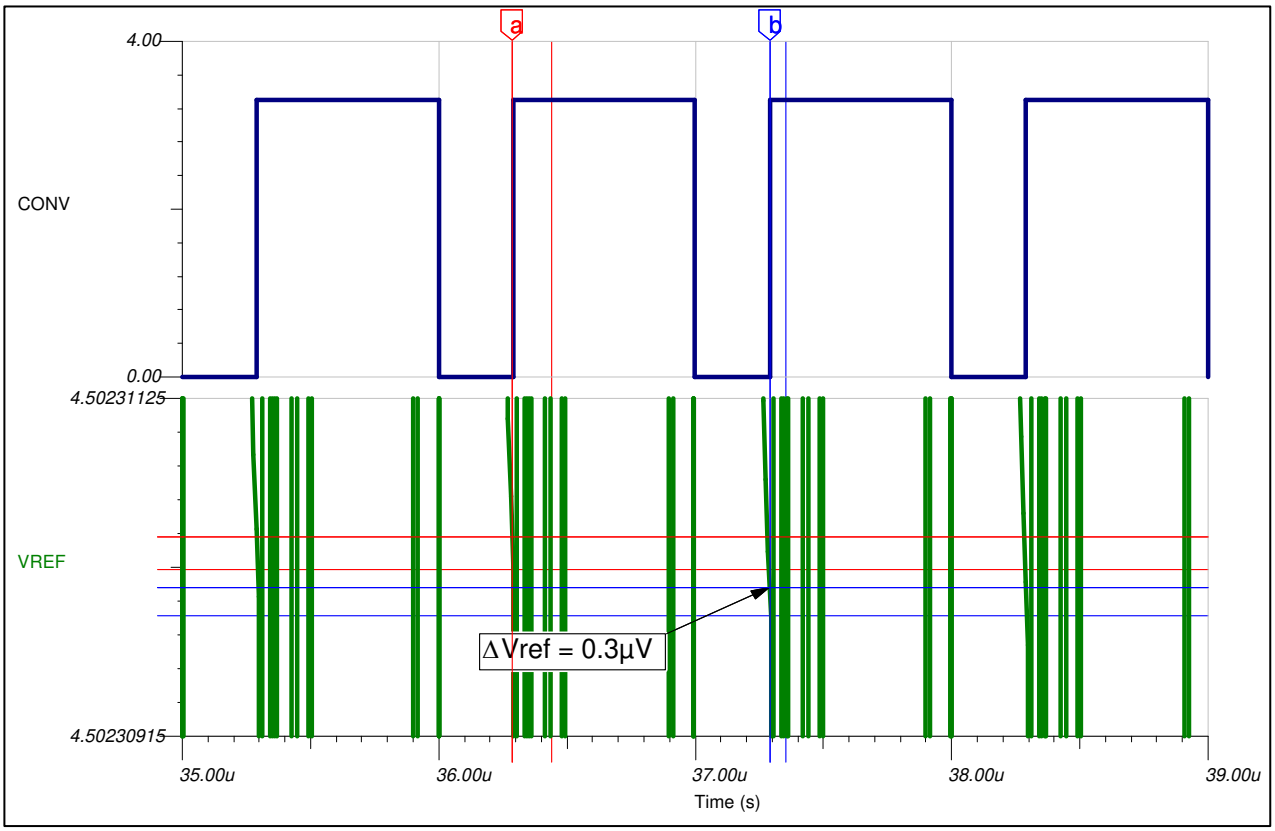

Figure 22: TINA-TI™ Schematic Result – ADC Reference Settling

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

The most important considerations in designing the PCB layout for this DAQ block are discussed below:

- The length of traces from the reference buffer circuit (REF5045, THS4281 and OPA333) to the REFP input pin of the ADC should be kept as small as possible to minimize the trace inductance that can lead to instability and potential issues with the accurate settling of the reference voltage
- The input driver circuit, comprised of THS4521 should be located as close as possible to the inputs of the ADC to minimize loop area, thus making the layout more robust against EMI/RFI rejection. Similarly, the resistors and capacitor of the anti-aliasing filter at the inputs of the ADC should be kept close together and close to the inputs of the ADC to minimize the loop area.
- The traces feeding the differential input voltage from the source up to the differential inputs of the ADC should be kept symmetrical without any sharp turns.

The complete PCB layout for this design is shown in Figure 23.

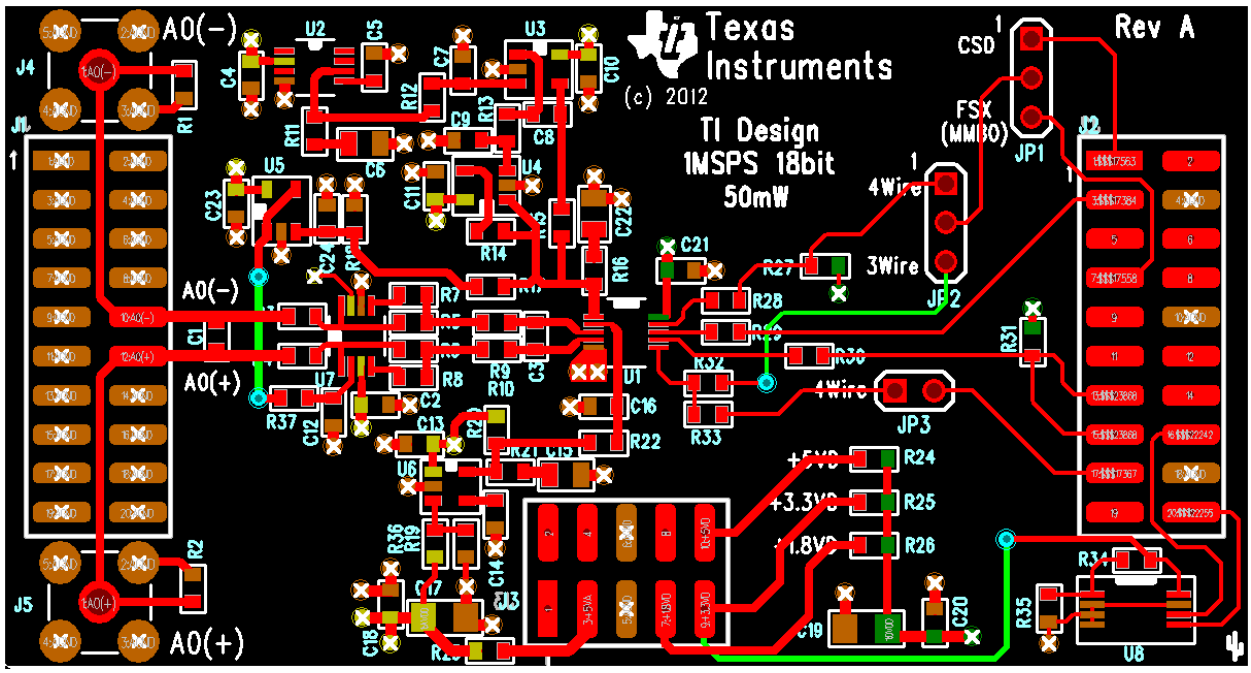

Figure 23: TI Design – 16-bit 50mW DAQ Block PCB Layout

6 Verification & Measured Performance

The measurement results for the verification of this design are listed in this section.

6.1 DC Noise Measurement

All ADC circuits suffer from some amount of inherent broadband noise contributed by the internal resistors, capacitors and other circuitry, which is referred to the inputs of the ADC. The front end driver circuit also contributes some noise to the system, which can also be referred to the ADC inputs. The cumulative noise, often called as the *input-referred noise* of the ADC has significant impact on the overall system performance. The most common way to characterize this noise is by using a constant dc voltage as the input signal and collecting a large number of ADC output codes. A histogram can then be plotted to show the distribution of output codes, which can be used to illustrate the impact of noise on the overall system performance. In this design, the dc noise for the system is measured by shorting the inputs of both input driving amplifiers to a common mode voltage, V_{cm} = ½ x V_{REF} = 2.25V, such that the differential voltage at the inputs of the ADC is equal to V_{DIFF} = 0V. The resulting histogram of output codes is shown in Figure 24.

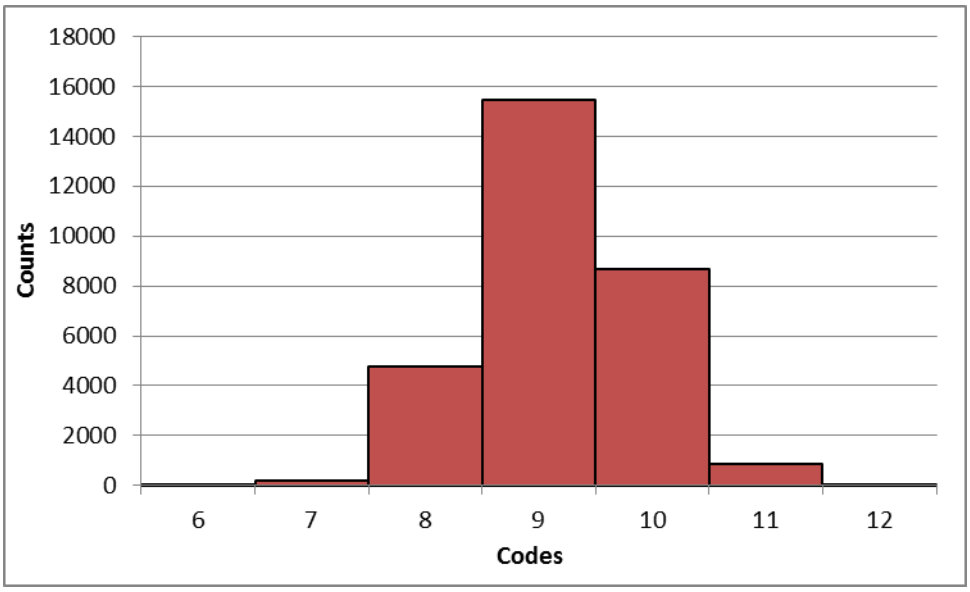

Figure 24: Measurement Data – Histogram Showing DC Noise (Mid-Scale)

The distribution of output codes looks like a Gaussian distribution which indicates a properly designed system. However, if the output code distribution has large peaks and valleys which make it distinctly non-Gaussian, then it indicates significant DNL errors in the ADC or issues with the system design like insufficient power supply decoupling, improper ground connections and/or other poor PCB layout effects. For a theoretically perfect ADC system, the histogram of output codes will be a single vertical bar since the ADC output will always be the same for a dc input voltage. However, the noise contributions from the ADC and the front-end circuit lead to a distribution of output codes, which provides a measure of the overall system's dc noise. The measured values of peak-to-peak difference between the codes (N_{PP}) and the standard deviation of codes (N_{σ}) are listed in Table 5.

The ***Noise-Free Resolution*** of an ADC is defined as the number of steady output bits from the converter beyond which the system performance is dominated by noise and it is not possible to differentiate between individual code transitions. This is an extremely conservative measurement of the ADC's performance because the formula for noise-free resolution is derived from the peak-to-peak code noise, which is extremely dependent on the total number of samples.

A more reliable approach is to use the standard deviation of output codes (N_σ) in calculating the ***Effective Resolution*** of the ADC. Please note that the results shown in Table 5 do not assume a Gaussian based formula in calculating the standard deviation from the peak-to-peak value because the overall dc noise is comparable to the size of the LSB. For an 18-bit ADC used in this design, the measured value of Effective Resolution is also equal to 18 bits which indicates that there is no degradation in the converter's performance due to the effects of dc noise.

Please note that the Effective Resolution and Effective Number of Bits (ENOB) shown in Section 6.2 should not be confused with each other as they are two completely different entities. The ENOB for an ADC is measured with an ac sinusoidal input signal and includes the effects due to quantization noise and distortion terms, which have no impact on a dc measurement.

Table 5: Measurement Results for DC Noise

Parameter	Formula	Measured Value
Mean Output Code	NA	9.17
Peak-to-Peak Code Noise (N_{PP})	NA	7
Standard Deviation (N_σ)	NA	0.752
Noise-Free Resolution	$\log_2\left(\frac{2^{18}}{N_{PP}}\right)$	15.19
Effective Resolution	$\log_2\left(\frac{2^{18}}{N_\sigma}\right)$	18

6.2 ADC Dynamic Performance Measurement

The design explained in this document has been optimized to achieve maximum performance out of ADS8881 at 1MSPS throughput for a full-scale transient input signal. Table 6 displays the ac performance of the data acquisition block. The measurements have been performed using a 10 kHz sinusoidal input signal. Figure 25 shows the FFT of the data acquisition block. The datasheet specifications are done for V_{REF} = 5V, but these measurements results indicate the ADC performance for V_{REF} = 4.5V, which implies that the measured values are approximately 0.9dB less than the actual ADC performance for SNR, THD and SINAD. Despite this adjustment, the measured THD of -110.04 from the system is at par with the specified THD of ADS8881. The data acquisition system is therefore able to achieve an **ENOB of 16-bit** as calculated in Table 6.

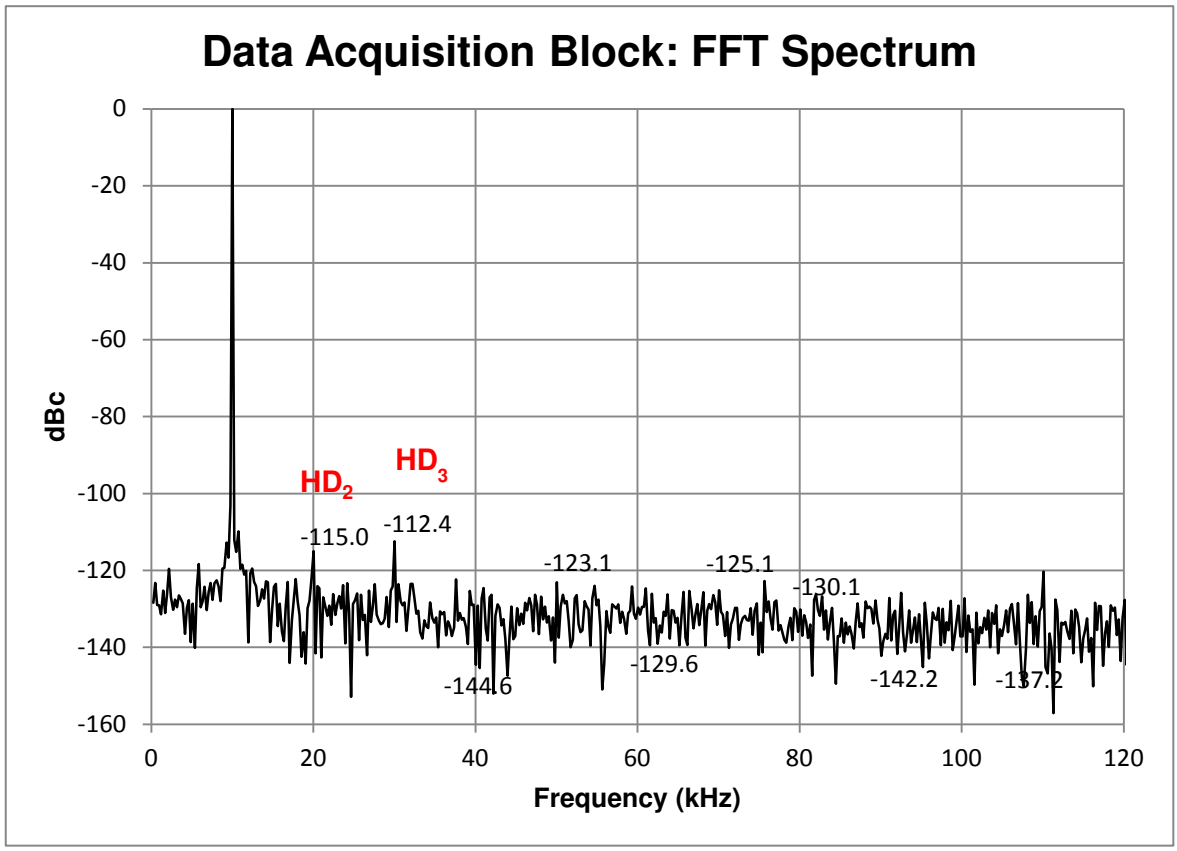

Figure 25: Measurement Result for FFT of the Data Acquisition Block

Table 6: Measurement Results for ADC AC Performance

Parameter	Specification (V_{REF} = 5V)	Measurement (V_{REF} = 4.5V)
Signal-to-Noise Ratio - SNR (dB)	99 dB	**98.73 dB**
Total Harmonic Distortion – THD (dB)	-110 dB	**-110.04 dB**
Signal-to-Noise & Distortion – SINAD (dB)	98 dB	**98.4 dB**
Effective Number of Bits – ENOB	16	**16.05**

6.3 ADC Linearity Measurement

The linearity of the system was measured by sweeping the differential input voltage from -4.45V to 4.45V in 26 voltage steps and the integral non-linearity (INL) error is plotted after cancelling the offset and gain errors from the response. The 26-point INL plot is shown in Figure 26 . The DAQ block provides the **best linearity performance** of ±1.5 LSB as seen in the figure below. The amplifier used in the front end driver (THS4521) has low output impedance which results in extremely low distortion.

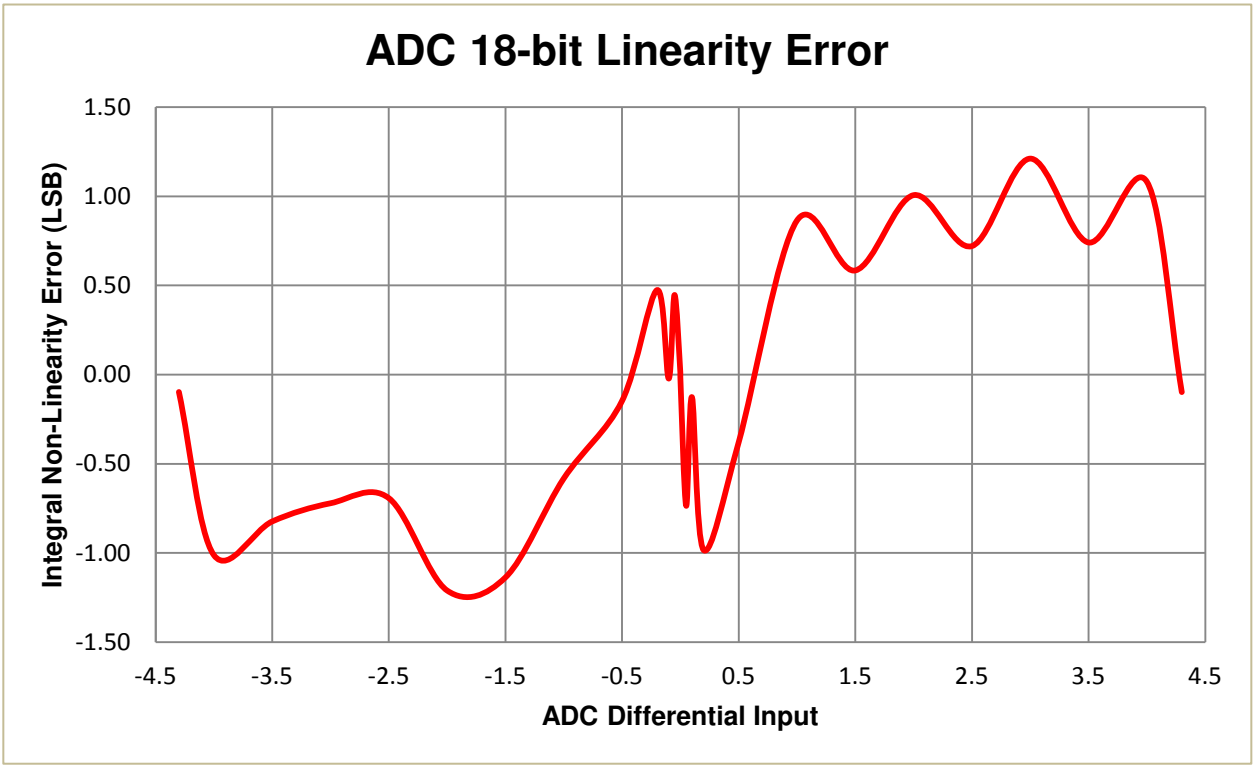

Figure 26: Measurement Data – ADC INL Plot (26 Points)

7 Modifications

The comparison in Table 7 shows some other low distortion and low noise RRO fully differential amplifiers from TI's portfolio which were considered for this design.

Table 7: Several alternative amplifiers compared with the THS4521

Op Amp	Quiescent Current (mA)	Noise Density @ 10kHz (nV/√Hz)	Total Harmonic Distortion (dB)	Bandwidth (MHz)
THS4521	1.14	4.6	-132	145
THS4531	0.25	10	-121	36
THS4031	7.9	1.6		100

The design principles described in this TI Precision Design can also be applied for applications that require higher throughput than 1 MSPS. An example application circuit using the ADS9110 is shown in Figure 27. The ADS9110 is an 18-bit, 2 MSPS SAR ADC with best-in-class ±0.5 LSB INL and 100dB SNR specifications under typical operating conditions. The input signal is processed through the OPA2625, a high-bandwidth, low-distortion, high-precision dual amplifier in an inverting gain configuration, and a low-pass RC filter before being fed into the ADC. Generally, the distortion from the input driver must be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the OPA2625 in an inverting gain configuration. The low-power OPA625 as an input driver provides exceptional ac performance because of its extremely low-distortion and high bandwidth specifications. In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal. The reference buffer is designed with the OPA625 and OPA378 in a composite architecture to achieve superior dc and ac performance at reduced power consumption, compared to using a single high-performance amplifier.

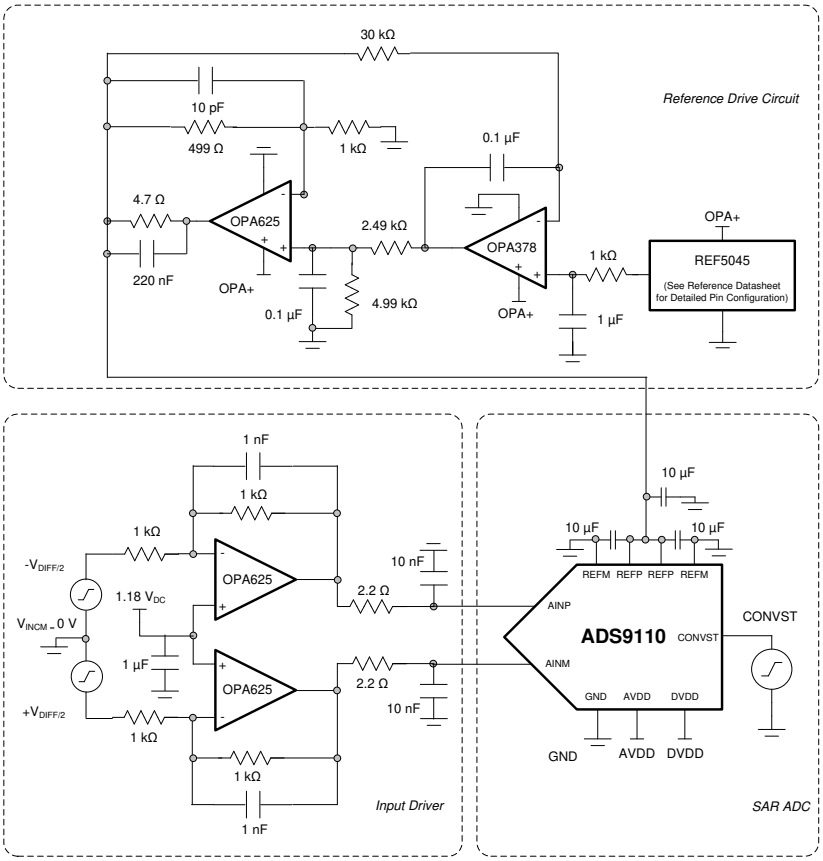

Figure 27: Differential Input DAQ Circuit for Lowest Distortion and Noise at 2 MSPS

The performance of this circuit is measured using a 2 kHz sinusoidal input signal. Figure 28 shows the FFT plot of the data acquisition block and the various performance specifications are mentioned in Table 8. The datasheet specifications are done for VREF = 5V, but these measurements results indicate the ADC performance for VREF = 4.5V, which implies that the measured values are approximately 0.9dB less than the actual ADC performance for SNR, THD and SINAD. Despite this adjustment, the measured THD of -120.2 from the system is better than the specified THD of ADS9110.

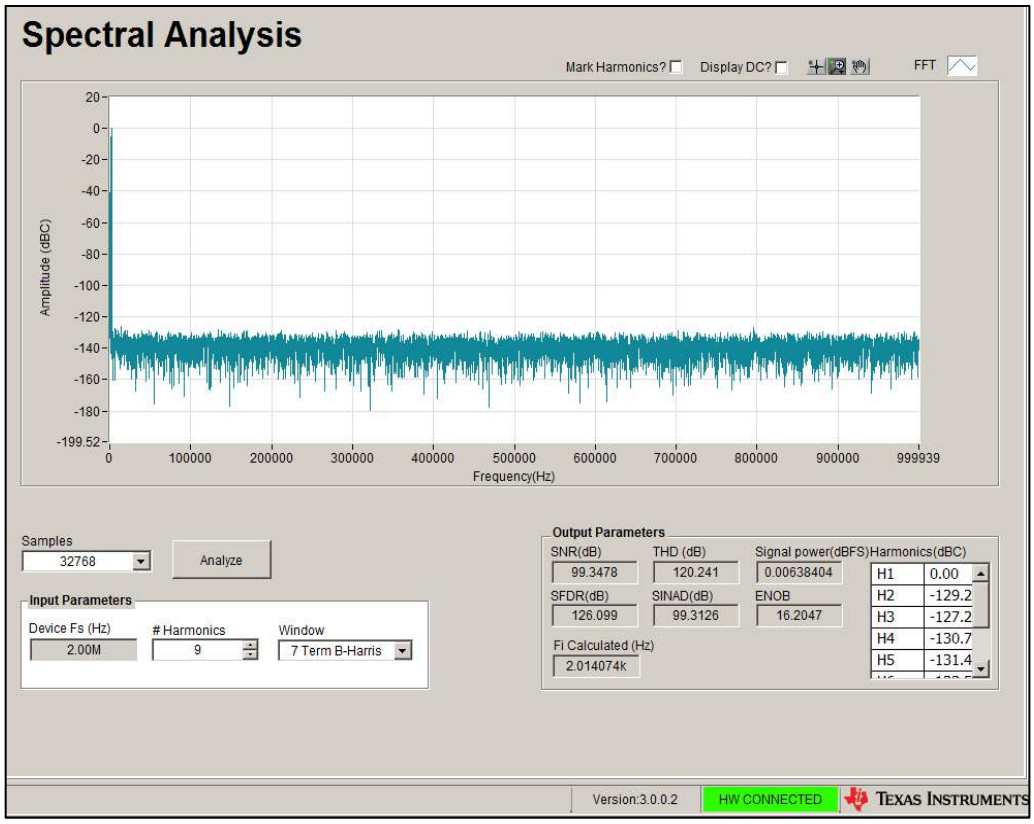

Figure 28: Measurement Result for FFT of the Data Acquisition Block

Table 8: Measurement Results for ADS9110 at 2 MSPS

Parameter	Specification (V_{REF} = 5V)	Measurement (V_{REF} = 4.5V)
Signal-to-Noise Ratio - SNR (dB)	100 dB	**99.3 dB**
Total Harmonic Distortion – THD (dB)	-118 dB	**-120.2 dB**
Signal-to-Noise & Distortion – SINAD (dB)	99.9 dB	**99.3 dB**

Appendix A. Appendix

A.1 Electrical Schematic

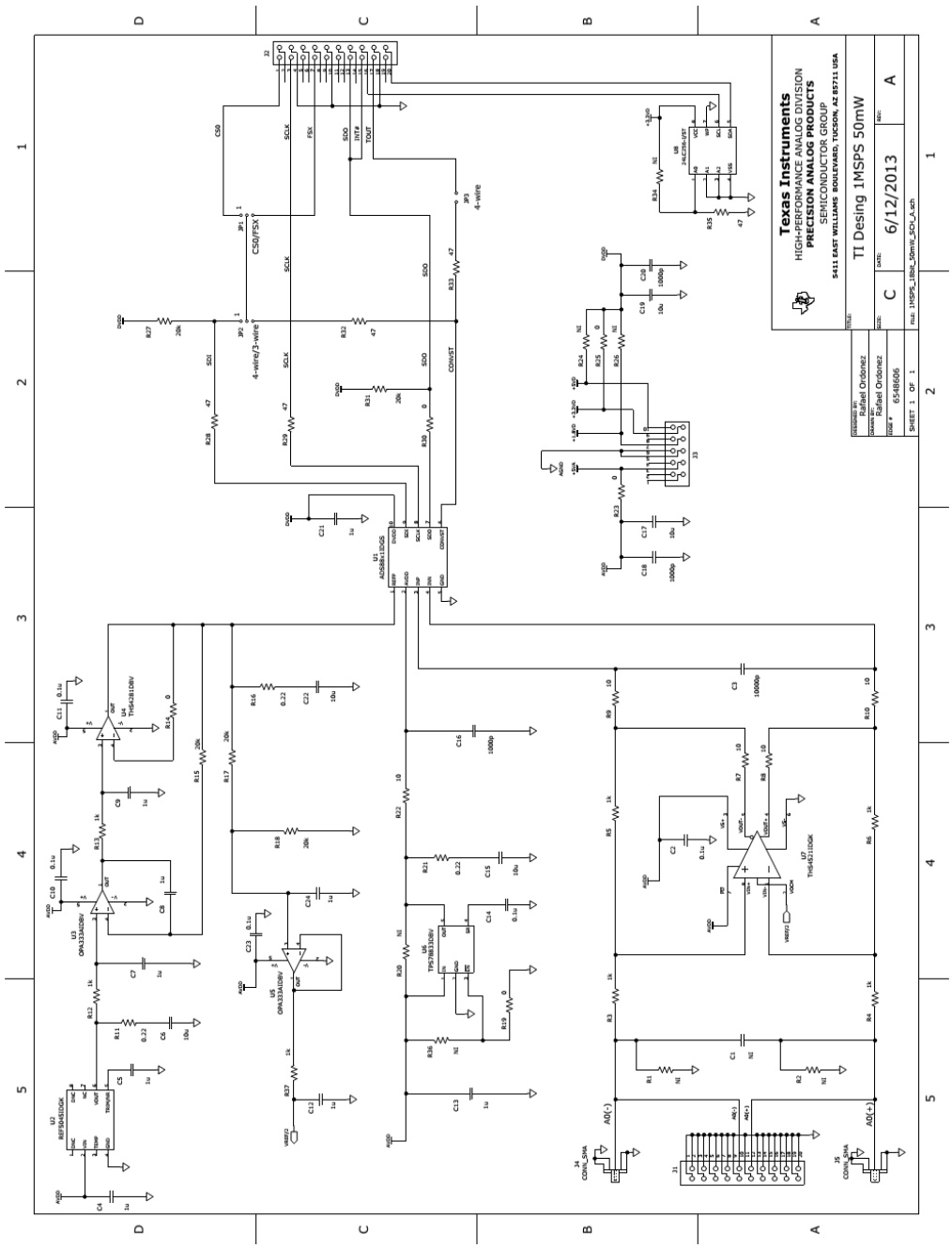

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Item	QTY	Value	Ref Des	Description	Manufacturer	Part Number
1	1		C1	Not Installed		
2	5	0.1u	C2, C10, C11, C14, C23	Capacitor, X7R Ceramic +/-10%, 25WV, 0603	Murata	GRM188R71E104KA01D
3	1	10000p	C3	Capacitor, NP0 Ceramic +/-5%, 50WV, 0603	TDK	C1608C0G1H103J
4	9	1u	C4, C5, C7, C8, C9, C12, C13, C21, C24	Capacitor, X7R Ceramic +/-10%, 25WV, 0603	Murata	GRM188R71E105KA12D
5	3	10u	C6, C15, C22	Capacitor, X7R Ceramic +/-10%, 10WV, 0805	Murata	GRM21BR71A106KE51L
6	3	1000p	C16, C18, C20	Capacitor, C0G Ceramic +/-5%, 50WV, 0603	Murata	GRM1885C1H102JA01D
7	2	10u	C17, C19	Capacitor, X7R Ceramic +/-10%, 16WV, 1206	TDK	C3216X7R1C106K
8	2		J1, J2 (Top)	Header 20 Pin SMT Plug, .100" Gold (2x10)	Samtec	TSM-110-01-L-DV-P
9	2		J1, J2 (Bottom)	Header 20 Pin SMT Socket, .100" Gold (2x10)	Samtec	SSW-110-22-F-D-VS-K
10	1		J3 (Top)	Header 10 Pin SMT Plug, .100" Gold (2x5)	Samtec	TSM-105-01-L-DV-P
11	1		J3 (Bottom)	Header 10 Pin SMT Socket, .100" Gold (2x5)	Samtec	SSW-105-22-F-D-VS-K
12	2		J4, J5	CONN SMA JACK STRAIGHT PCB	Amphenol	132134
					Emerson	142-0701-201
13	2		JP1, JP2	Header Strip, 3 pin .100" Gold (1x3)	Samtec	TSW-103-07-L-S
14	1		JP3	Header Strip, 2 pin .100" Gold (1x2)	Samtec	TSW-102-07-L-S
15	7		R1, R2, R20, R24, R26, R34, R36	Not Installed		
16	4	1k	R3, R4, R5, R6	Resistor, Thin Film Chip, 0.1%, 1/10W, 0603	Panasonic	ERA-3AEB102V
17	5	10	R7, R8, R9, R10, R22	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Vishay/Dale	CRCW060310R0FKEA
18	3	0.22	R11, R16, R21	Resistor, Thin Film Chip, 1%, 1/5W, 0603	Susumu	RL0816S-R22-F
19	3	1k	R12, R13, R37	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF1001V
20	5	0	R14, R19, R23, R25, R30	Resistor, Thick Film Chip, 1/10W, 0603	Panasonic	ERJ-3GEY0R00V
21	5	20k	R15, R17, R18, R27, R31	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF2002V
22	5	47	R28, R29, R32, R33, R35	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF47R0V
23	1		U1	IC ADC 16-bit 1MSPS Fully Diff 10-MSOP	TI	ADS8881IDGS
24	1		U2	IC VREF SERIES PREC 4.5V 8-MSOP	TI	REF5045IDGK
25	1		U3	IC OPAMP CHOP R-R 350KHZ SOT23-5	TI	OPA333AIDBV
26	1		U4	IC OPAMP VFB R-R 95MHZ SOT23-5	TI	THS4281DBV
27	1		U5	IC OPAMP GP R-R CMOS SOT23-5	TI	OPA330AIDBV
28	1		U6	IC REG LDO 3.3V .15A SOT-23-5	TI	TPS78833DBV
29	1		U7	IC OPAMP DIFF R-R 145MHZ 8MSOP	TI	THS4521IDGK
30	1		U8	IC EEPROM 256KBIT 400KHZ 8TSSOP	Microchip	24LC256-I/ST

Figure A-2: Bill of Materials

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