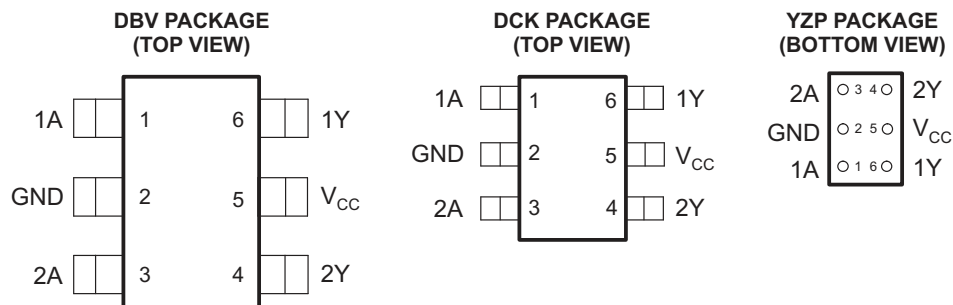


DUAL BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t_{pd} of 2.5 ns at 1.8 V
- Low Power Consumption, 10 μ A at 1.8 V
- \pm 8-mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This dual buffer/driver is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The output of the SN74AUC2G07 is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING ⁽²⁾ |
|-------------|--|--------------|-----------------------|---------------------------------|
| –40C to 85C | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | Reel of 3000 | SN74AUC2G07YZPR | __ _UV_ |
| | SOT (SOT-23) – DBV | Reel of 3000 | SN74AUC2G07DBVR | U07_ |
| | | Reel of 250 | SN74AUC2G07DBVT | |
| | SOT (SC-70) – DCK | Reel of 3000 | SN74AUC2G07DCKR | UV_ |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.



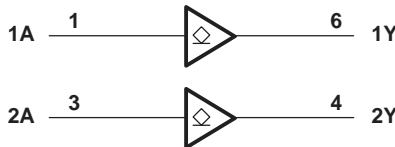
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

**FUNCTION TABLE
(EACH BUFFER/DRIVER)**

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | H |
| L | L |

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|--|---|-------------|----------------|---------|
| V_{CC} | Supply voltage range | -0.5 | 3.6 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 3.6 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 3.6 | V |
| V_O | Output voltage range ⁽²⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | | -50 mA |
| I_{OK} | Output clamp current | $V_O < 0$ | | -50 mA |
| I_O | Continuous output current | | | ±20 mA |
| Continuous current through V_{CC} or GND | | | | ±100 mA |
| θ_{JA} | Package thermal impedance ⁽³⁾ | DBV package | | 165 |
| | | DCK package | | 259 |
| | | YZP package | | 123 |
| T_{stg} | Storage temperature range | -65 | 150 | C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|--|---------------------|------|
| V_{CC} | Supply voltage | 0.8 | 2.7 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 0.8\text{ V}$ | V_{CC} | V |
| | | $V_{CC} = 1.1\text{ V to }1.95\text{ V}$ | $0.65 \cdot V_{CC}$ | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.7 | |
| V_{IL} | Low-level input voltage | $V_{CC} = 0.8\text{ V}$ | 0 | V |
| | | $V_{CC} = 1.1\text{ V to }1.95\text{ V}$ | $0.35 \cdot V_{CC}$ | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 0.7 | |
| V_I | Input voltage | 0 | 3.6 | V |
| V_O | Output voltage | 0 | 3.6 | V |
| I_{OL} | Low-level output current | $V_{CC} = 0.8\text{ V}$ | 0.7 | mA |
| | | $V_{CC} = 1.1\text{ V}$ | 3 | |
| | | $V_{CC} = 1.4\text{ V}$ | 5 | |
| | | $V_{CC} = 1.65\text{ V}$ | 8 | |
| | | $V_{CC} = 2.3\text{ V}$ | 9 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | ns/V |
| T_A | Operating free-air temperature | –40 | 85 | C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------|----------|----------------------------------|----------------|-----|--------------------|------|------|
| V_{OL} | | $I_{OL} = 100\ \mu\text{A}$ | 0.8 V to 2.7 V | | | 0.2 | V |
| | | $I_{OL} = 0.7\text{ mA}$ | 0.8 V | | 0.25 | | |
| | | $I_{OL} = 3\text{ mA}$ | 1.1 V | | | 0.3 | |
| | | $I_{OL} = 5\text{ mA}$ | 1.4 V | | | 0.4 | |
| | | $I_{OL} = 8\text{ mA}$ | 1.65 V | | | 0.45 | |
| | | $I_{OL} = 9\text{ mA}$ | 2.3 V | | | 0.6 | |
| I_I | A inputs | $V_I = V_{CC}$ or GND | 0 to 2.7 V | | | ±5 | μA |
| I_{off} | | V_I or $V_O = 2.7\text{ V}$ | 0 | | | ±10 | μA |
| I_{CC} | | $V_I = V_{CC}$ or GND, $I_O = 0$ | 0.8 V to 2.7 V | | | 10 | μA |
| C_i | | $V_I = V_{CC}$ or GND | 2.5 V | | 2.5 | | pF |

(1) All typical values are at $T_A = 25\text{C}$.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 0.8$ V | $V_{CC} = 1.2$ V ± 0.1 V | | $V_{CC} = 1.5$ V ± 0.1 V | | $V_{CC} = 1.8$ V ± 0.15 V | | | $V_{CC} = 2.5$ V ± 0.2 V | | UNIT |
|-----------|-----------------|----------------|------------------|---------------------------------|-----|---------------------------------|-----|----------------------------------|-----|-----|---------------------------------|-----|------|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | TYP | MAX | MIN | MAX | |
| t_{PLH} | A | Y | 4.3 | 1.2 | 3 | 1 | 2.2 | 1 | 1.8 | 2.5 | 0.9 | 1.6 | ns |
| t_{PHL} | | | 6.2 | 1 | 3.1 | 0.6 | 2.3 | 0.6 | 1 | 1.9 | 0.6 | 1.2 | |

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see [Figure 1](#))

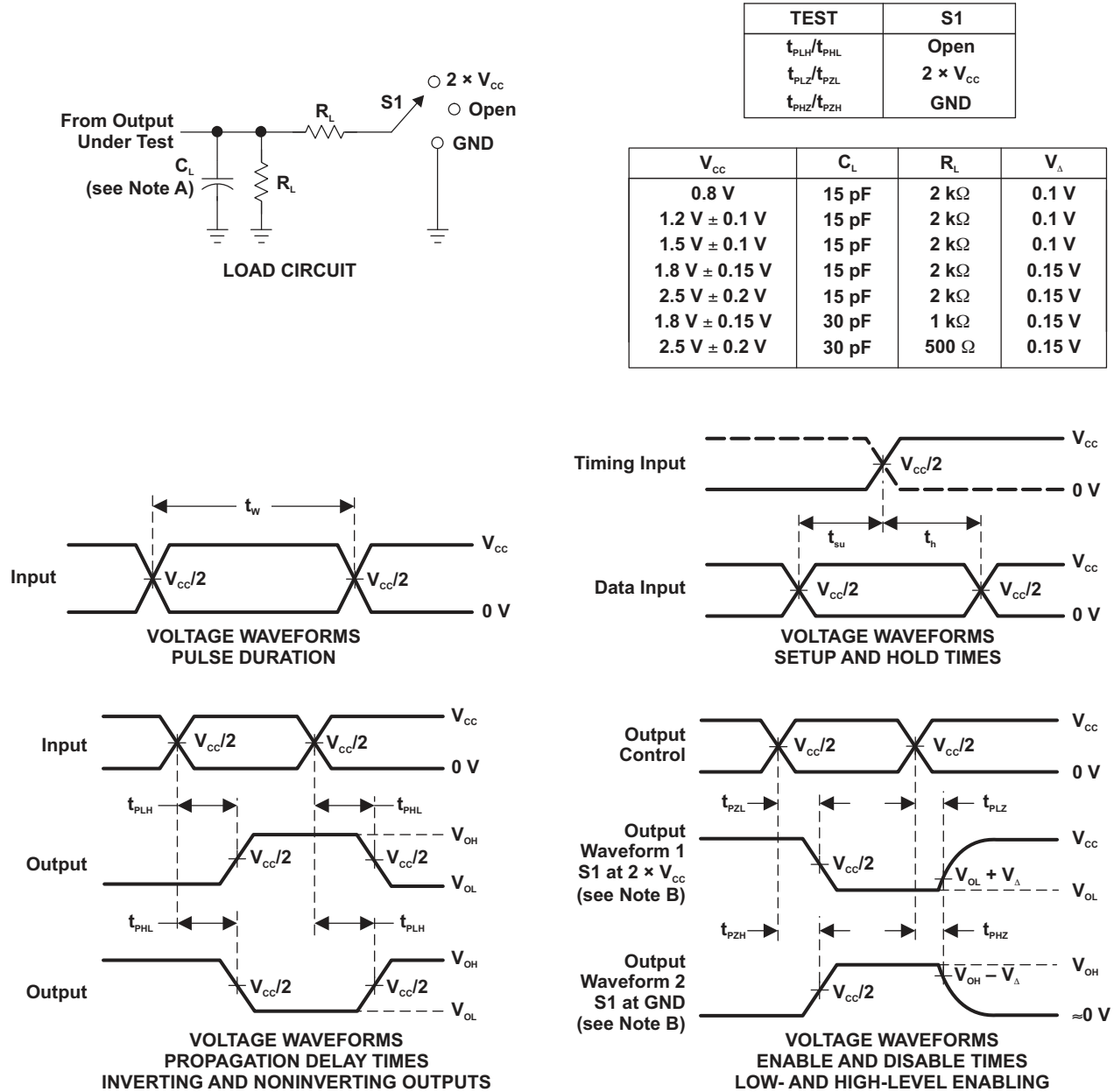
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 1.8$ V ± 0.15 V | | | $V_{CC} = 2.5$ V ± 0.2 V | | UNIT |
|-----------|-----------------|----------------|----------------------------------|-----|-----|---------------------------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| t_{PLH} | A | Y | 1 | 2 | 2.5 | 0.6 | 1.2 | ns |
| t_{PHL} | | | 0.9 | 1.5 | 2.3 | 0.8 | 1.8 | |

OPERATING CHARACTERISTICS

$T_A = 25$ C

| PARAMETER | TEST CONDITIONS | $V_{CC} = 0.8$ V | $V_{CC} = 1.2$ V | $V_{CC} = 1.5$ V | $V_{CC} = 1.8$ V | $V_{CC} = 2.5$ V | UNIT |
|--|--------------------|------------------|------------------|------------------|------------------|------------------|------|
| | | TYP | TYP | TYP | TYP | TYP | |
| C_{pd} Power dissipation capacitance | $f = 10$ MHz | 2.5 | 2.5 | 2.5 | 2.5 | 3.5 | pF |

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, slew rate ≥ 1 V/ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74AUC2G07DBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | (U075, U07F, U07R) | Samples |
| SN74AUC2G07DBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | U07R | Samples |
| SN74AUC2G07DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (UV5, UVF, UVR) | Samples |
| SN74AUC2G07DCKRG4 | ACTIVE | SC70 | DCK | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (UV5, UVF, UVR) | Samples |
| SN74AUC2G07YZPR | ACTIVE | DSBGA | YZP | 6 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | UVN | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AUC2G07DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUC2G07DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUC2G07DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74AUC2G07DBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUC2G07DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AUC2G07YZPR | DSBGA | YZP | 6 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

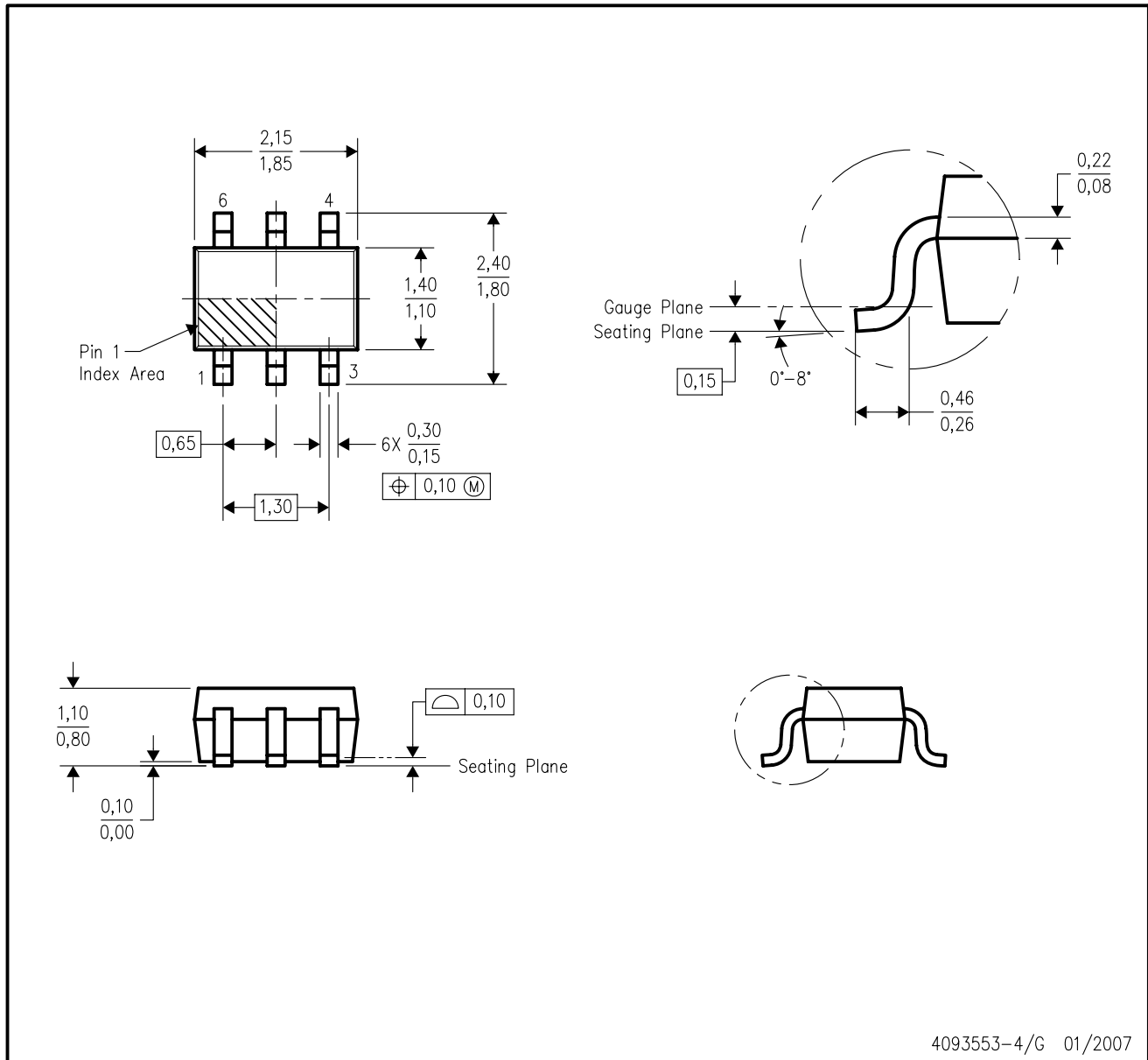
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AUC2G07DBVR | SOT-23 | DBV | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUC2G07DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUC2G07DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUC2G07DBVT | SOT-23 | DBV | 6 | 250 | 202.0 | 201.0 | 28.0 |
| SN74AUC2G07DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUC2G07YZPR | DSBGA | YZP | 6 | 3000 | 220.0 | 220.0 | 35.0 |

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

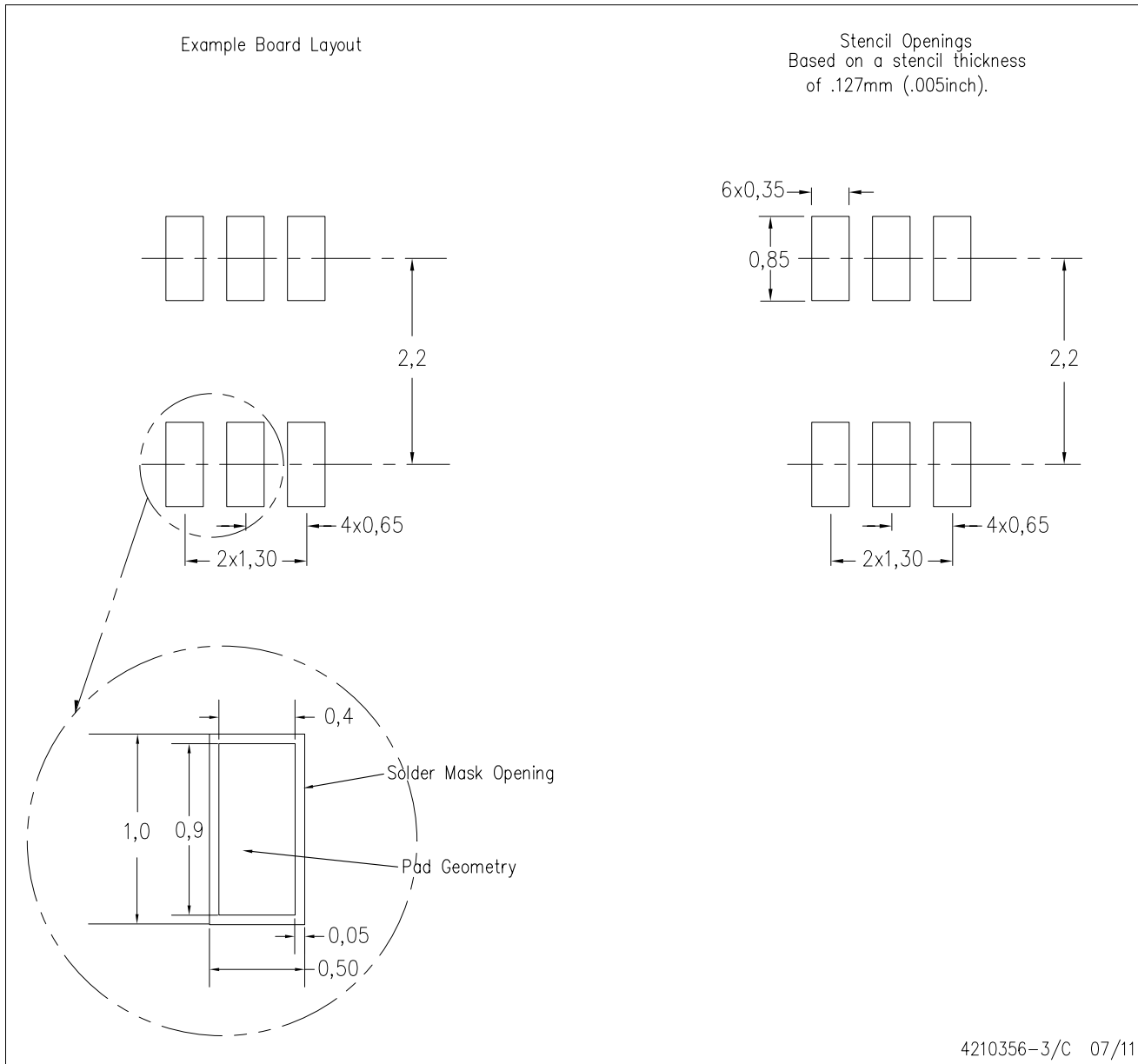


4093553-4/G 01/2007

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

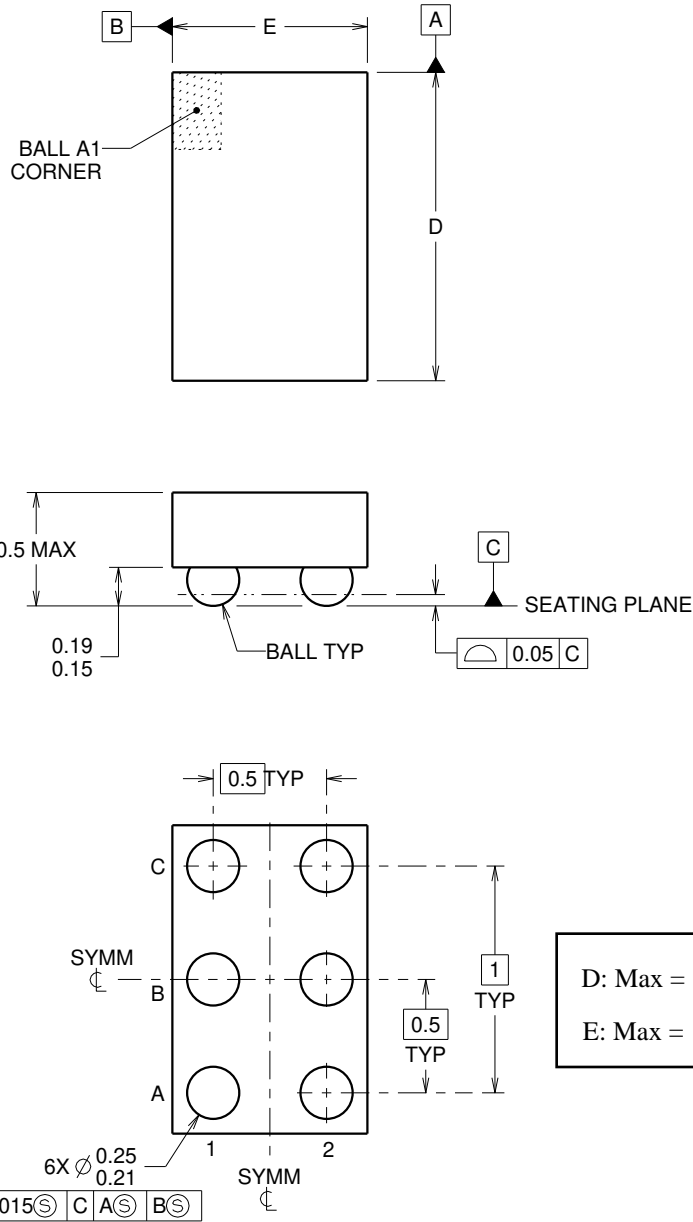
YZP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min = 1.357 mm
 E: Max = 0.918 mm, Min = 0.857 mm

4219524/A 06/2014

NOTES:

NanoFree Is a trademark of Texas Instruments.

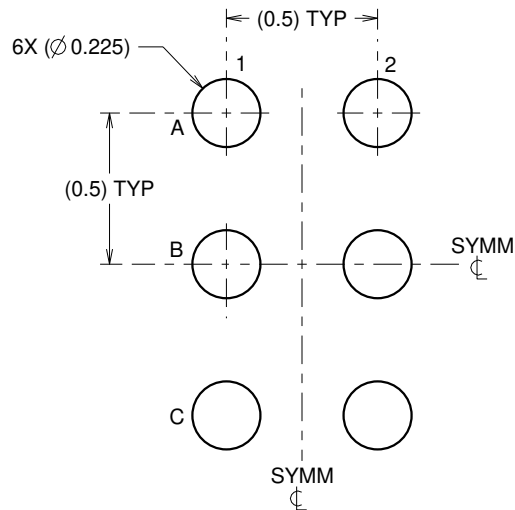
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

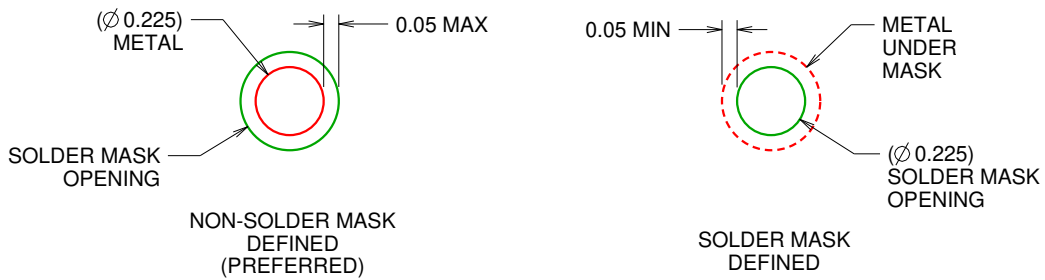
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

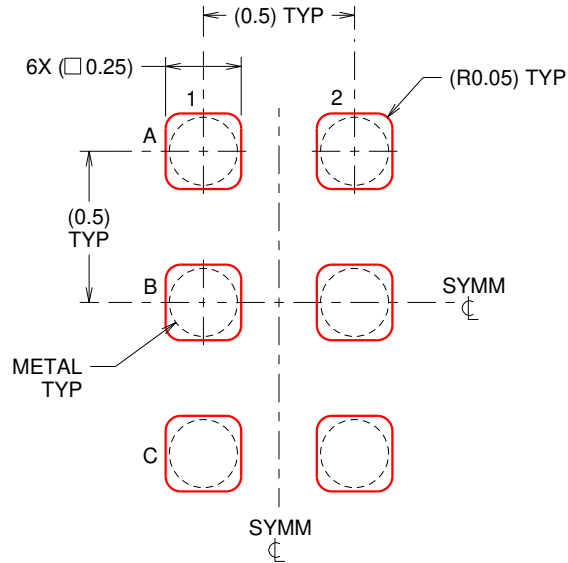
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

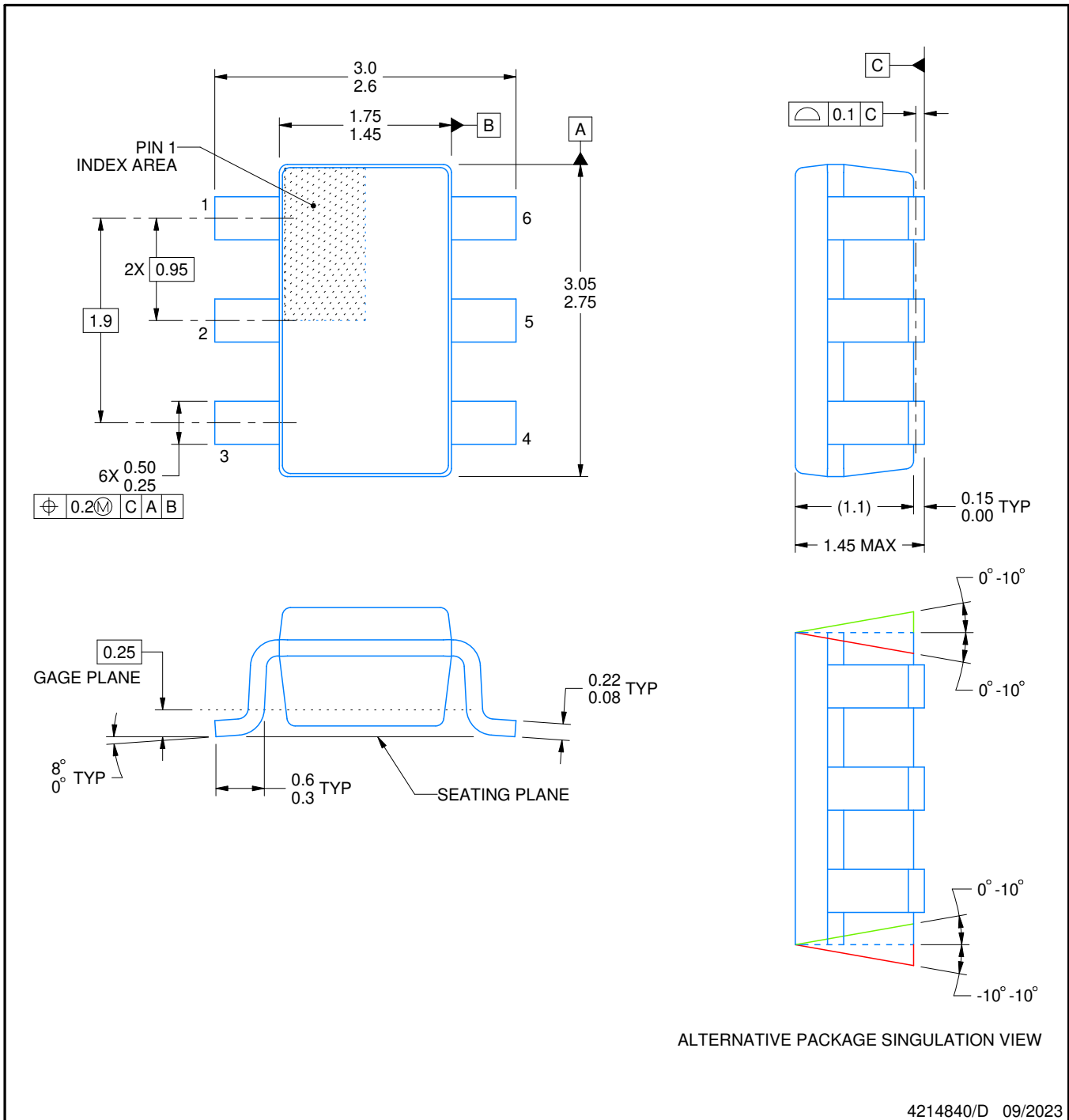
DBV0006A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

4214840/D 09/2023

NOTES:

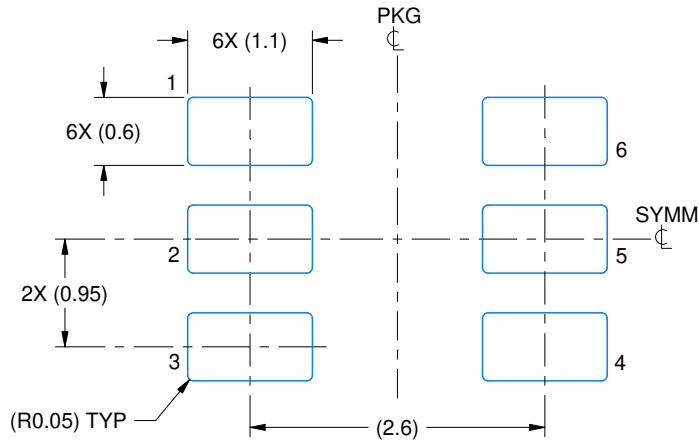
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

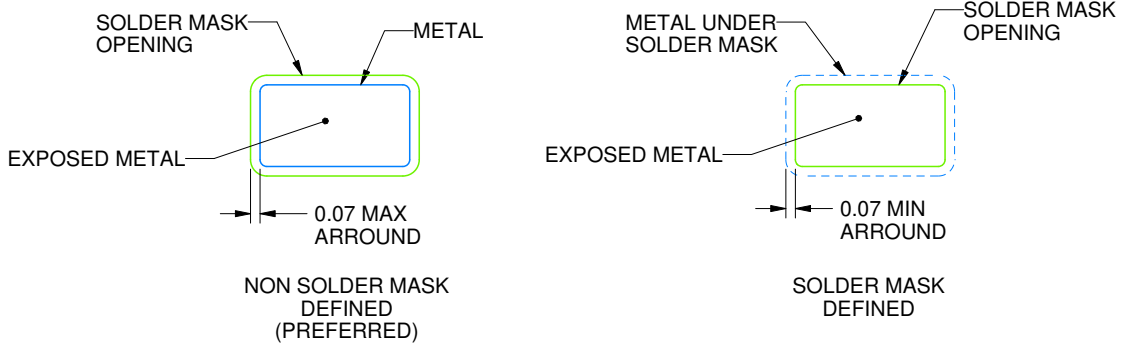
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/D 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

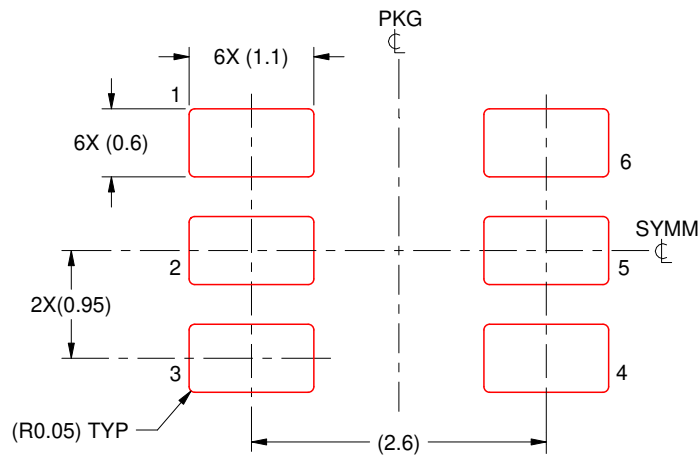
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/D 09/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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