

SN74CBT3384A 10-BIT FET BUS SWITCH

SCDS004L – NOVEMBER 1992 – REVISED JANUARY 2004

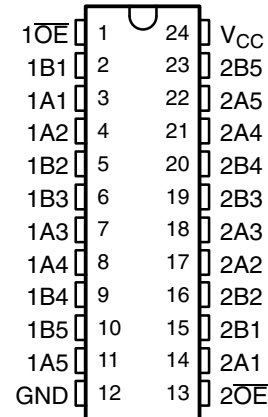
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

description/ordering information

The SN74CBT3384A provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as two 5-bit switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on, and port A is connected to port B. When \overline{OE} is high, the switch is open, and the high-impedance state exists between the two ports.

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-------------------|------------------|-----------------------|------------------|
| -40°C to 85°C | SOIC – DW | Tube | SN74CBT3384ADW | CBT3384A |
| | | Tape and reel | SN74CBT3384ADWR | |
| | SSOP – DB | Tape and reel | SN74CBT3384ADBR | CU384A |
| | SSOP (QSOP) – DBQ | Tape and reel | SN74CBT3384ADBQR | CBT3384A |
| | TSSOP – PW | Tube | SN74CBT3384APW | CU384A |
| | | Tape and reel | SN74CBT3384APWR | |
| TVSOP – DGV | Tape and reel | SN74CBT3384ADGVR | CU384A | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each 5-bit bus switch)

| INPUTS | | INPUTS/OUTPUTS | |
|--------|-----|----------------|---------|
| 1OE | 2OE | 1B1–1B5 | 2B1–2B5 |
| L | L | 1A1–1A5 | 2A1–2A5 |
| L | H | 1A1–1A5 | Z |
| H | L | Z | 2A1–2A5 |
| H | H | Z | Z |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

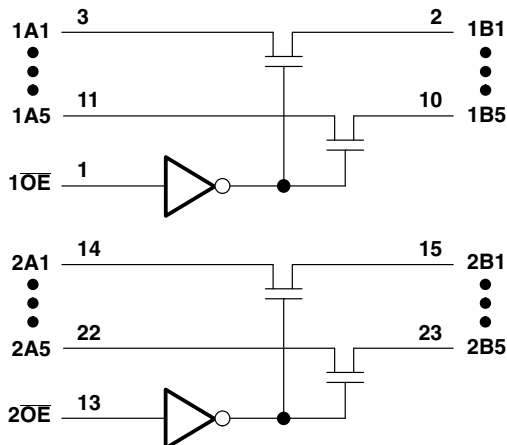
Copyright © 2004, Texas Instruments Incorporated

SN74CBT3384A

10-BIT FET BUS SWITCH

SCDS004L – NOVEMBER 1992 – REVISED JANUARY 2004

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|--|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Continuous channel current | 128 mA |
| Input clamp current, I_{IK} ($V_{I/O} < 0$) | -50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): | |
| DB package | 63°C/W |
| DBQ package | 61°C/W |
| DGV package | 86°C/W |
| DW package | 46°C/W |
| PW package | 88°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | MIN | MAX | UNIT |
|---|-----|-----|------|
| V_{CC} Supply voltage | 4 | 5.5 | V |
| V_{IH} High-level control input voltage | 2 | | V |
| V_{IL} Low-level control input voltage | | 0.8 | V |
| T_A Operating free-air temperature | -40 | 85 | °C |

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|--------------------------|----------------|---|---|----------------------|------|---------|---------------|
| V_{IK} | | $V_{CC} = 4.5\text{ V}$, | $I_I = -18\text{ mA}$ | | | -1.2 | V |
| I_I | | $V_{CC} = 5.5\text{ V}$, | $V_I = 5.5\text{ V or GND}$ | | | ± 1 | μA |
| I_{CC} | | $V_{CC} = 5.5\text{ V}$, | $I_O = 0$, $V_I = V_{CC}\text{ or GND}$ | | | 3 | μA |
| ΔI_{CC}^\ddagger | Control inputs | $V_{CC} = 5.5\text{ V}$, | One input at 3.4 V, Other inputs at V_{CC} or GND | | | 2.5 | mA |
| C_i | Control inputs | $V_I = 3\text{ V or 0}$ | | | | 4 | pF |
| $C_{io(OFF)}$ | | $V_O = 3\text{ V or 0}$, | $\overline{OE} = V_{CC}$ | | | 4.5 | pF |
| r_{on}^\S | | $V_{CC} = 4\text{ V}$, TYP at $V_{CC} = 4\text{ V}$ | $V_I = 2.4\text{ V}$, | $I_I = 15\text{ mA}$ | 14 | 20 | Ω |
| | | | $V_I = 0$ | $I_I = 64\text{ mA}$ | 5 | 7 | |
| | | $V_{CC} = 4.5\text{ V}$ | $V_I = 0$ | $I_I = 30\text{ mA}$ | 5 | 7 | |
| | | | $V_I = 2.4\text{ V}$, | $I_I = 15\text{ mA}$ | 10 | 15 | |

† All typical values are at $V_{CC} = 5\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

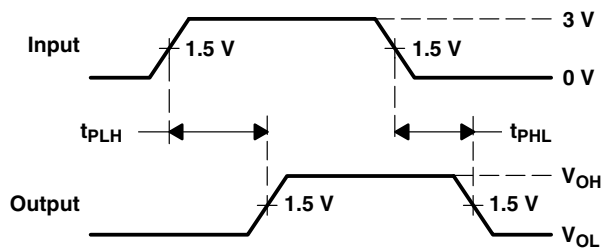
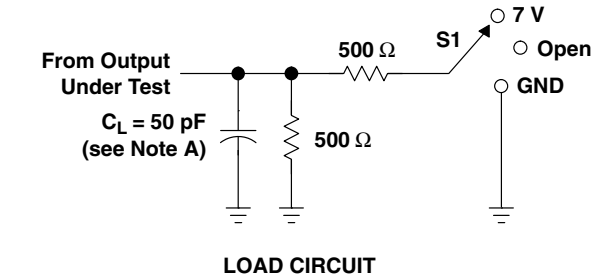
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4\text{ V}$ | | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | | UNIT |
|----------------------|-----------------|-------------|-----------------------|-----|--|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t_{pd}^{\parallel} | A or B | B or A | 0.35 | | 0.25 | | ns |
| t_{en} | \overline{OE} | A or B | 6.2 | | 1.9 | 5.7 | ns |
| t_{dis} | \overline{OE} | A or B | 5.5 | | 2.1 | 5.2 | ns |

^{||} The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

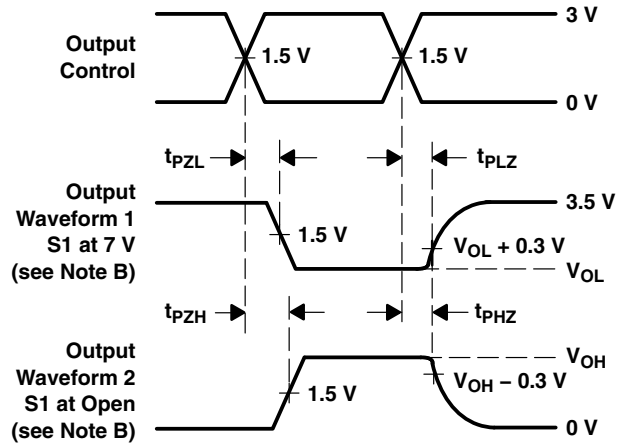
SN74CBT3384A 10-BIT FET BUS SWITCH

SCDS004L – NOVEMBER 1992 – REVISED JANUARY 2004

PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SN74CBT3384ADBQR | LIFEBUY | SSOP | DBQ | 24 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CBT3384A | |
| SN74CBT3384ADBR | LIFEBUY | SSOP | DB | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CU384A | |
| SN74CBT3384ADGVR | LIFEBUY | TVSOP | DGV | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CU384A | |
| SN74CBT3384ADW | LIFEBUY | SOIC | DW | 24 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBT3384A | |
| SN74CBT3384ADWR | LIFEBUY | SOIC | DW | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBT3384A | |
| SN74CBT3384APW | LIFEBUY | TSSOP | PW | 24 | 60 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CU384A | |
| SN74CBT3384APWR | LIFEBUY | TSSOP | PW | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CU384A | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

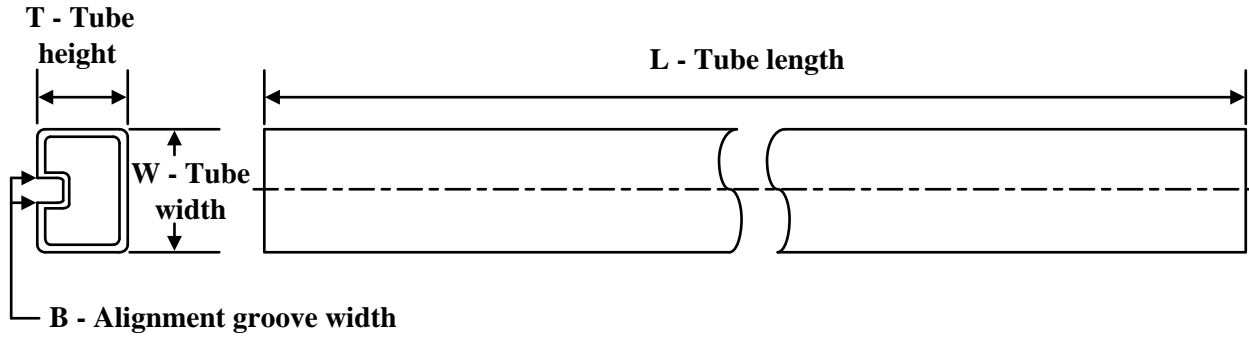

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CBT3384ADBQR | SSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74CBT3384ADBR | SSOP | DB | 24 | 2000 | 330.0 | 16.4 | 8.2 | 8.8 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74CBT3384ADGVR | TVSOP | DGV | 24 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74CBT3384ADWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74CBT3384APWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74CBT3384ADBQR | SSOP | DBQ | 24 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74CBT3384ADBR | SSOP | DB | 24 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74CBT3384ADGVR | TVSOP | DGV | 24 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74CBT3384ADWR | SOIC | DW | 24 | 2000 | 350.0 | 350.0 | 43.0 |
| SN74CBT3384APWR | TSSOP | PW | 24 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


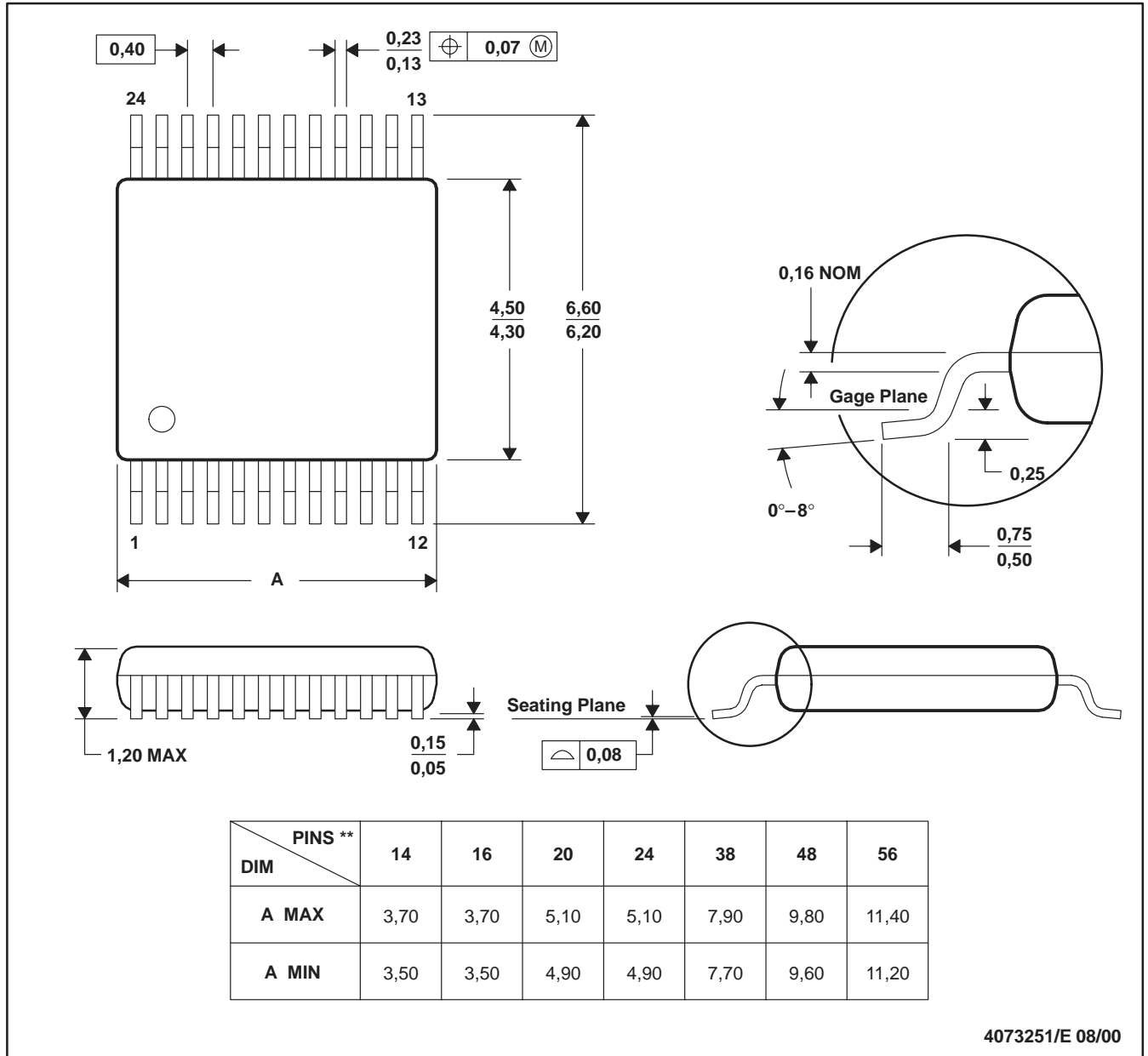
*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74CBT3384ADW | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74CBT3384APW | PW | TSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

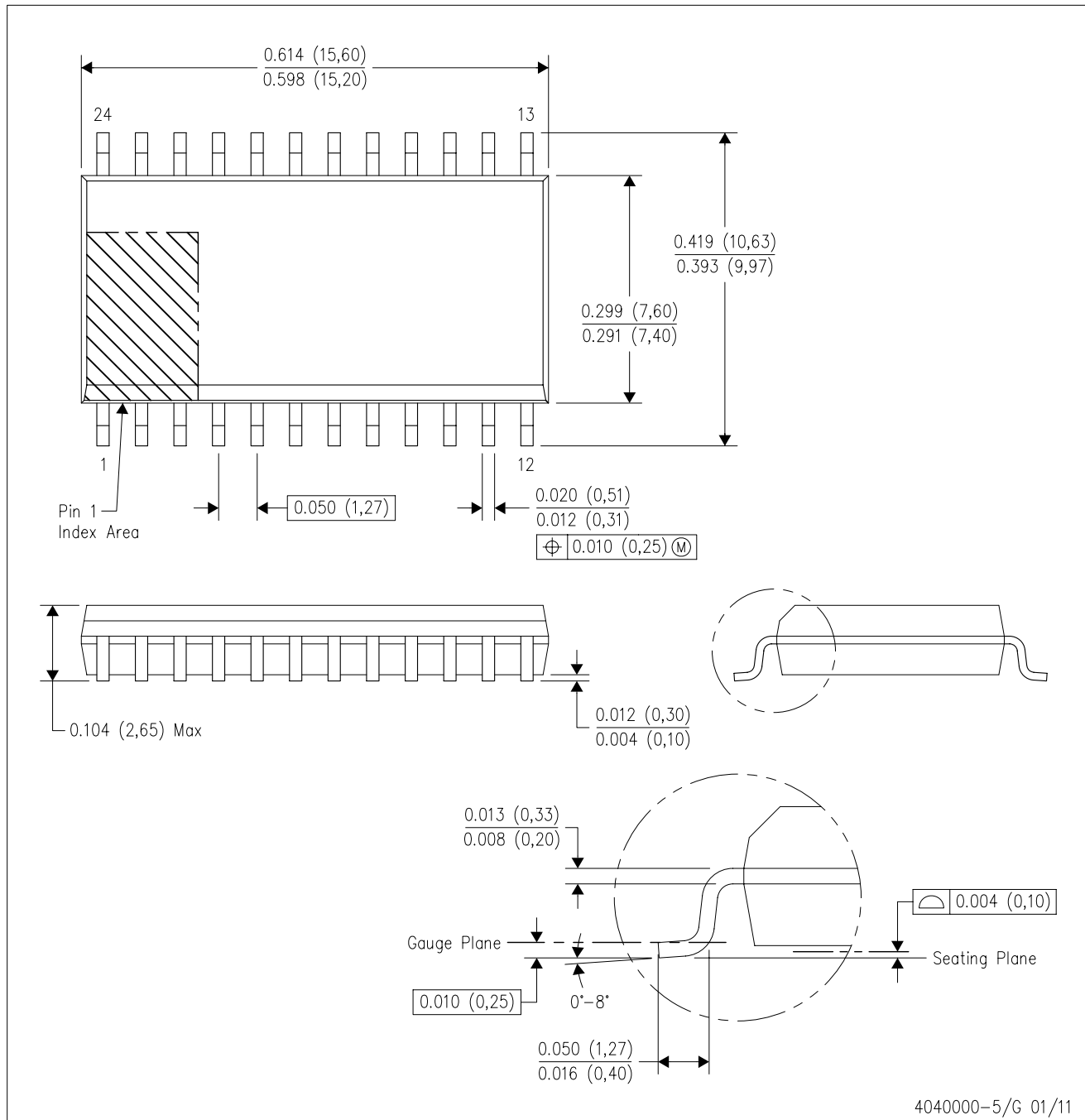
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G24)

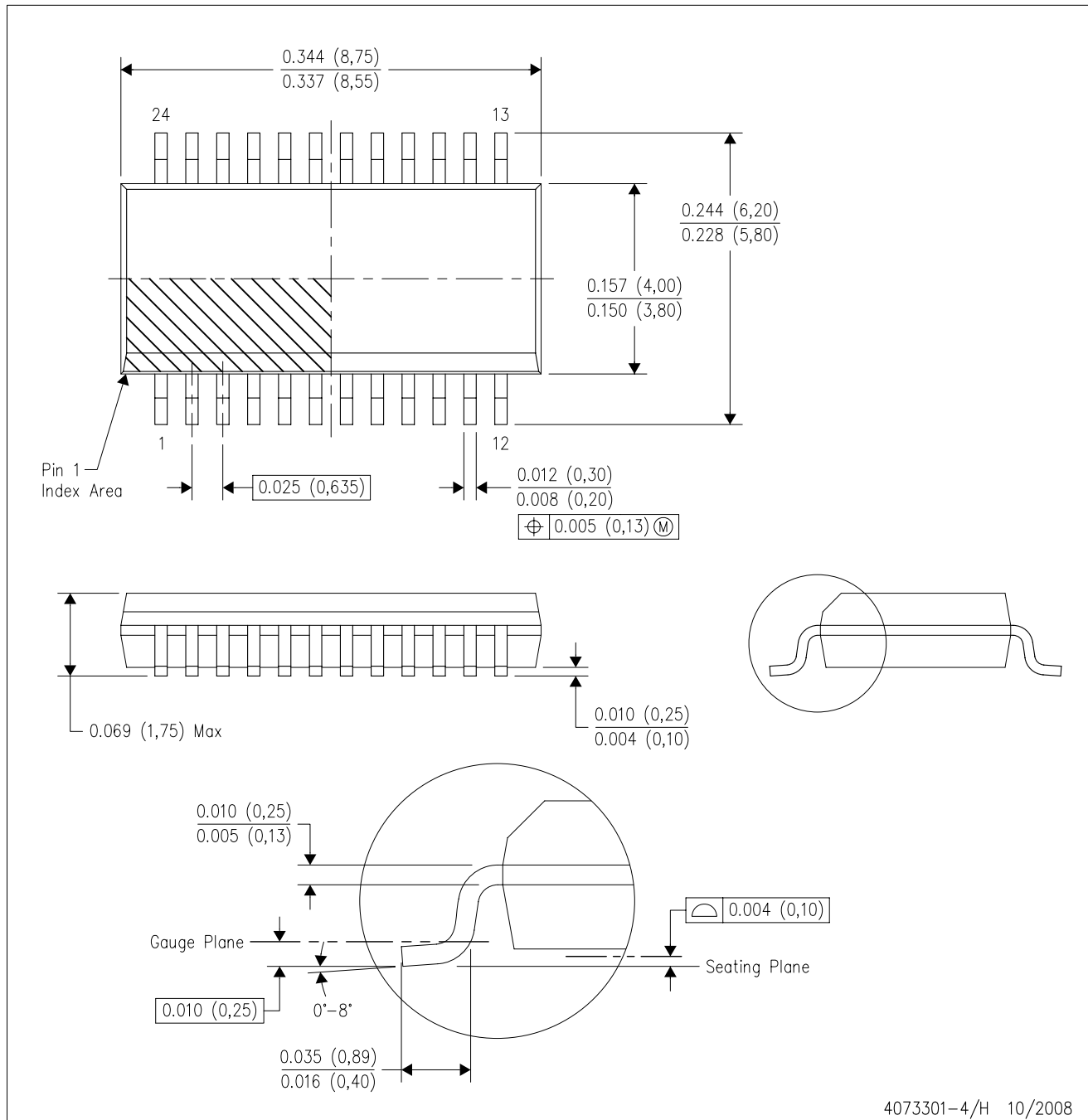
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AE.

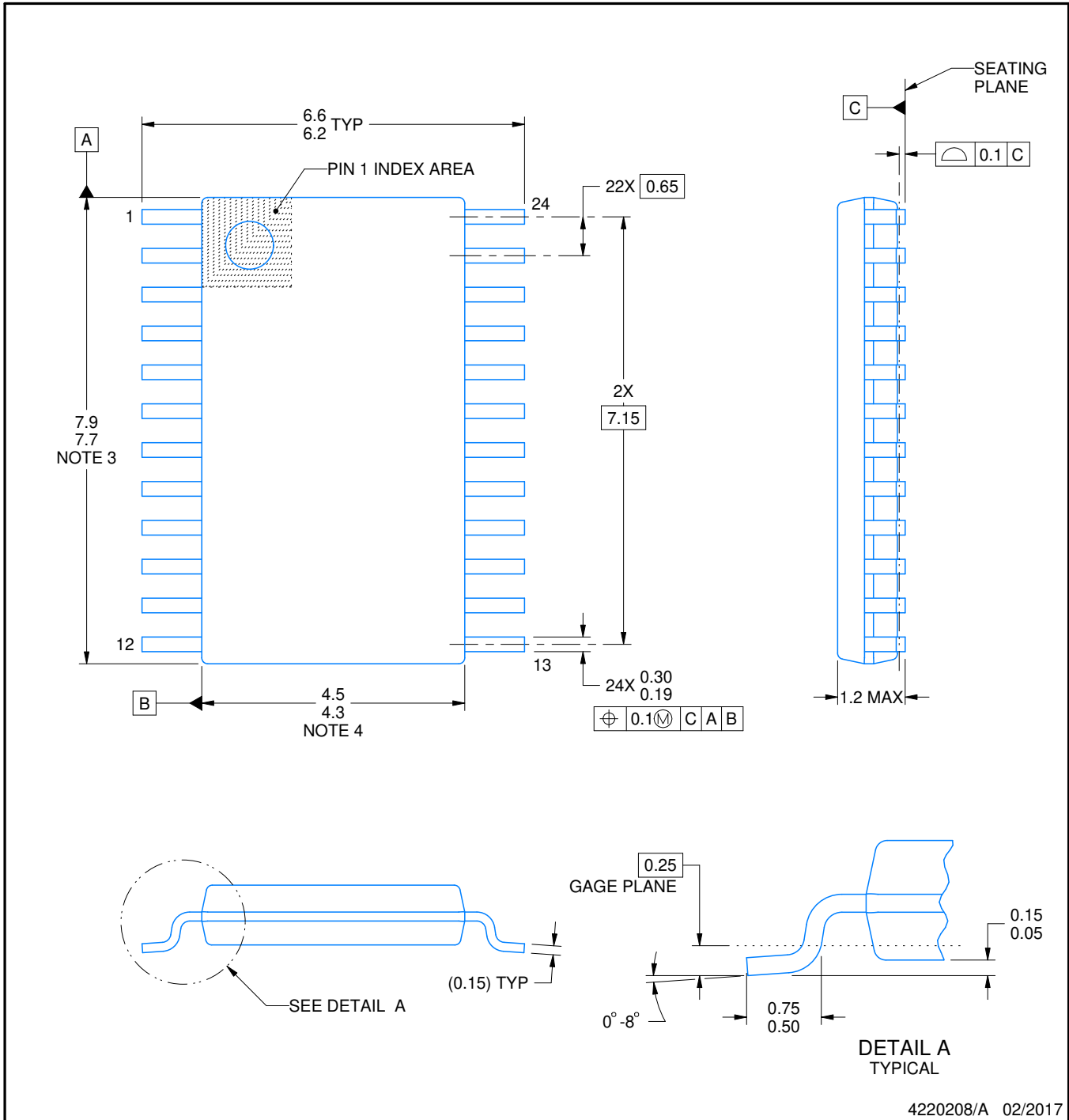
PW0024A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

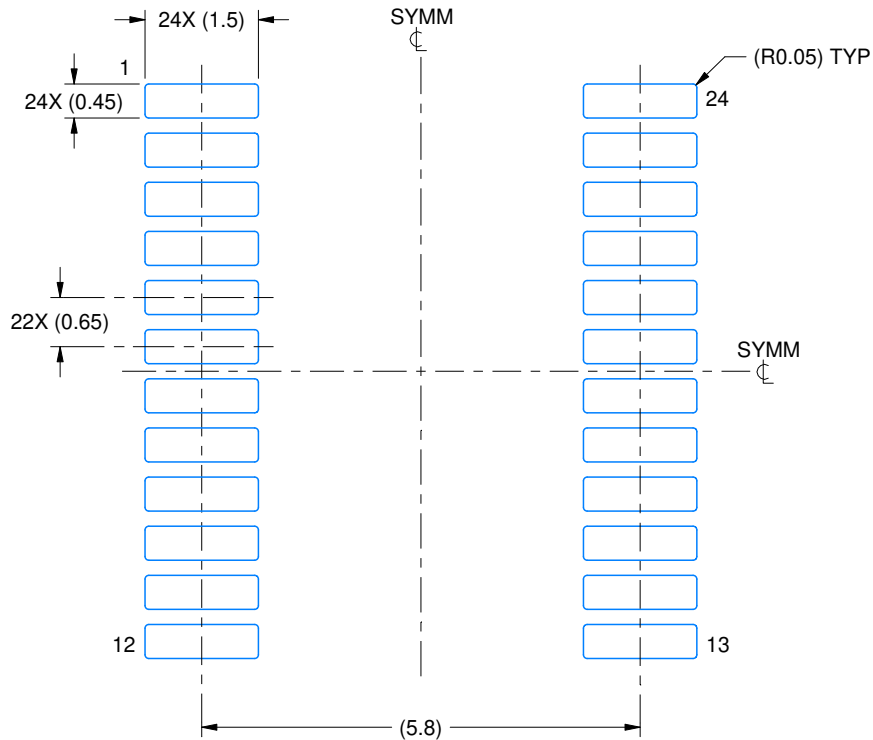
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

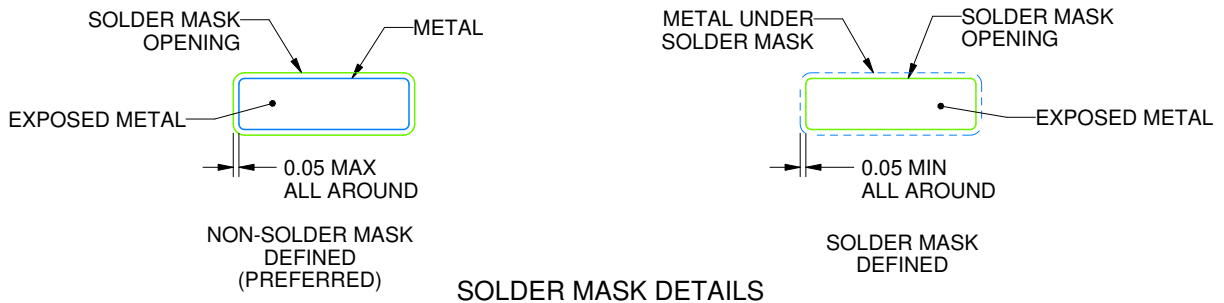
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

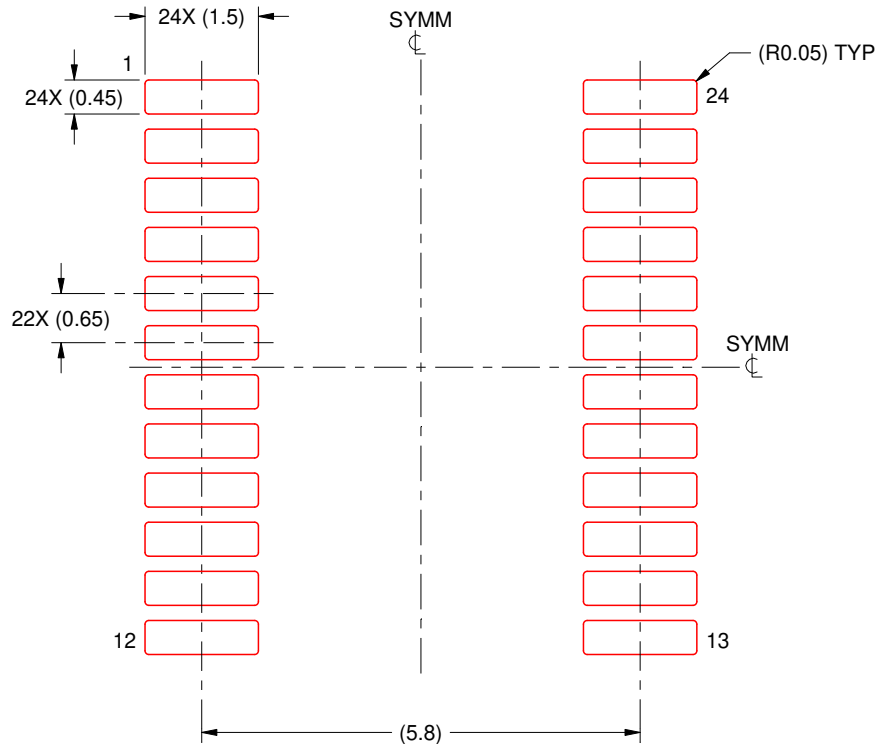
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

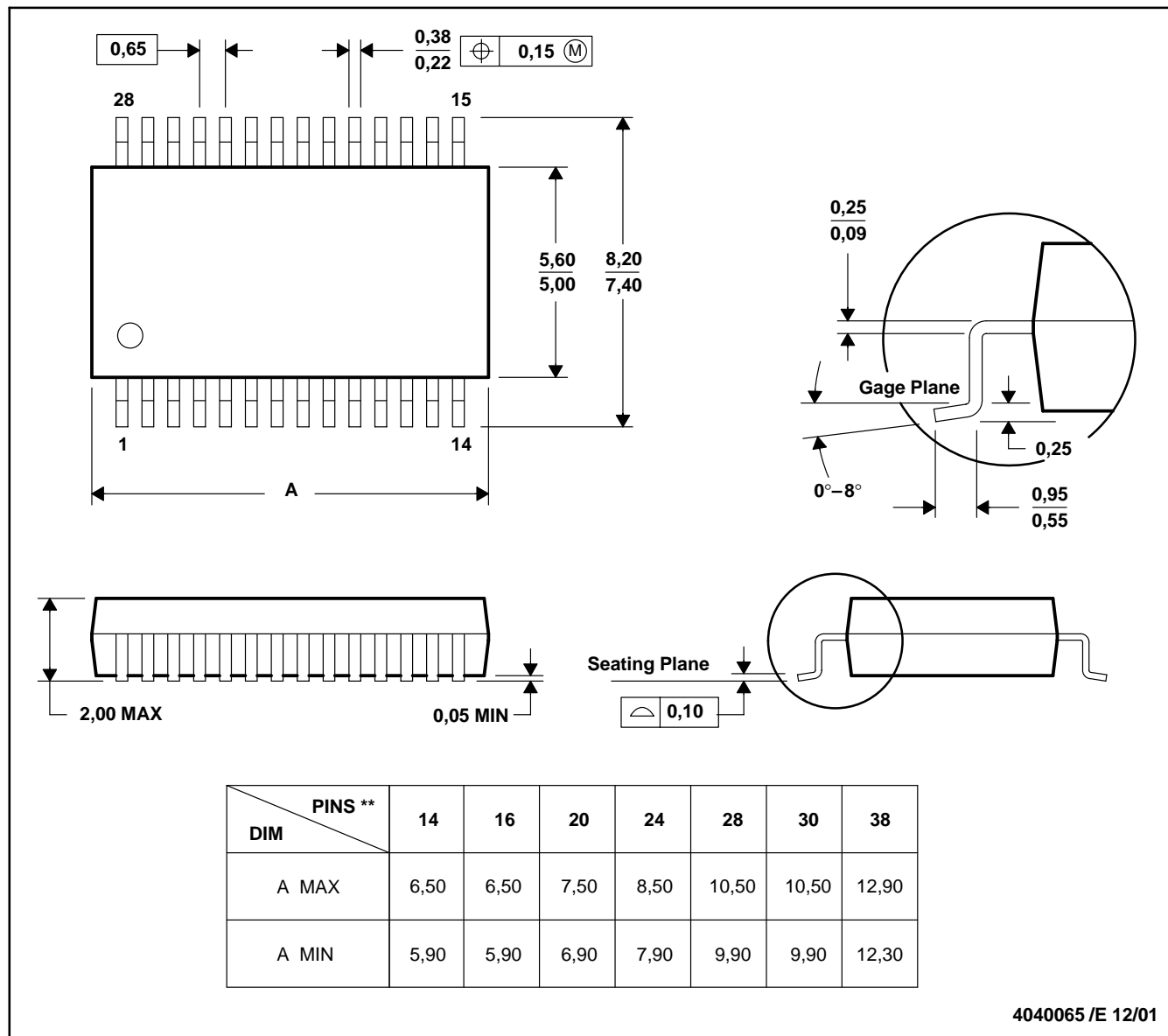
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated