

ISL54000, ISL54001, ISL54002

Integrated Audio Amplifier Systems

**NOT RECOMMENDED FOR NEW DESIGNS
NO RECOMMENDED REPLACEMENT**
contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc

FN6458
Rev 2.00
Oct 17, 2007

The Intersil ISL54000, ISL54001, ISL54002 family of devices are integrated audio power amplifier systems that combine stereo BTL 8Ω amplifiers in a single package. The devices are designed to operate from a single +2.7V to +5V power supply. All devices are offered in a 20 Ld 4x4 thin QFN package. Targeted applications include handheld equipment such as cell-phones, MP3 players, and games/toys.

The ISL54000, ISL54001, ISL54002 parts contain two class AB bridge-tied (BTL) type power amplifiers for driving stereo 8Ω speakers. Each BTL is capable of delivering 800mW (typ) with 0.4% THD+N and 941mW (typ) with 1% THD+N of continuous average power into an 8Ω BTL speaker load when using a 5V supply.

The ISL54001 and ISL54002 feature a 2:1 stereo input multiplexer front-end. This allows selection between two stereo sources. In addition the ISL54002 has the capability of mixing the stereo inputs.

All devices in this family feature low power shutdown, thermal overload protection and click/pop suppression. The click and pop circuitry eliminates audible transients during audio source changes and transitioning in and out of shutdown.

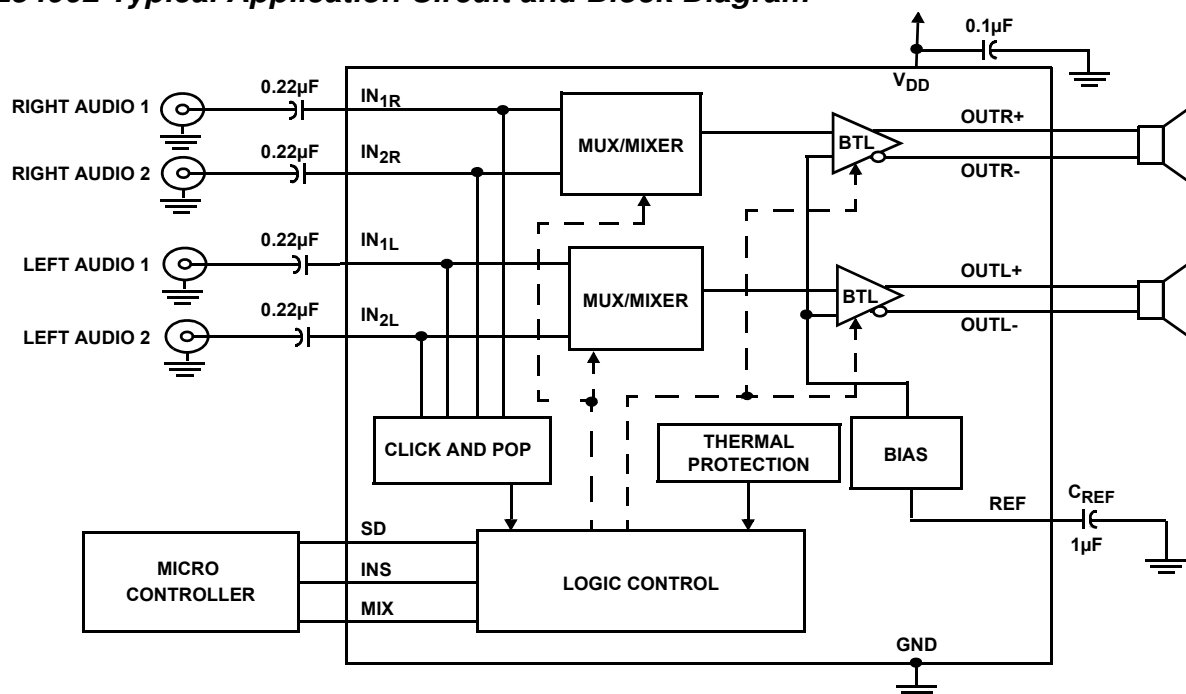
Features

- Pb-Free (RoHS Compliant)
- Class AB 941mW Stereo BTL Speaker Amplifiers
- Single Supply Operation. +2.7V to +5.5V
- THD+N at 1kHz, 800mW into 8Ω. 0.4%
- THD+N at 1kHz, 941mW into 8Ω 1%
- Low Power Shutdown
- Thermal Shutdown Protection
- “Click and Pop” Suppression Circuitry
- 2:1 Stereo Input Mux (ISL54001, ISL54002)
- Mixing of Two Stereo Inputs (ISL54002)
- TTL Logic-Compatible
- Available in 20 Ld 4x4 Thin QFN

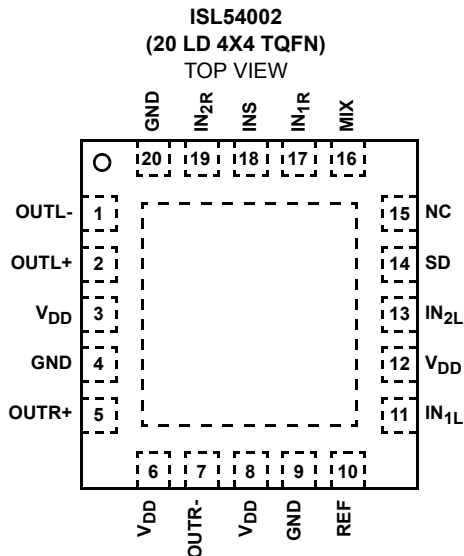
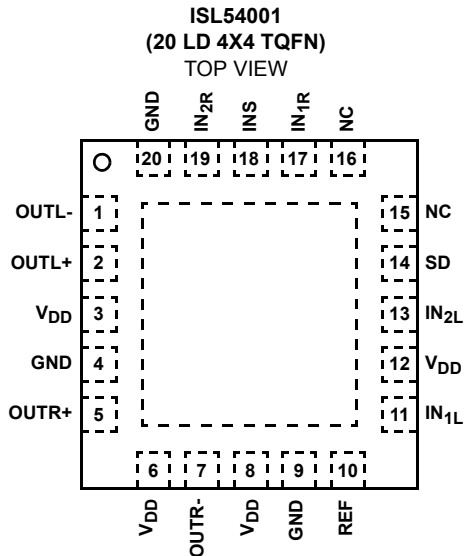
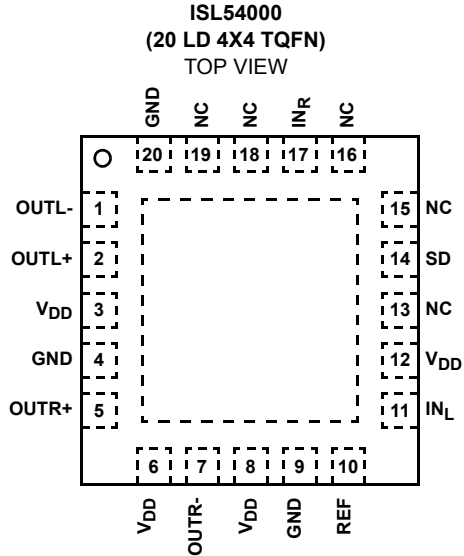
Applications

- Battery powered, Handheld, and Portable Equipment
 - Cellular/mobile Phones
 - PDA's, MP3 Players, DVD Players, Cameras
 - Laptops, Notebooks, Palmtops
 - Handheld Games and Toys
- Desktop Computers

ISL54002 Typical Application Circuit and Block Diagram



Pinouts



Pin Descriptions

PIN			NAME	FUNCTION
ISL54000	ISL54001	ISL54002		
3, 6, 8, 12	3, 6, 8, 12	3, 6, 8, 12	V _{DD}	System Power Supply
4, 9, 20	4, 9, 20	4, 9, 20	GND	Ground Connection
11	-	-	IN _L	Left Channel Audio Input 1
-	11	11	IN _{1L}	Left Channel Audio Input 1
-	13	13	IN _{2L}	Left Channel Audio Input 2
17	-	-	IN _R	Right Channel Audio Input 1
-	17	17	IN _{1R}	Right Channel Audio Input 1
-	19	19	IN _{2R}	Right Channel Audio Input 2
2	2	2	OUTL+	Positive Speaker Output
5	5	5	OUTR+	Positive Speaker Output
1	1	1	OUTL-	Negative Speaker Output
7	7	7	OUTR-	Negative Speaker Output
14	14	14	SD	Shutdown, High to disable amplifiers, Low for normal operation.
-	18	18	INS	Input Select
-	-	16	MIX	Mixer, High to mix Right and Left Audio Inputs, Low to pass Audio Inputs without mixing
10	10	10	REF	Common-mode Bias Voltage, Bypass with a 1μF capacitor to GND
13, 15, 16, 18, 19	15, 16	15	NC	No Connect

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free) Tape & Reel	PKG. DWG. #
ISL54000IRTZ* (Note)	540 00IRTZ	-40 to +85	20 Ld 4x4 TQFN (Pb-free)	L20.4x4A
ISL54001IRTZ* (Note)	540 01IRTZ	-40 to +85	20 Ld 4x4 TQFN (Pb-free)	L20.4x4A
ISL54002IRTZ* (Note)	540 02IRTZ	-40 to +85	20 Ld 4x4 TQFN (Pb-free)	L20.4x4A

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

ISL54000 Truth Table

SD	OUTR+	OUTR-	OUTL+	OUTL-
1	Disabled	Disabled	Disabled	Disabled
0	IN _R	IN _R	IN _L	IN _L

ISL54001 Truth Table

SD	INS	OUTR+	OUTR-	OUTL+	OUTL-
1	X	Disabled	Disabled	Disabled	Disabled
0	0	IN _{1R}	IN _{1R}	IN _{1L}	IN _{1L}
0	1	IN _{2R}	IN _{2R}	IN _{2L}	IN _{2L}

ISL54002 Truth Table

SD	MIX	INS	OUTR+	OUTR-	OUTL+	OUTL-
1	X	X	Disabled	Disabled	Disabled	Disabled
0	0	0	IN _{1R}	IN _{1R}	IN _{1L}	IN _{1L}
0	0	1	IN _{2R}	IN _{2R}	IN _{2L}	IN _{2L}
0	1	X	IN _{1R} + IN _{2R}	IN _{1R} + IN _{2R}	IN _{1L} + IN _{2L}	IN _{1L} + IN _{2L}

Absolute Maximum Ratings

VDD to GND	-0.3V to +6.5V
Input Voltages	
In_R, In_L, SD, INS, MIX	-0.3V to (VDD + 0.3V)
Output Voltages	
OUT_+, OUT_-	-0.3V to (VDD + 0.3V)
Continuous Current (VDD, OUT_, GND)	750mA
ESD Rating	
Human Body Model	>2kV
Machine Model	>200V
Charged Device Model	>1kV

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ld 4x4 TQFN Package	45	6.5
Maximum Junction Temperature	+150°C	
Maximum Storage Temperature Range	-65°C to +150°C	
Pb-free reflow profile	see link below	
http://www.intersil.com/pbfree/Pb-FreeReflow.asp		

Operating Conditions

Temperature Range	-40°C to +85°C
-------------------	----------------

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. θ_{JC} , the "case temp" is measured at the center of the exposed metal pad on the package underside. See Tech Brief TB379.
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications - 5V Supply

Test Conditions: $V_{DD} = +5V$, $GND = 0V$, $V_{INH} = 2.4V$, $V_{INL} = 0.8V$, $SD = MIX = INS = V_{INL}$, $C_{REF} = 1\mu F$, R_L is terminated between OUT_+ and OUT_- , Unless Otherwise Specified (Note 3).

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 4, 5)	TYP	MAX (Notes 4, 5)	UNITS
GENERAL						
Power Supply Range, V_{DD}		Full	2.7	-	5.5	V
Quiescent Supply Current, I_{DD}	INS = MIX = V_{INL} or V_{INH} , R_L = None, Inputs AC coupled to ground (0.1 μF)	25	-	4.6	12	mA
		Full	-	5.5	-	mA
Shutdown Supply Current, I_{SD}	SD = V_{INH} , INS = MIX = V_{INL} or V_{INH} , $R_L = 8\Omega$ (BTL), Inputs AC coupled to ground (0.1 μF)	25	-	28	50	μA
		Full	-	31	-	μA
Input Resistance, R_{IN}	INS = 0V or V_{DD}	25	-	100	-	k Ω
Thermal Shutdown, T_{SD}	INS = MIX = 0V or V_{DD}	25	-	150	-	°C
Thermal Shutdown Hysteresis		25	-	10	-	°C
SD to Full Operation, $T_{SD(ON)}$	INS = 0V or 5V, MIX = 0V or 5V	Full	-	1	-	ms
BTL AMPLIFIER DRIVER						
Output Offset Voltage, V_{OS}	Measured OUT_+ and OUT_- , Input AC coupled to ground (0.1 μF)	25	-	38	-	mV
		Full	-	49	-	mV
Power Supply Rejection Ratio, PSRR	$V_{RIPPLE} = 200mV_{P-P}$, $R_L = 8\Omega$, Input AC coupled to ground (0.1 μF)	$F_{RIPPLE} = 217Hz$	25	-	49	dB
		$F_{RIPPLE} = 1kHz$	25	-	47	dB
Output Power, P_{OUT}	$R_L = 8\Omega$, THD + N = 1%, f = 1kHz	25	-	941	-	mW
	$R_L = 8\Omega$, THD + N = 10%, f = 1kHz	25	-	1.23	-	W
Total Harmonic Distortion + Noise, THD + N	$R_L = 8\Omega$, $P_{OUT} = 800mW$, f = 1kHz	25	-	0.4	-	%
	$R_L = 8\Omega$, $P_{OUT} = 800mW$, f = 20Hz to 20kHz	25	-	0.7	-	%
Max Output Voltage Swing, V_{OUT}	$R_L = 8\Omega$, $V_{SIGNAL} = 5V_{P-P}$, f = 1kHz	25	7.2	7.7	-	V_{P-P}
Signal to Noise Ratio, SNR	$R_L = 8\Omega$, $P_{OUT} = 900mW$, f = 1kHz	25	-	85	-	dB
Output Noise, N_{OUT}	A - Weight filter, BW = 22Hz to 22kHz	25	-	125	-	μV_{RMS}

Electrical Specifications - 5V Supply

Test Conditions: $V_{DD} = +5V$, $GND = 0V$, $V_{INH} = 2.4V$, $V_{INL} = 0.8V$, $SD = MIX = INS = V_{INL}$, $C_{REF} = 1\mu F$, R_L is terminated between OUT_+ and OUT_- , Unless Otherwise Specified (Note 3). (Continued)

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 4, 5)	TYP	MAX (Notes 4, 5)	UNITS
Crosstalk R_{CH} to L_{CH} , L_{CH} to R_{CH}	$R_L = 8\Omega$, $P_{OUT} = 800mW$, $f = 1kHz$, Signal coupled from the input of active amplifier to the output of an adjacent amplifier with its input AC coupled to ground.	25	-	80	-	dB
Off-Isolation	$SD = V_{INH}$, $P_{OUT} = 800mW$, $f = 10kHz$, Signal coupled from input to output of a disabled amplifier.	25	-	130	-	dB
Channel Gain Matching R_{CH} to L_{CH}	$R_L = 8\Omega$, $V_{INxR} = V_{INxL} = 3.88V_{P-P}$ (Connect to the same source)	25	-	+0.1	-	dB
Channel Phase Matching R_{CH} to L_{CH}	$R_L = 8\Omega$, $V_{INxR} = V_{INxL} = 3.88V_{P-P}$ (Connect to the same source)	25	-	0.01	-	°
LOGIC INPUT						
Input Leakage Current, I_{SD} , I_{INS} , I_{MIX}	$V_{DD} = 5V$, $SD = 0V$, $INS = 0V$, $MIX = 0V$	25	-3	1.9	3	μA
		Full	-	1.9	-	μA
Input Leakage Current, I_{SD} , I_{INS} , I_{MIX}	$V_{DD} = 5V$, $SD = V_{DD}$, $INS = V_{DD}$, $MIX = V_{DD}$	25	-1	0.02	-1	μA
		Full	-	0.02	-	μA
V_{INH}		Full	2.4	-	-	V
V_{INL}		Full	-	-	0.8	V

Electrical Specifications - 3.6V Supply

Test Conditions: $V_{DD} = +3.6V$, $GND = 0V$, $V_{INH} = 1.4V$, $V_{INL} = 0.4V$, $SD = MIX = INS = GSO = GS1 = V_{INL}$, $C_{REF} = 1\mu F$, R_L is terminated between OUT_+ and OUT_- , Unless Otherwise Specified (Note 3).

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 4, 5)	TYP	MAX (Notes 4, 5)	UNITS
GENERAL						
Quiescent Supply Current, I_{DD}	$INS = 0V$ or V_{DD} , $MIX = 0V$ or V_{DD} , $R_L = \text{None}$, Input AC coupled to ground (0.1 μF)	25	-	2.7	12	mA
		Full	-	3	-	mA
Shutdown Supply Current, I_{SD}	$INS = 0V$ or V_{DD} , $MIX = 0V$ or V_{DD} , $R_L = 8\Omega$ (BTL), Input AC coupled to ground (0.1 μF)	25	-	13	50	μA
		Full	-	15	-	μA
BTL AMPLIFIER DRIVER, $HD = V_{INH}$, $HO = V_{INH}$, UNLESS OTHERWISE SPECIFIED						
Output Offset Voltage, V_{OS}	Measured between OUT_+ and OUT_- , Input AC coupled to ground (0.1 μF)	25	-	25	-	mV
		Full	-	40	-	mV
Power Supply Rejection Ratio, PSRR	$V_{RIPPLE} = 200mV_{P-P}$, $R_L = 8\Omega$, Input AC coupled to ground (0.1 μF)	$F_{RIPPLE} = 217Hz$	25	-	49	dB
		$F_{RIPPLE} = 1kHz$	25	-	47	dB
Output Power, P_{OUT}	$R_L = 8\Omega$, THD + N = 1%, $f = 1kHz$	25	-	310	-	mW
	$R_L = 8\Omega$, THD + N = 10%, $f = 1kHz$	25	-	528	-	mW
Total Harmonic Distortion + Noise, THD + N	$R_L = 8\Omega$, $P_{OUT} = 200mW$, $f = 1kHz$	25	-	0.4	-	%
	$R_L = 8\Omega$, $P_{OUT} = 200mW$, $f = 20kHz$ to 20kHz	25	-	0.4	-	%
Max Output Voltage Swing, V_{OUT}	$R_L = 8\Omega$, $V_{SIGNAL} = 3.6V_{P-P}$, $f = 1kHz$	25	-	5.8	-	V_{P-P}
LOGIC INPUT						
Input Leakage Current, I_{SD} , I_{INS} , I_{MIX}	$V_{DD} = 5V$, $SD = 0V$, $INS = 0V$, $MIX = 0V$	25	-3	1.9	3	μA
		Full	-	1.9	-	μA

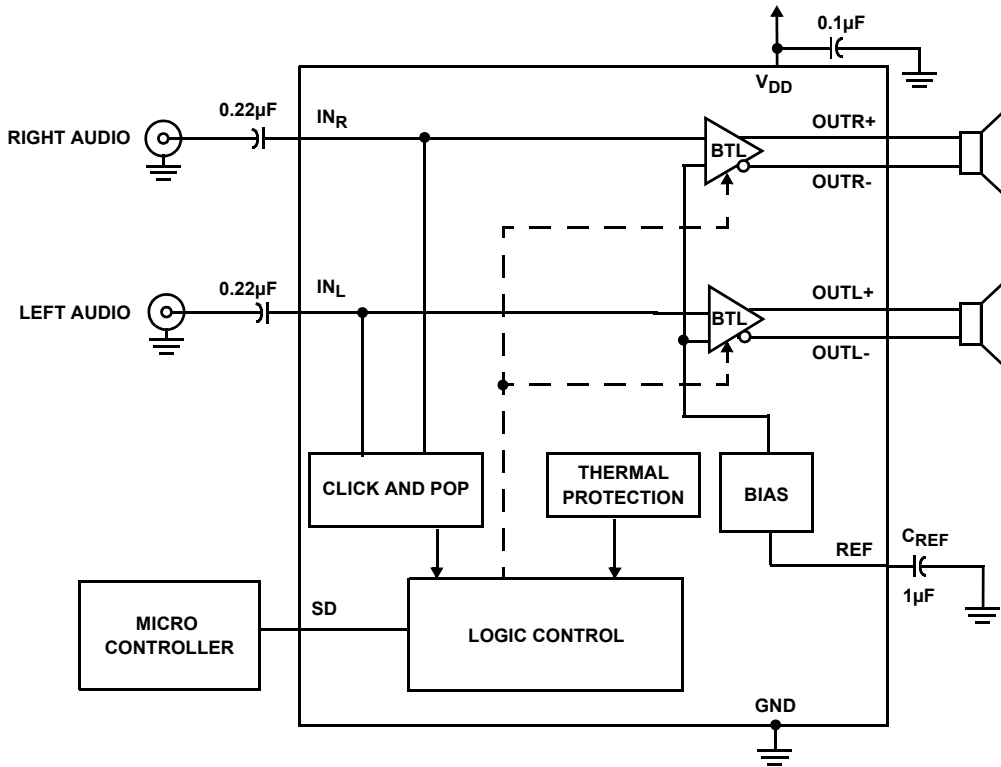
Electrical Specifications - 3.6V Supply Test Conditions: $V_{DD} = +3.6V$, $GND = 0V$, $V_{INH} = 1.4V$, $V_{INL} = 0.4V$, $SD = MIX = INS = GSO = GS1 = V_{INL}$, $C_{REF} = 1\mu F$. R_L is terminated between OUT_+ and OUT_- , Unless Otherwise Specified (Note 3). **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 4, 5)	TYP	MAX (Notes 4, 5)	UNITS
Input Leakage Current, I_{SD} , I_{INS} , I_{MIX}	$V_{DD} = 5V$, $SD = V_{DD}$, $INS = V_{DD}$, $MIX = V_{DD}$	25	-1	0.02	1	μA
		Full	-	0.02	-	μA
V_{INH}		Full	1.4	-	-	V
V_{INL}		Full	-	-	0.4	V

NOTES:

- V_{IN} = input voltage to perform proper function.
- The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

ISL54000 Typical Application Circuit and Block Diagram



© Copyright Intersil Americas LLC 2007. All Rights Reserved.

All trademarks and registered trademarks are the property of their respective owners.

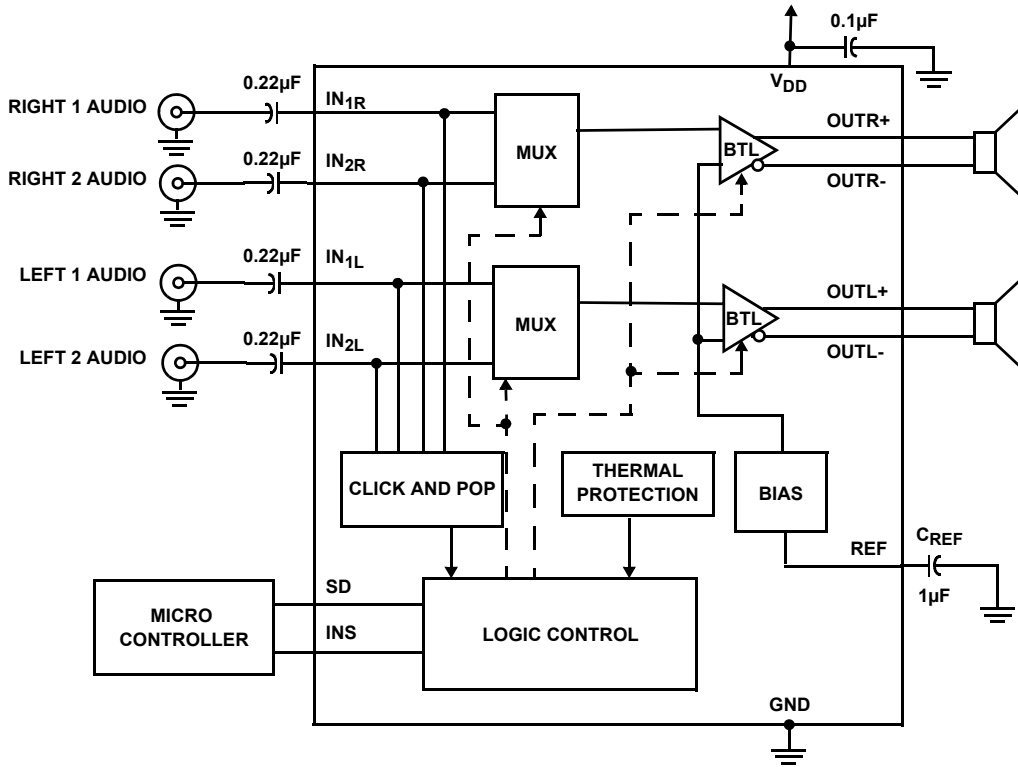
For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

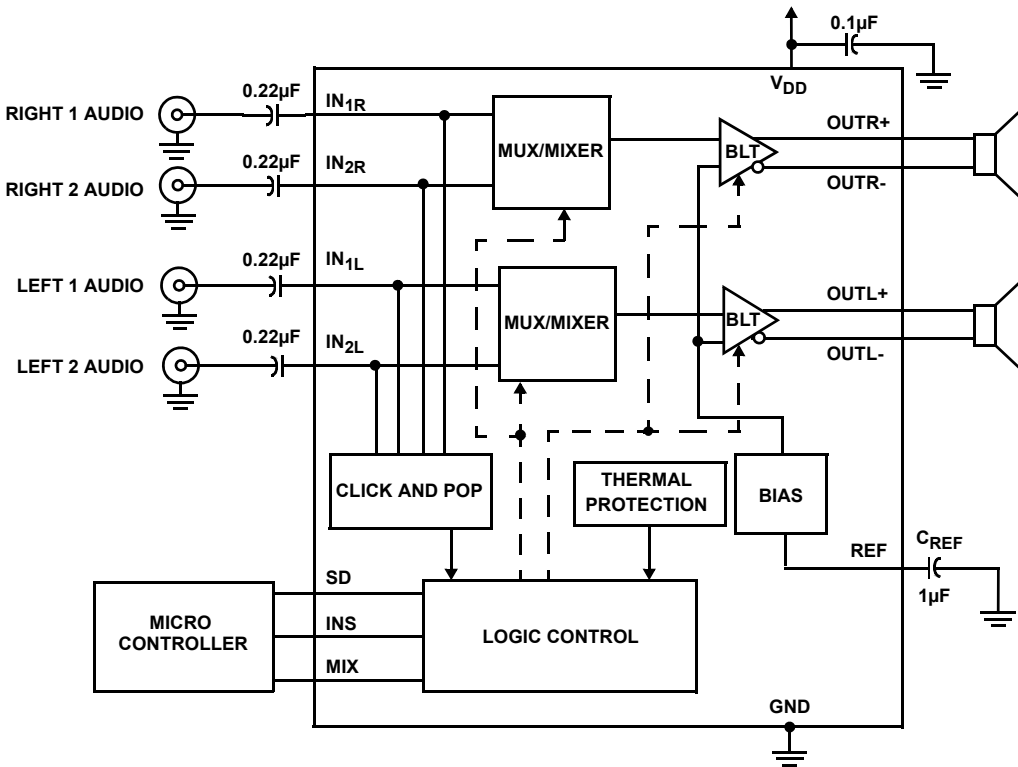
Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

ISL54001 Typical Application Circuit and Block Diagram



ISL54002 Typical Application Circuit and Block Diagram



Detailed Description

The Intersil ISL54000, ISL54001, ISL54002 family of devices are integrated audio power amplifier systems designed to drive 8Ω speaker loads. They can operate with a supply voltage of +2.7V to +5V and provide good quality audio, while requiring minimal external components. Its low 0.4% THD+N while driving 800mW into an 8Ω speaker ensures clean, low distortion amplification of the audio signals. The devices are offered in a 20 Ld 4x4 TQFN package. Targeted applications include handheld equipment such as cell-phones, MP3 players, and games/toys.

The ISL54000, ISL54001, ISL54002 parts contain two class AB bridge-tied (BTL) type power amplifiers for driving stereo 8Ω speakers. When powered with a 5V supply, each BTL is capable of delivering 941mW (typ) of continuous average power to an 8Ω speaker load with 1% THD+N performance. When the speaker load is connected across the positive and negative terminals of the BTL driver, the voltage is doubled across the load and the power is quadrupled.

The ISL54001 and ISL54002 feature a 2:1 stereo input multiplexer front-end. This allows selection between two stereo sources. The INS control pin determines which stereo input is active. Applying a logic "0" to the INS control pin selects stereo input 1 (R₁ and L₁). Applying a logic "1" to the INS control pin selects stereo input 2 (R₂ and L₂).

The ISL54002 has the capability of mixing the two stereo inputs. When in MIX Mode (MIX = "1") the ISL54002 mixes the R₁ input with the R₂ input and sends the combined signal to the OUTR_ BTL driver and it mixes the L₁ input with the L₂ input and sends the combined signal to the OUTL_ BTL driver.

All devices in this family feature low power shutdown, thermal overload protection and click/pop suppression. The click and pop circuitry prohibits switching between input channels until the audio input signals are at their lowest point, which eliminates audible transients in the speakers when changing audio input sources. The click/pop circuitry also keeps speaker transients to an inaudible level when entering and leaving shutdown.

Typical application circuits and block diagrams for each device in the family are on page 6 and 7.

DC Bias Voltage

The ISL54000, ISL54001, ISL54002 have internal DC bias circuitry, which DC offsets the incoming audio signal at V_{DD}/2. When using a 5V supply, the DC offset will be 2.5V. When using a 3.6V supply, the DC offset will be 1.8V.

Since the signal gets biased internally at V_{DD}/2, the audio signals need to be AC coupled to the inputs of the device. The value of the AC coupling capacitor depends on the low frequency range required for the application. A capacitor of 0.22μF will pass a signal as low as 7.2Hz. The formula required

to calculate the capacitor value is shown in Equation 1:

$$C \geq 1/6.28 \cdot f \cdot 100k\Omega \quad (\text{EQ. 1})$$

The 100kΩ is the impedance looking into the input of the ISL54000, ISL54001, and ISL54002 devices.

BTL Speaker Amplifiers

The ISL54000, ISL54001, and ISL54002 contain two bridge-tied load (BTL) amplifiers designed to drive a speaker load differentially. The output from one BTL is OUTL+ and OUTL-. The output of the other BTL is OUTR+ and OUTR-.

A single BTL driver consists of inverting and non-inverting power op amps. The AC signal out of each op amp are equal in magnitude but 180° out-of-phase, so the AC signal at OUTL+ and OUTL- have the same amplitude but are 180° out-of-phase. The same is true of OUTR+ and OUTR-. The speaker load gets connected between the + terminal and - terminal outputs.

Driving the load differentially using a BTL configuration doubles the output voltage across the speaker load and quadruples the power to the load. In effect you get a gain of two due to this configuration at the load as compared to driving the load with a single-ended amplifier with its load connected between a single amplifier's output and ground.

The outputs of each BTL are biased at V_{DD}/2. When the load gets connected across the + and - terminal of the BTL, the mid supply DC bias voltage at each output gets cancelled out eliminating the need for large bulky output coupling capacitors.

Low Power Shutdown

With a logic "1" at the SD control pin the device enters the low power shutdown state. When in shutdown the output amplifiers go into an high impedance state and supply current is reduced to 26μA (typ).

In shutdown mode before the amplifiers enter the high impedance/low current drive state, the bias voltage of V_{DD}/2 remains connected at the output through a 100kΩ resistor. This resistor is not present during active operation of the drivers but gets switched in when the SD pin goes high and disconnected when the SD pin goes low.

Leaving the DC bias voltage connected through this 100kΩ resistor reduces the transient that is generated across the speaker, while going into or out of shutdown, to a level that does not produce clicking or popping in the speaker.

QFN Thermal Pad Considerations

The QFN package features an exposed thermal pad on its underside. This pad lowers the package's thermal resistance by providing a direct heat conduction path from the die to the PCB. Connect the exposed thermal pad to GND by using a large copper pad and multiple vias to the GND plane. The vias

should be plugged and tented with plating and solder mask to ensure good thermal conductivity.

Best thermal performance is achieved with the largest practical copper ground plane area.

PCB Layout Considerations and Power Supply Bypassing

To maintain the highest load dissipation and widest output voltage swing the power supply PCB traces and the traces that connect the output of the drivers to the speaker loads should be made as wide as possible to minimize losses due to parasitic trace resistance.

Proper supply bypassing is necessary for high power supply rejection and low noise performance. A filter network consisting of a 10 μ F capacitor in parallel with a 0.1 μ F capacitor is recommended at the voltage regulator that is providing the power to the ISL54000, ISL54001, and ISL54002 IC.

Local bypass capacitors of 0.1 μ F should be put at each V_{DD} pin of the ISL54000, ISL54001, ISL54002 devices. They should be located as close as possible to the pin, keeping the length of leads and traces as short as possible.

A 1 μ F capacitor from the REF pin (pin 10) to GND is needed for optimum PSRR and internal bias voltage stability.

Typical Performance Curves $T_A = +25^\circ\text{C}$, Unless Otherwise Specified.

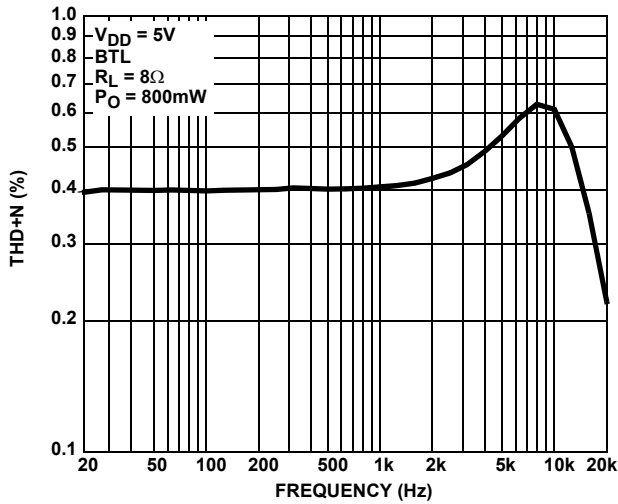


FIGURE 1. THD+N vs FREQUENCY

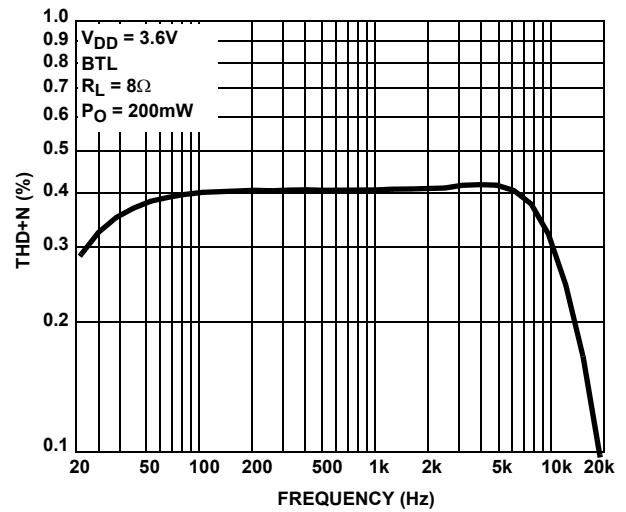


FIGURE 2. THD+N vs FREQUENCY

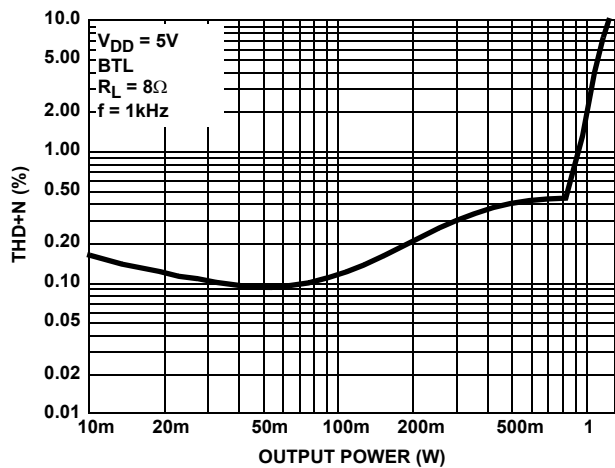


FIGURE 3. THD+N vs OUTPUT POWER

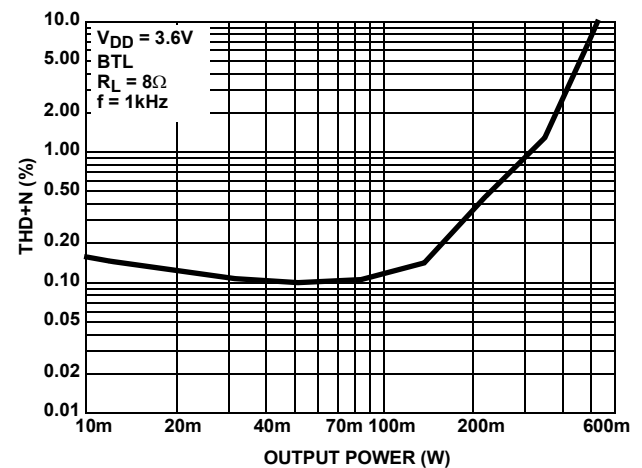


FIGURE 4. THD+N vs OUTPUT POWER

Typical Performance Curves $T_A = +25^\circ\text{C}$, Unless Otherwise Specified. (Continued)

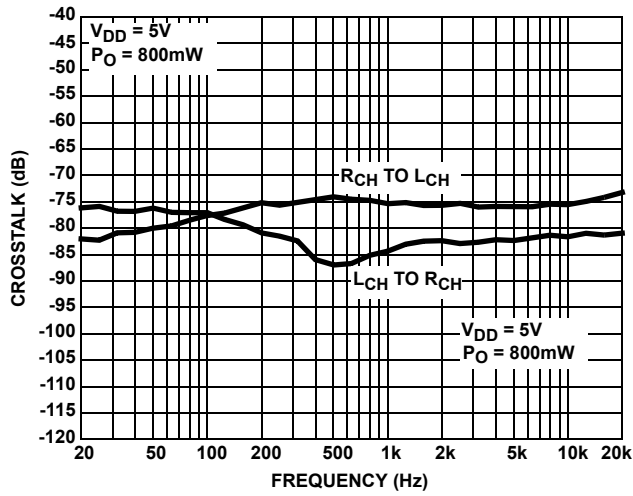


FIGURE 5. CROSSTALK vs FREQUENCY

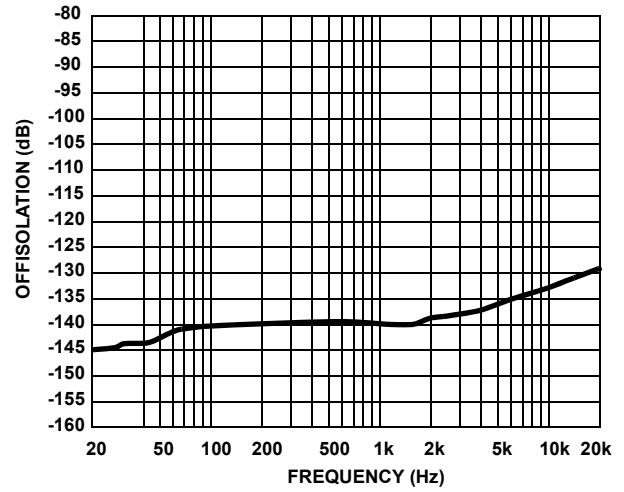


FIGURE 6. OFFISOLATION vs FREQUENCY

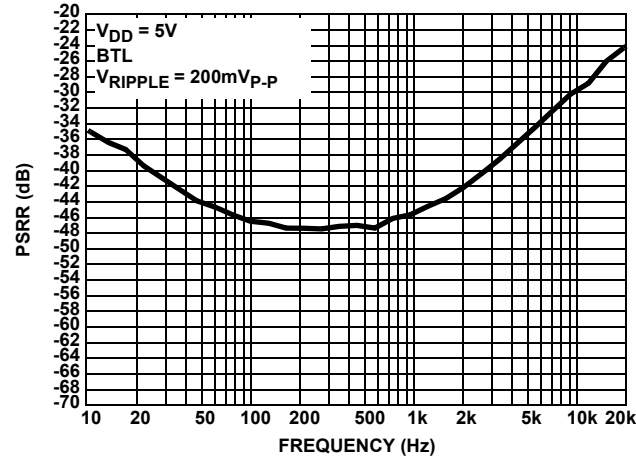


FIGURE 7. PSRR vs FREQUENCY

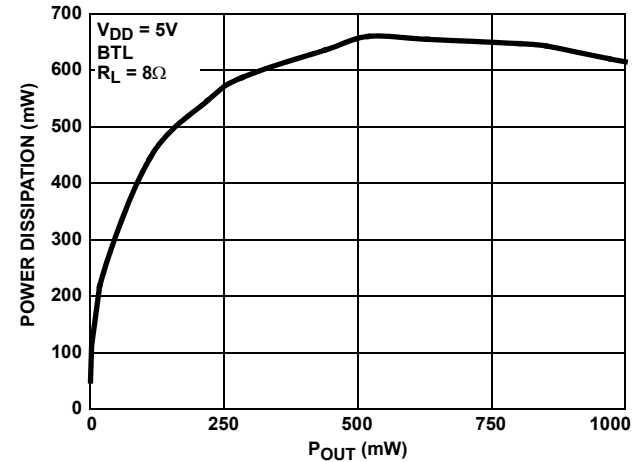


FIGURE 8. POWER DISSIPATION vs OUTPUT POWER

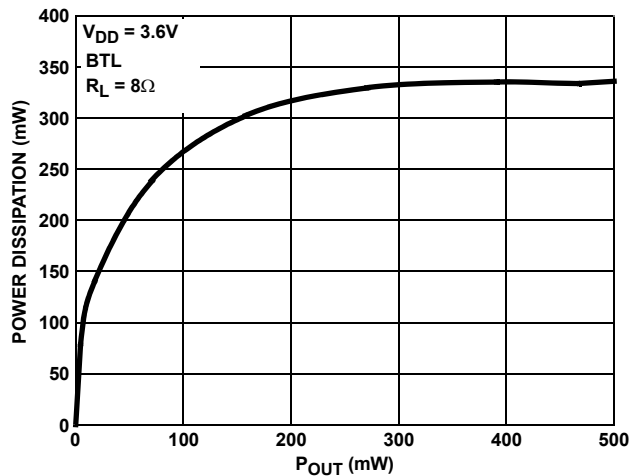


FIGURE 9. POWER DISSIPATION vs OUTPUT POWER

Die Characteristics

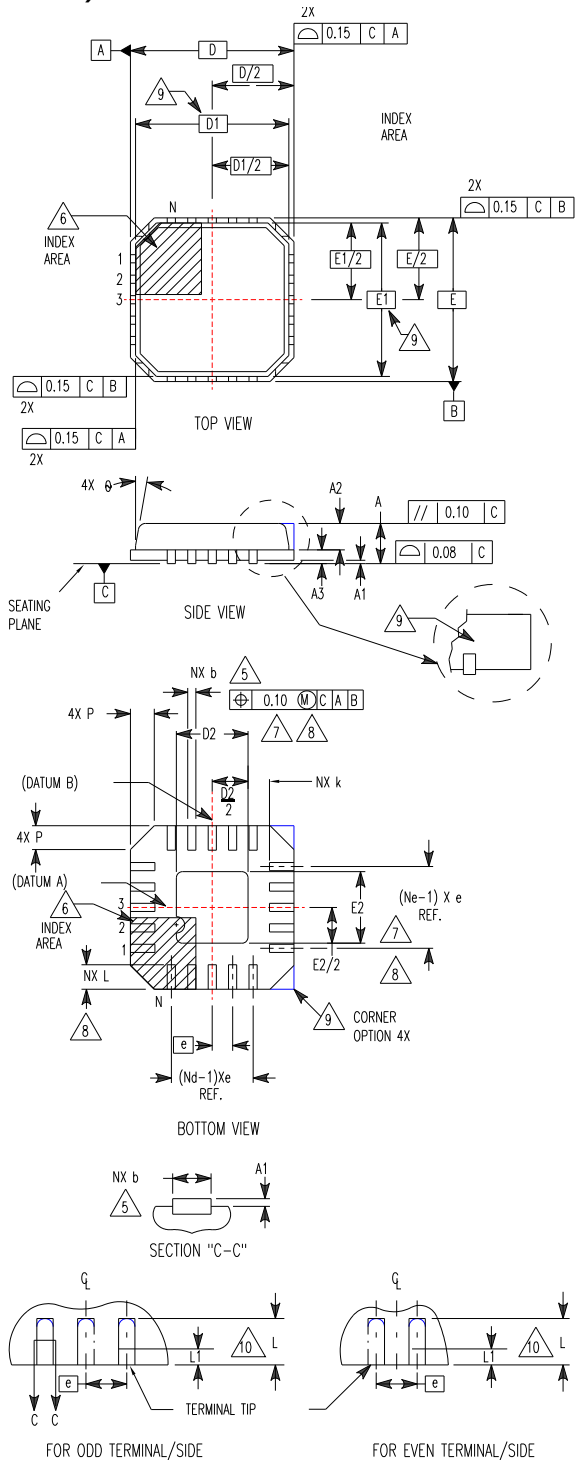
SUBSTRATE POTENTIAL (POWERED UP):

GND

PROCESS:

Submicron CMOS

Thin Quad Flat No-Lead Plastic Package (TQFN)
Thin Micro Lead Frame Plastic Package (TMLFP)



L20.4x4A

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
 (COMPLIANT TO JEDEC MO-220WGGD-1 ISSUE I)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	0.02	0.05	-
A2	-	0.55	0.80	9
A3	0.20 REF			9
b	0.18	0.25	0.30	5, 8
D	4.00 BSC			-
D1	3.75 BSC			9
D2	1.95	2.10	2.25	7, 8
E	4.00 BSC			-
E1	3.75 BSC			9
E2	1.95	2.10	2.25	7, 8
e	0.50 BSC			-
k	0.20	-	-	-
L	0.35	0.60	0.75	8
N	20			2
Nd	5			3
Ne	5			3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 0 11/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.