Agilent WS2411
4 x 4 Power Amplifier Module for UMTS1900 (1850 – 1910 MHz)
Data Sheet

Description
The WS2411, a Wide-band Code Division Multiple Access (WCDMA) Power Amplifier (PA), is a fully matched 10-pin surface mount module developed for WCDMA handset applications. This power amplifier module operates in the 1850 – 1910 MHz bandwidth. The WS2411 meets the stringent WCDMA linearity requirements for output power of up to 28.5 dBm. A low current (Vcont) pin is provided for high efficiency improvement of the low output power range.

The WS2411 features CoolPAM Circuit technology offering state-of-the-art reliability, temperature stability and ruggedness.

The WS2411 is self contained, incorporating 50ohm input and output matching networks.

Features
- **CoolPAM circuit technology**
- **Good linearity**
- **High efficiency**
- **10-pin surface mounting package (4 mm x 4 mm x 1.4 mm)**
- **Low power-state control**
- **Low quiescent current**
- **Internal 50Ω matching networks for both RF input and output**

Applications
- **WCDMA handsets**
- **HSDPA handsets**

Functional Block Diagram

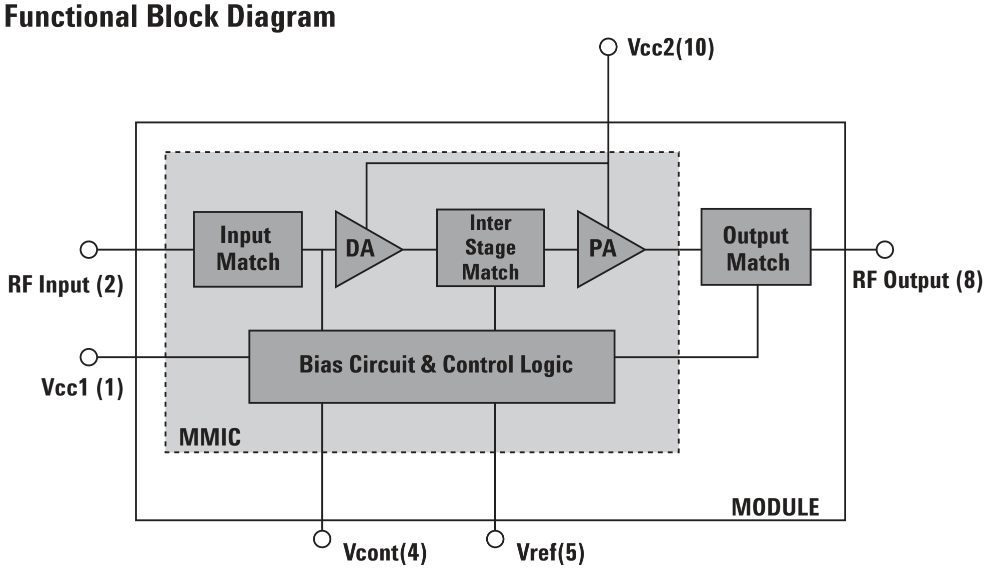


Table 1. Absolute Maximum Ratings[1]

Parameter	Symbol	Min.	Nominal	Max.	Unit
RF Input Power	P_{in}	–	–	10.0	dBm
DC Supply Voltage	V_{cc}	–	3.4	5.0	V
DC Reference Voltage	V_{ref}	–	2.85	3.3	V
Storage Temperature	T_{stg}	-55	–	+125	°C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min.	Nominal	Max.	Unit
DC Supply Voltage – Mid/High Power Mode – Low Power Mode	V_{cc}	3.2	3.4 1.5	4.2	V V
DC Reference Voltage	V_{ref}	2.75	2.85	2.95	V
Mode Control Voltage – High Power Mode – Low/Mid Power Mode	V_{cont} V_{cont}	– –	0 2.85	– –	V V
Operating Frequency	Fo	1850		1910	MHz
Ambient Temperature	Ta	-20	25	90	°C

Table 3. Power Range Truth Table

Power Mode	Symbol	Vref	Vcont[2]	Vcc	Range
High Power Mode[3]	PR3	2.85	Low	3.4	~28.5 dBm
Mid Power Mode[3]	PR2	2.85	High	3.4	~16 dBm
Low Power Mode[3]	PR1	2.85	High	1.5	~ 7 dBm
Shut Down Mode[4]	–	0.00	X	3.4	–

Notes:

1. No damage assuming only one parameter is set at limit at a time with all other parameters set at or below nominal value.
2. High (1.5V – 3.0V), Low (0.0V – 0.5V).
3. To change between High Power Mode and Low Power Mode, switch Vcont accordingly.
4. In order to shut down the module, turn off Vref accordingly.

Table 4. Electrical Characteristics for WCDMA Mode (Vref=2.85V, Vcc=3.4V, T=+25°C)[1]

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Frequency Range		F		1850		1910	MHz
Gain		Gain_hiw [2]	High Power Mode, Pout=28.5 dBm	24	27		dB
		Gain_hi	High Power Mode, Pout=28.5 dBm	24	27		dB
		Gain_mid	Mid Power Mode, Pout=16.0 dBm	14	17		dB
		Gain_low	Low Power Mode, Pout=7.0 dBm, Vcc=1.5V	10	13.5		dB
Power Added Efficiency		PAE_hiw [2]	High Power Mode, Pout=28.5 dBm	37.5	41.5		%
		PAE_hi	High Power Mode, Pout=28.5 dBm	38.5	42		%
		PAE_mid	Mid Power Mode, Pout=16.0 dBm	16.4	21		%
		PAE_low	Low Power Mode, Pout=7.0 dBm, Vcc=1.5V	10.2	15.5		%
Total Supply Current		Icc_hiw [2]	High Power Mode, Pout=28.5 dBm		500	550	mA
		Icc_hi	High Power Mode, Pout=28.5 dBm		490	540	mA
		Icc_mid	Mid Power Mode, Pout=16.0 dBm		54	70	mA
		Icc_low	Low Power Mode, Pout=7.0 dBm, Vcc=1.5V		21	33	mA
Quiescent Current		Iq_hi	High Power Mode	45	65	90	mA
		Iq_mid	Mid Power Mode	7	13	22	mA
		Iq_low	Low Power Mode, Vcc=1.5V	5	11	18	mA
Reference Current		Iref_hi	High Power Mode		3.5	7	mA
		Iref_mid	Mid Power Mode		4	8	mA
		Iref_low	Low Power Mode, Vcc=1.5V		4	8	mA
Control Current [3]		Icont_mid	Mid Power Mode		0.18	1	mA
		Icont_low	Low Power Mode, Vcc=1.5V		0.18	1	mA
Total Current in Power-down mode		Ipd	Vref=0.0V		0.2	5	µA
ACLR in High power mode [4]	5 MHz offset	ACLR1_hiw [2]	High Power Mode, Pout=28.5 dBm	–	-41	-37	dBc
	10 MHz offset	ACLR2_hiw [2]	High Power Mode, Pout=28.5 dBm	–	-54	-47	dBc
ACLR in High power mode [4]	5 MHz offset	ACLR1_hi	High Power Mode, Pout=28.5 dBm	–	-39	-37	dBc
	10 MHz offset	ACLR2_hi	High Power Mode, Pout=28.5 dBm	–	-53	-47	dBc
ACLR in Mid power mode [4]	5 MHz offset	ACLR1_mid	Mid Power Mode, Pout=16.0 dBm	–	-42	-37	dBc
	10 MHz offset	ACLR2_mid	Mid Power Mode, Pout=16.0 dBm	–	-55	-47	dBc
ACLR in Low power mode [4]	5 MHz offset	ACLR1_low	Low Power Mode, Pout=7.0 dBm, Vcc=1.5V	–	-40	-37	dBc
	10 MHz offset	ACLR2_low	Low Power Mode, Pout=7.0 dBm, Vcc=1.5V	–	-55	-47	dBc
Harmonic Suppression	Second	2f0	High Power Mode, Pout=28.5 dBm	–	-36	-30	dBc
	Third	3f0	High Power Mode, Pout=28.5 dBm	–	-60	-45	dBc
Input VSWR		VSWR		–	2:1	2.5:1	
Stability (Spurious Output)		S	VSWR 6:1, All phase	–	–	-60	dBc
Noise Power in Rx Band		RxBN	High Power Mode, Pout=28.5 dBm	–	-136.5	-133	dBm/Hz

Notes:

1. Electrical characteristics are specified under HSDPA modulated Up-Link signal (DPCCH/DPDCH=12/15, HS-DPCCH/DPDCH=15/15) unless specified otherwise.
2. Specified under WCDMA modulated (3GPP Uplink DPCCH + 1DPDCH) signal.
3. Control current when series 6.2kohm is used.
4. ACP is expressed as a ratio of total adjacent power to signal power, both with 3.84 MHz bandwidth at specified offsets.

Table 4, continued. Electrical Characteristics for WCDMA Mode (Vref=2.85V, Vcc=3.4V, T=+25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Ruggedness		Ru	Pout<28.5dBm, Pin<10dBm, All phase	–	–	10:1	VSWR
Phase discontinuity		Ph mid_hi	Mid <–> Hi at Pout=16.0dBm	–	12	25	Degree
		Ph low_mid	Low <–> Mid at Pout=7.0dBm	–	12	25	Degree
Switching Time High [5]	DC	TswhighDC		–	20	–	µs
	RF	TswhighRF		–	1	–	µs
Switching Time Low [5]	DC	TswlowDC		–	20	–	µs
	RF	TswlowRF		–	1	–	µs
Turn On Time [6]	DC	TonDC		–	20	–	µs
	RF	TonRF		–	1	–	µs
Turn Off Time [6]	DC	ToffDC		–	20	–	µs
	RF	ToffDC		–	1	–	µs

Notes:

5. TswhighDC, TswlowDC is time required to reach stable quiescent bias (10%) after Vcont is switched low and high, respectively. TswhighRF, TswlowRF is time required to reach final output power(±1dB) after Vcont is switched low and high, respectively. TonDC is time required to reach stable quiescent bias (10%) after Vref is switched high.
6. ToffDC is time required for the current to be less than 10% of the Iq after Vref is switched low. TonRF is time required to reach final output power (±1 dB) after Vref is switched high. ToffRF is time required to output power to drop 30dB after Vref is switched low.

Characteristics Data (HSDPA, Control scheme: 3-mode control, Vcc = 3.4V, Vref = 2.85V, T = 25°C, Fo = 1880 MHz)

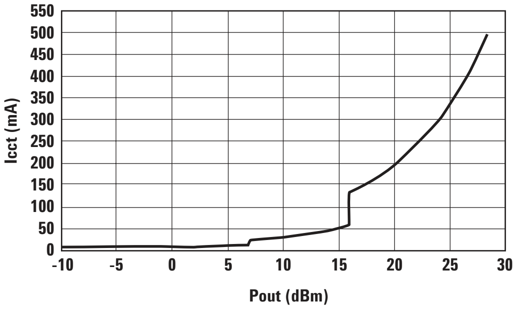


Figure 1. Total Current vs. Output Power.

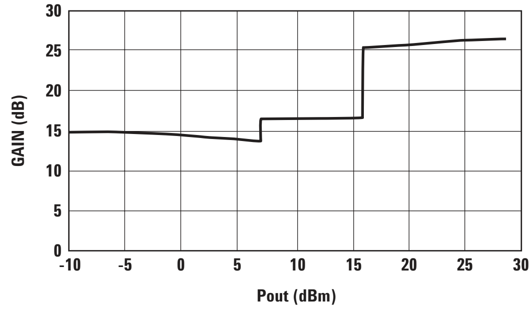


Figure 2. Gain vs. Output Power.

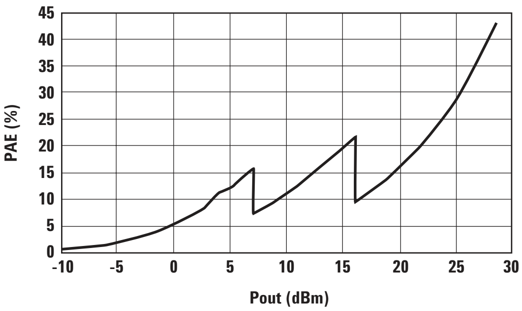


Figure 3. Power Added Efficiency vs. Output Power.

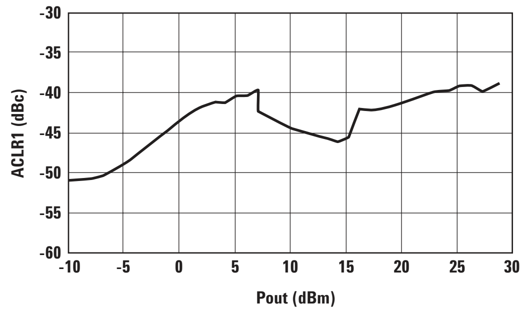


Figure 4. Adjacent Channel Leakage Ratio 1 vs. Output Power.

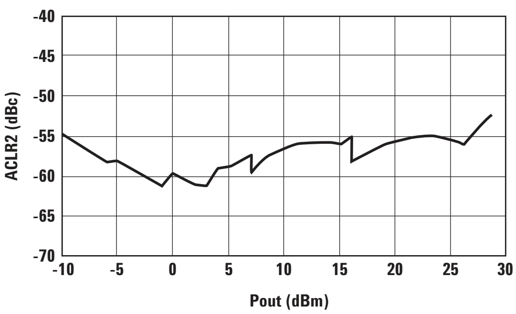


Figure 5. Adjacent Channel Leakage Ratio 2 vs. Output Power.

Characteristics Data (WCDMA, Control scheme: 3-mode control, Vcc = 3.4V, Vref = 2.85V, T = 25°C, Fo = 1880 MHz)

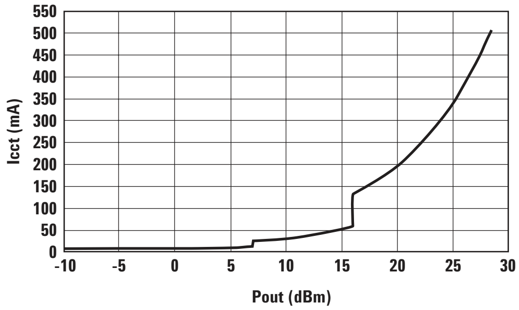


Figure 6. Total Current vs. Output Power.

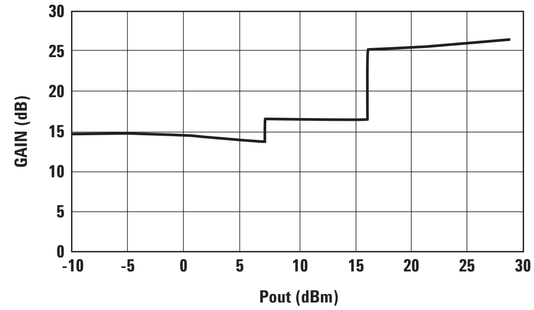


Figure 7. Gain vs. Output Power.

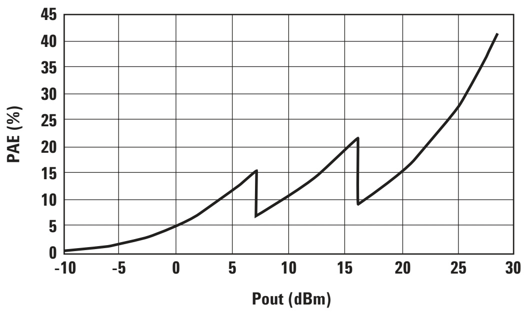


Figure 8. Power Added Efficiency vs. Output Power.

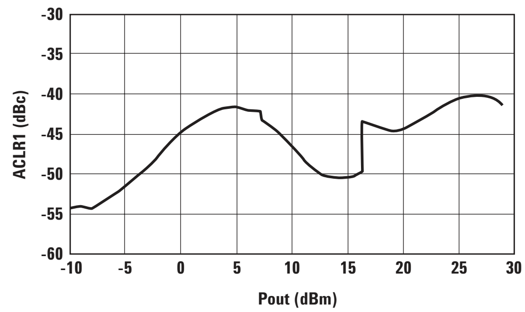


Figure 9. Adjacent Channel Leakage Ratio 1 vs. Output Power.

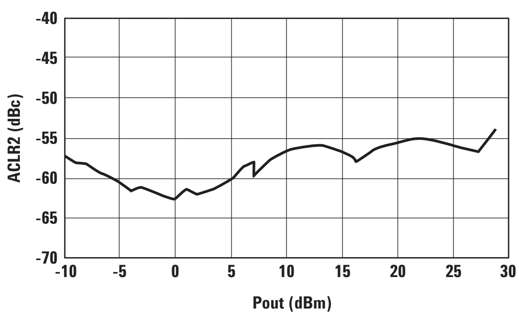


Figure 10. Adjacent Channel Leakage Ratio 2 vs. Output Power.

Characteristics Data (WCDMA, Control scheme: 2-mode control, Vcc = 3.4V, Vref = 2.85V, T = 25°C, Fo = 1880 MHz)

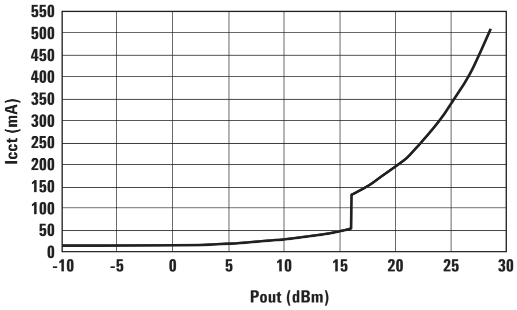


Figure 11. Total Current vs. Output Power.

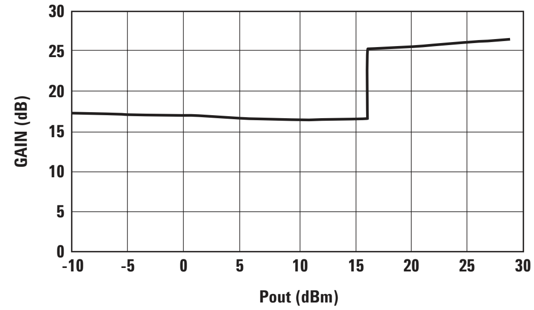


Figure 12. Gain vs. Output Power.

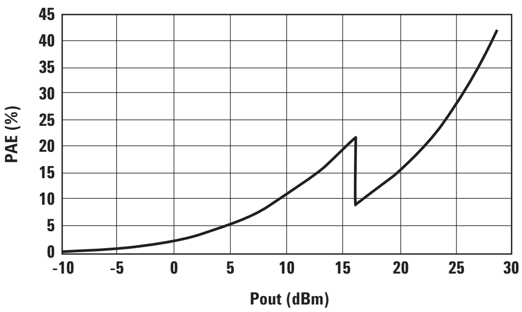


Figure 13. Power Added Efficiency vs. Output Power.

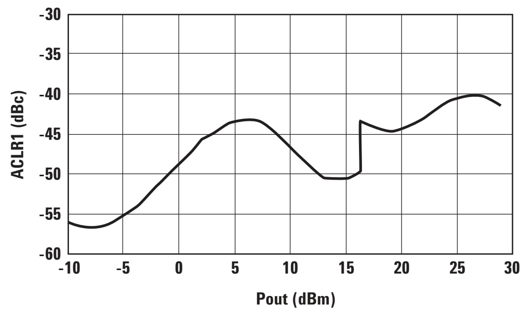


Figure 14. Adjacent Channel Leakage Ratio 1 vs. Output Power.

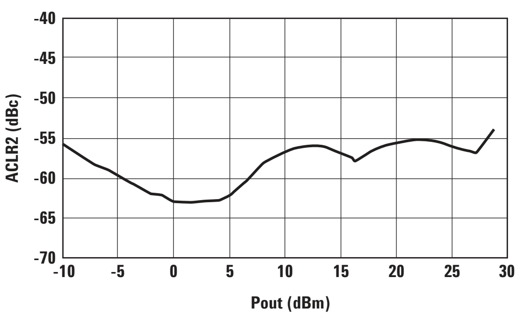


Figure 15. Adjacent Channel Leakage Ratio 2 vs. Output Power.

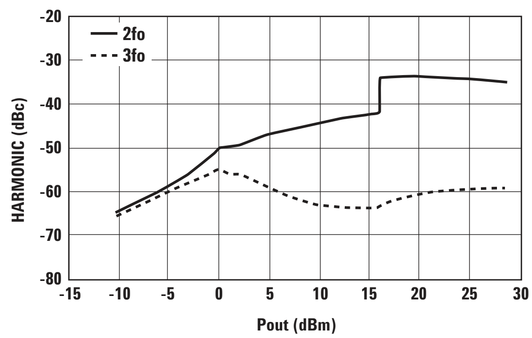


Figure 16. Harmonic Suppression 2 vs. Output Power.

Evaluation Board Description

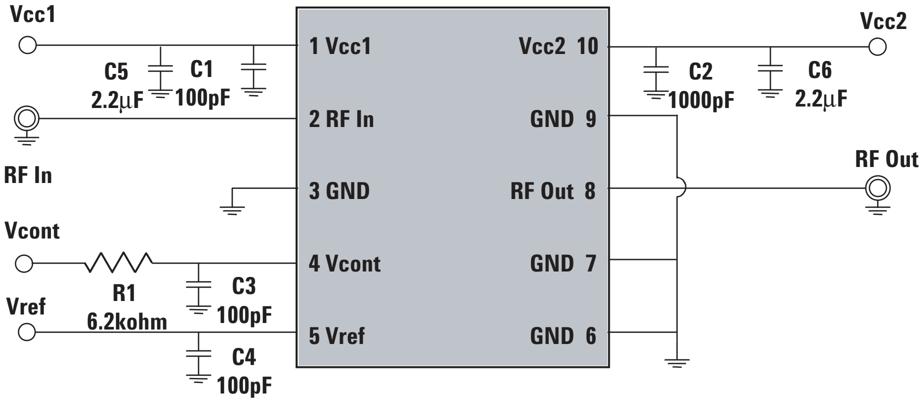


Figure 17. Evaluation Board Schematic.

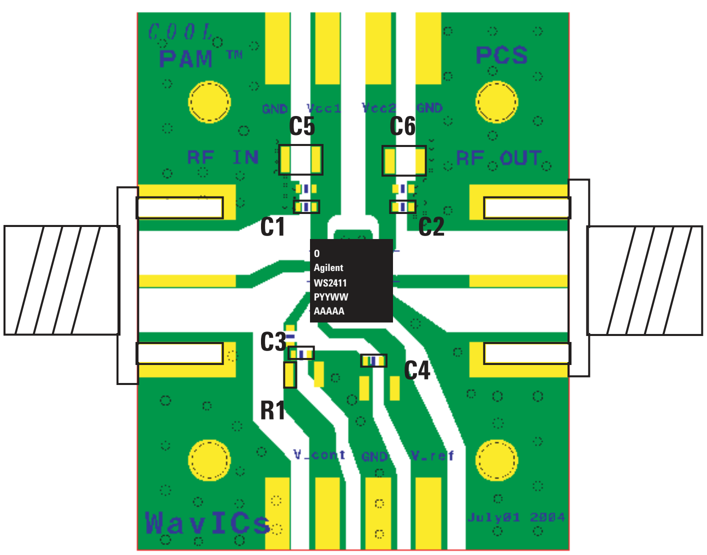
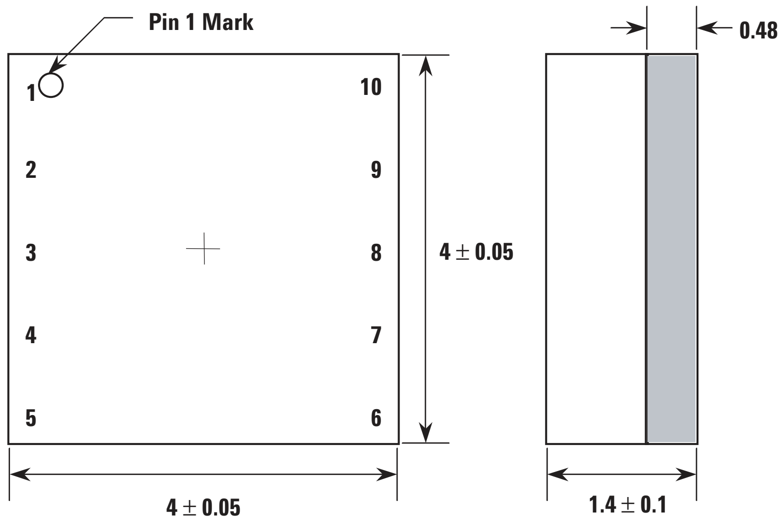
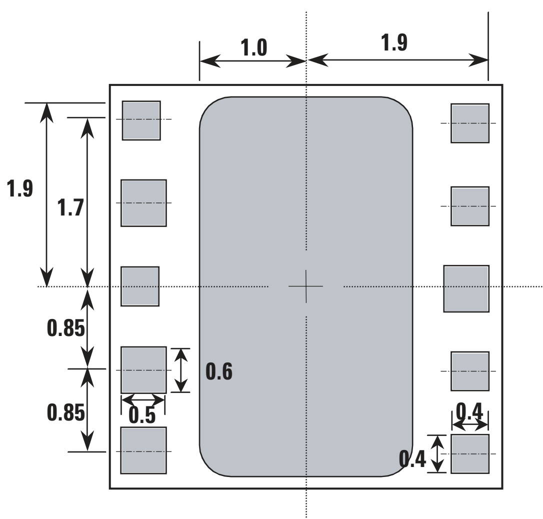


Figure 18. Evaluation Board Assembly Diagram.

Package Dimensions and Pin Descriptions





Pin #	Name	Description
1	Vcc1	Supply Voltage
2	RF In	RF Input
3	GND	Ground
4	Vcont	Control Voltage
5	Vref	Reference Voltage
6	GND	Ground
7	GND	Ground
8	RF Out	RF Output
9	GND	Ground
10	Vcc2	Supply Voltage

BOTTOM VIEW

PIN DESCRIPTIONS

all dimensions are in millimeters

Figure 19. Package Dimensional Drawing and Pin Descriptions.

Package Dimensions and Pin Descriptions, continued

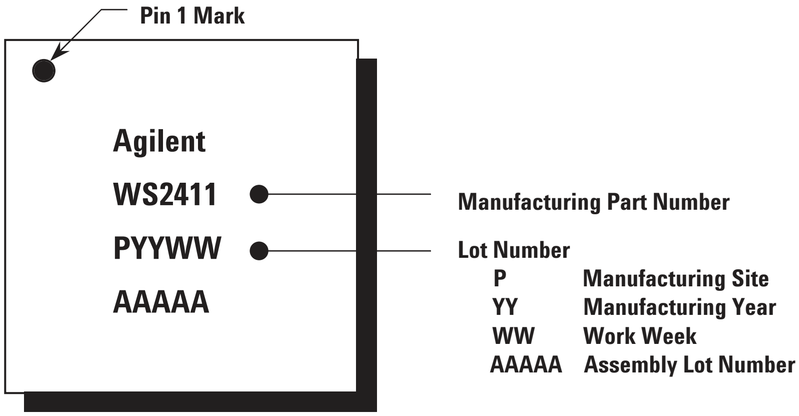


Figure 20. Marking Specification.

Peripheral Circuit in Handset

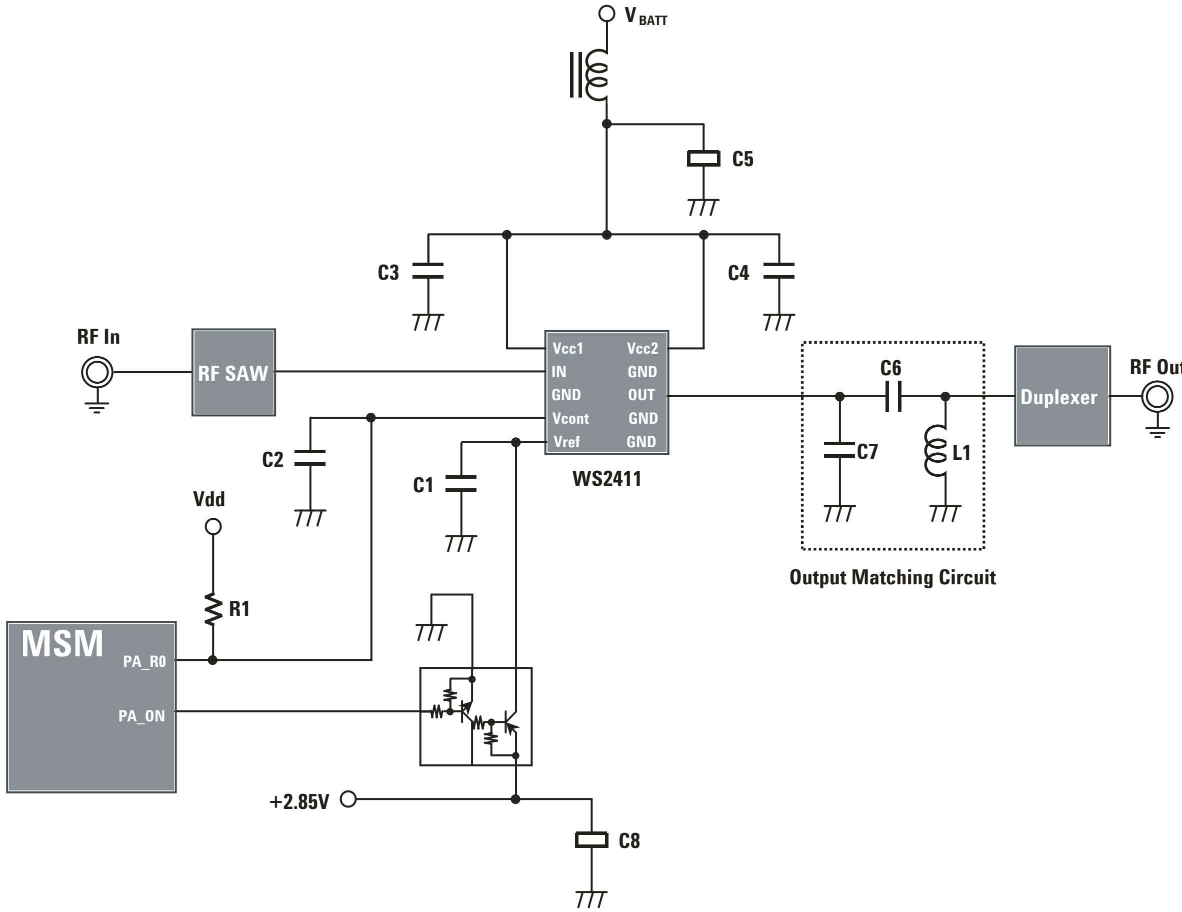


Figure 21. Peripheral Circuit.

Notes:

1. Recommended voltage for Vref is 2.85V.
2. Place C1 near to Vref pin.
3. Place C3 and C4 close to pin 1 (Vcc1) and pin 10 (Vcc2). These capacitors can affect the RF performance.
4. Use 50Ω transmission line between PAM and Duplexer and make it as short as possible to reduce conduction loss.
5. π-type circuit topology is good to use for matching circuit between PA and Duplexer,.
6. Pull-up resistor (R1) should be used to limit current drain. 6.2 kohm is recommended for WS2411.

Calibration

Calibration procedure is shown in Figure 22. CoolPAM requires two calibration tables for high mode and low mode respectively. This is due to gain difference in each mode.

For continuous output power at the points of mode change, the input power should be adjusted according to gain step during the mode change.

Offset value

(difference between rising point and falling point)

Offset value, which is the difference between the rising point (output power where PA mode changes from low mode to high mode) and falling point (output power where PA mode changes from high mode to low mode), should be set to prevent system oscillation. 3 to 5 dB is recommended for Hysteresis.

Average Current and Talk Time

Probability Distribution Function implies that what is important for longer talk time is the efficiency of low or medium power range rather than the efficiency at full power. WS2411 idle current is 13 mA and operating current at 16 dBm is 54 mA at nominal condition. Average current calculated with CDMA PDF is 29 mA in urban area and 56 mA in suburban area for 2-mode control. Average current can be reduced with 3-mode control, which results in 24 mA in urban area and 51mA in suburban area. This PA with low current consumption prolongs talk time by no less than 30 minutes compared to other PAs.

Average current = $\int (PDF \times Current)\,dp$

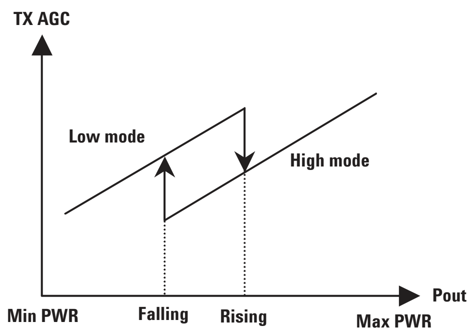


Figure 22. Calibration procedure.

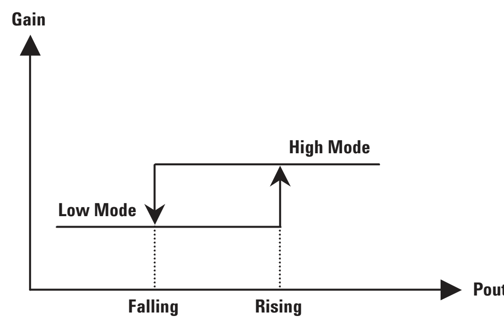


Figure 23. Setting of offset between rising and falling power.

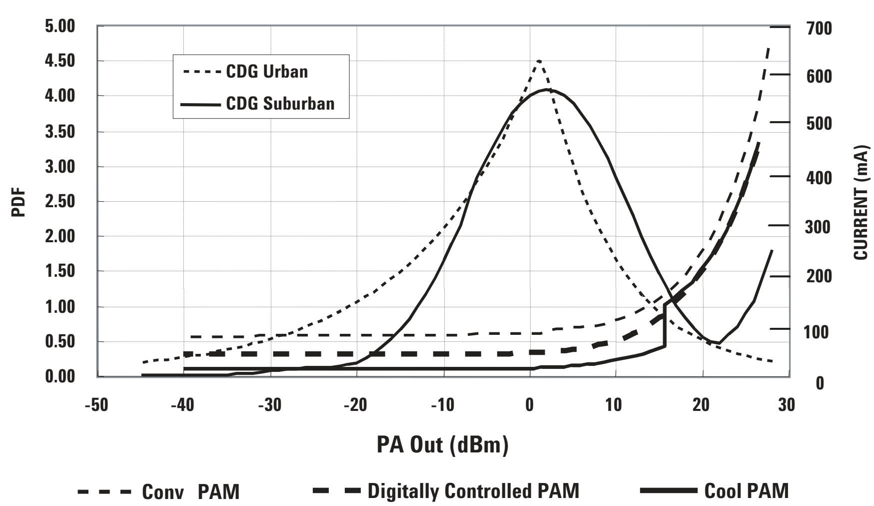


Figure 24. CDMA Power Distribution Function.

PCB Design Guidelines

The recommended WS2411 PCB Land pattern is shown in Figure 25 and Figure 26. The substrate is coated with solder mask between the I/O and conductive paddle to protect the gold pads from short circuit that is caused by solder bleeding/bridging.

Stencil Design Guidelines

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads.

The recommended stencil layout is shown in Figure 27. Reducing the stencil opening can potentially generate more voids. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads or conductive paddle to adjacent I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use laser cut stencil composed of 0.100 mm (4mils) or 0.127 mm (5mils) thick stainless steel which is capable of producing the required fine stencil outline.

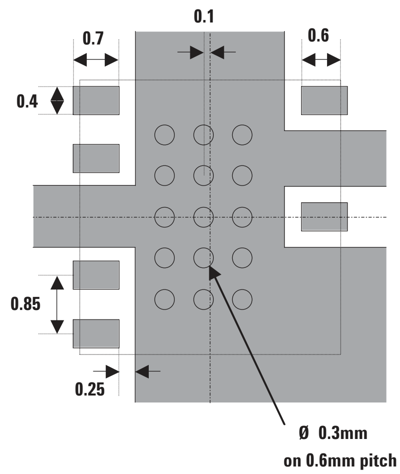


Figure 25. Metallization.

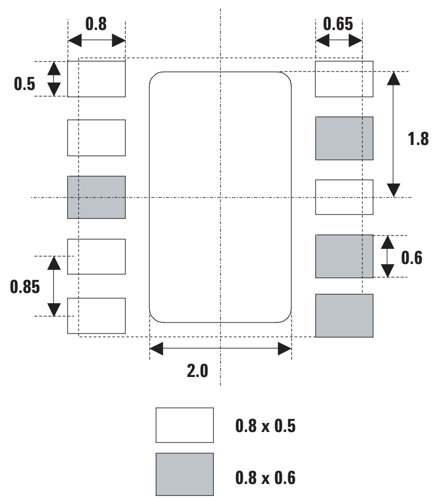


Figure 26. Solder Mask Opening.

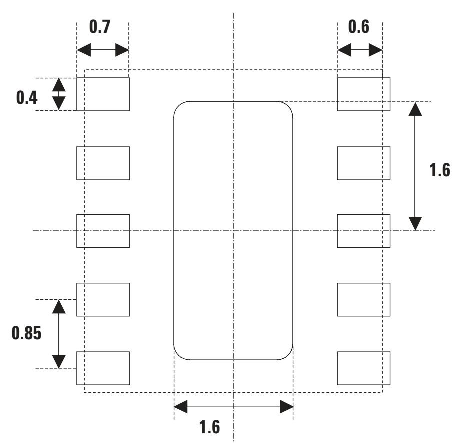


Figure 27. Solder Paste Stencil Aperature.

Power control scheme

- 2-mode control scheme

This control scheme doesn't require DC-DC converter. Vcont changes PA into Low Power Mode or High Power Mode, which results in 2-mode control without DC-DC converter. WS2411 is designed to change the mode at 16 dBm output power.

- 3-mode control scheme

This control scheme requires DC-DC converter. When DC-DC converter is used, Vcc voltage as well as Vcont can be changed, which results in 3-mode control scheme—Low/Mid/High power mode. Vcc changes at 7 dBm output and Vcont changes at 16 dBm output. Voltages for Vcc are 1.5V for low power mode and 3.4V (battery voltage) for mid and high power mode.

PAE graphs for 2-mode control and 3-mode control are shown in Figure 28 and Figure 29.

HSDPA

WS2411 meets stringent HSDPA linearity requirement up to 28.5 dBm. WS2411 can operate up to 28.5 dBm with Rel.99, which has a lower PAR (peak-to-average ratio) than HSDPA.

Table 5. Control scheme: 2-mode control

Power Mode	Vref	Vcont	Vcc	Power range
High Power Mode	2.85	Low	3.4	~28.5 dBm
Low Power Mode	2.85	High	3.4	~16 dBm
Shut Down Mode	0.00	–	3.4	–

Table 6. Control scheme: 3-mode control (DC-DC Converter Compatible)

Power Mode	Vref	Vcont	Vcc	Power range
High Power Mode	2.85	Low	3.4	~28.5 dBm
Middle Power Mode	2.85	High	3.4	~16 dBm
Low Power Mode	2.85	High	1.5	~7 dBm
Shut Down Mode	0.00	–	3.4	–

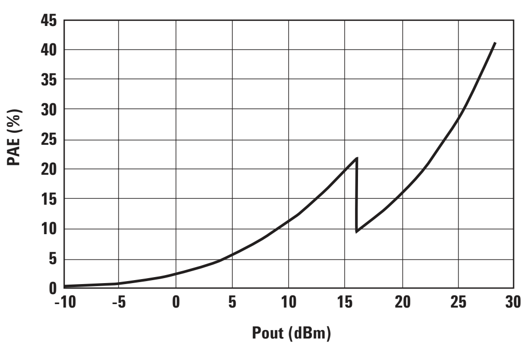


Figure 28. PAE (2-mode control).

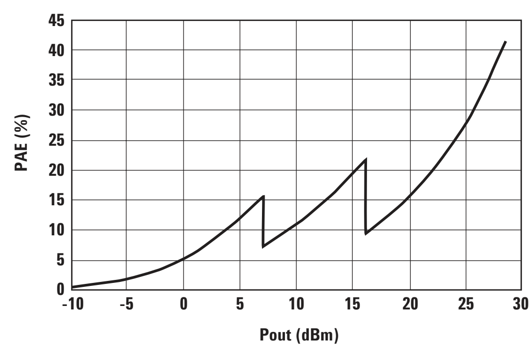
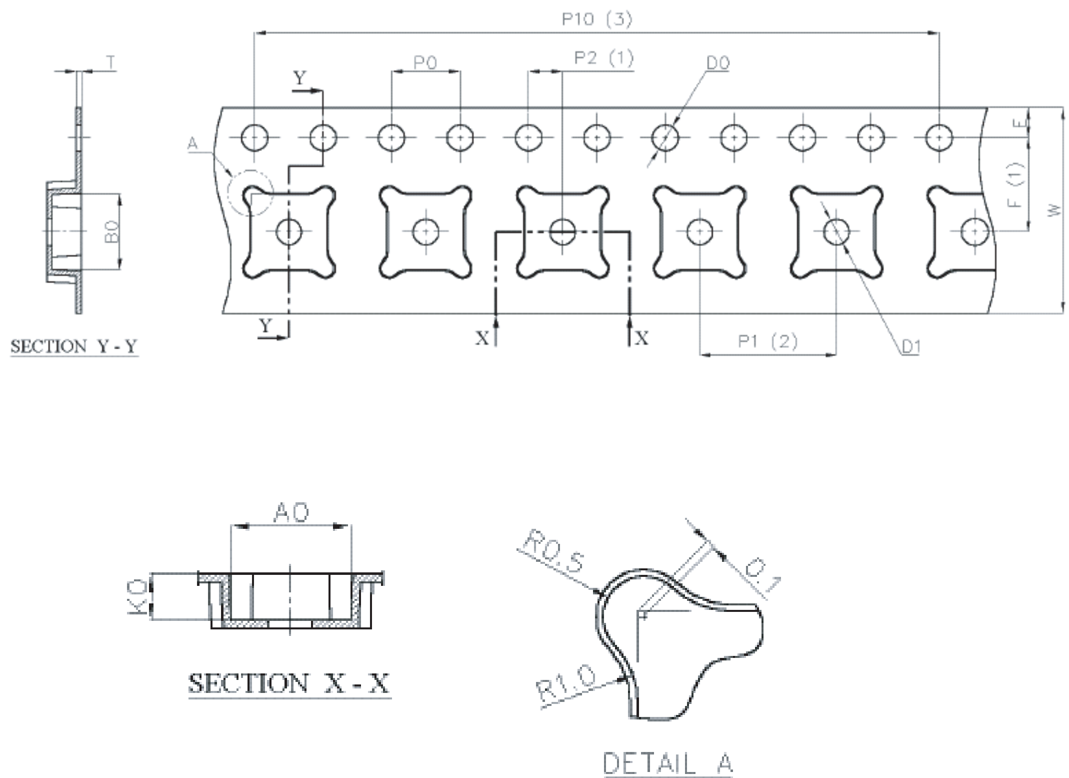


Figure 29. PAE (3-mode control).

Ordering Information

Part Number	Number of Devices	Container
WS2411-BLK	100	Bulk
WS2411-TR1	2500	13" Tape and Reel

Tape and Reel Information

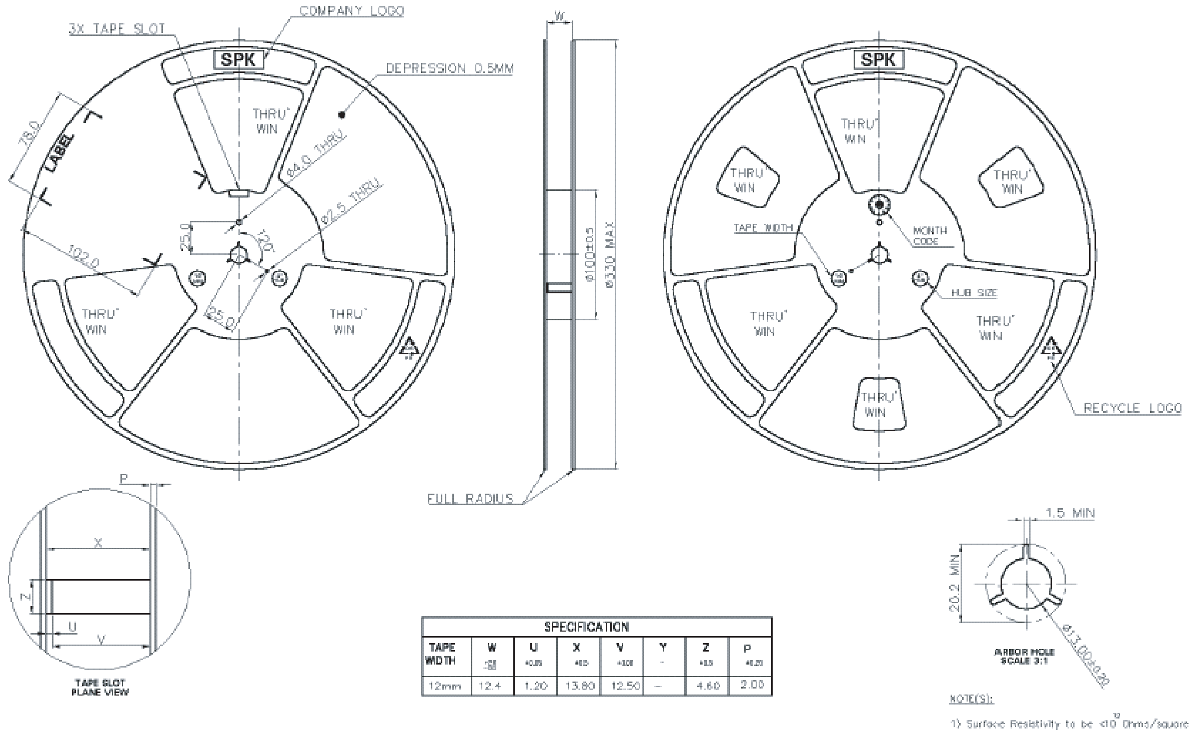


Dimension List

Annote	Millimeter
A0	4.40 ±0.10
B0	4.40 ±0.10
K0	1.70 ±0.10
D0	1.55 ±0.05
D1	1.60 ±0.10
P0	4.00 ±0.10
P1	8.00 ±0.10

Annote	Millimeter
P2	2.00 ±0.05
P10	40.00 ±0.20
E	1.75 ±0.10
F	5.50 ±0.05
W	12.00 ±0.30
T	0.30 ±0.05

Figure 30. Tape and Reel Format– 4 mm x 4 mm.



SPECIFICATION

TAPE WIDTH	W	U	X	V	Y	Z	P
12mm	12.4	1.20	13.80	12.50	–	4.60	2.00

all dimensions are in millimeters

Figure 31. Plastic Reel Format–13"/14".

Handling and Storage

ESD (Electrostatic Discharge)

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlet of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

MSL (Moisture Sensitivity Level)

Plastic encapsulated surface mount package is sensitive to damage induced by absorbed moisture and temperature. Agilent Technologies follows JEDEC Standard J-STD 020B. Each component and package type is classified for moisture sensitivity by soaking a known dry package at various temperatures and relative humidity, and times. After soak, the components are subjected to three consecutive simulated reflows.

The out of bag exposure time maximum limits are determined by the classification test described below which corresponds to a MSL classification level 6 to 1 according to the JEDEC standard IPC/JEDEC J-STD-020B and J-STD-033.

WS2411 is MSL3. Thus, according to the J-STD-033 p.11 the maximum Manufacturers Exposure Time (MET) for this part is 168 hours. After this time period, the part would need to be removed from the reel, de-taped and then re-baked.

MSL classification reflow temperature for the WS2411 is targeted at 250°C +0/-5°C. Figure 32 and Table 9 show typical SMT profile for maximum temperature of 250+0/-5°C.

Table 7. ESD Classification

Pin#	Name	Description	HBM	CDM	Classification
1	Vcc1	Supply Voltage	± 2000V	± 200V	Class 2
2	RF In	RF Input	± 2000V	± 200V	Class 2
3	GND	Ground	± 2000V	± 200V	Class 2
4	Vcont	Control Voltage	± 2000V	± 200V	Class 2
5	Vref	Reference Voltage	± 2000V	± 200V	Class 2
6	GND	Ground	± 2000V	± 200V	Class 2
7	GND	Ground	± 2000V	± 200V	Class 2
8	RFOut	RF Output	± 2000V	± 200V	Class 2
9	GND	Ground	± 2000V	± 200V	Class 2
10	Vcc2	Supply Voltage	± 2000V	± 200V	Class 2

Note:
1. Module products should be considered extremely ESD sensitive.

Table 8. Moisture Classification Level and Floor Life

MSL Level	Floor Life (out of bag) at factory ambient ≤ 30°C/60% RH or as stated
1	Unlimited at ≤ 30°C/85% RH
2	1 year
2a	4 weeks
3	**168 hours**
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

Note:
1. The MSL Level is marked on the MSL Label on each shipping bag.

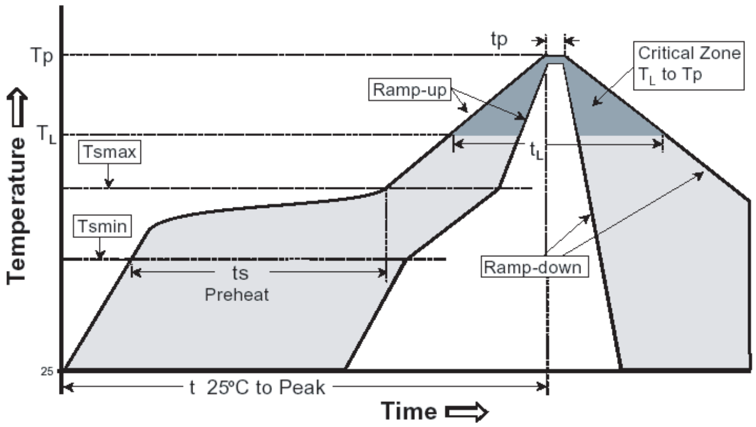


Figure 32. Typical SMT Reflow Profile for Maximum Temperature = 250+0/-5°C.

Table 9. Typical SMT Reflow Profile for Maximum Temperature = 250+0/-5°C

Profile Feature	Sn-Pb Solder	Pb-Free Solder
Average ramp-up rate (T_L to T_P)	3°C/sec max	3°C/sec max
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	 100°C 150°C 60–120 sec	 100°C 150°C 60–180 sec
Tsmax to T_L - Ramp-up Rate		 3°C/sec max
Time maintained above: - Temperature (T_L) - Time (T_L)	 183°C 60–150 sec	 217°C 60–150 sec
Peak Temperature (T_p)	225 +0/-5°C	250 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10–30 sec	10–30 sec
Ramp-down Rate	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 min max	8 min max

Storage Conditions

Packages described in this document must be stored in sealed moisture barrier, anti-static bags. Shelf life in a sealed moisture barrier bag is 12 months at <40°C and 90% relative humidity (RH) J-STD-033 p.7.

Out-of-Bag Time Duration
After unpacking the device must be soldered to the PCB within 168 hours as listed in the J-STD-020B p.11 with factory conditions <30°C and 60% RH.

Baking
It is not necessary to re-bake the part if both conditions (storage conditions and out-of-bag conditions) have been satisfied. Baking must be done if at least one of the conditions above have not been satisfied. The baking conditions are 125°C for 12 hours J-STD-033 p.8.

CAUTION: Tape and reel materials typically cannot be baked at the temperature described above. If out-of-bag exposure time is exceeded, parts must be baked for a longer time at low temperatures, or the parts must be de-reeled, de-taped, re-baked and then put back on tape and reel. (See moisture sensitive warning label on each shipping bag for information of baking).

Board Rework

Component Removal, Rework and Remount
If a component is to be removed from the board, it is recommended that localized heating be used and the maximum body temperatures of any surface mount component on the board not exceed 200°C. This method will minimize moisture related component damage. If any component temperature exceeds 200°C, the board must be baked dry per 4-2 prior to rework and/or component removal. Component temperatures **shall** be measured at the top center of the package body. Any SMD packages that have not exceeded their floor life can be exposed to a maximum body temperature as high as their specified maximum reflow temperature.

Removal for Failure Analysis
Not following the above requirements may cause moisture/reflow damage that could hinder or completely prevent the determination of the original failure mechanism.

Baking of Populated Boards
Some SMD packages and board materials are not able to withstand long duration bakes at 125°C. Examples of this are some FR-4 materials, which cannot withstand a 24 hr bake at 125°C. Batteries and electrolytic capacitors are also temperature sensitive. With component and board temperature restrictions in mind, choose a bake temperature from Table 4-1 in J-STD 033; then determine the appropriate bake duration based on the component to be removed. For additional considerations see IPC-7711 and IPC-7721.

Derating due to Factory Environmental Conditions

Factory floor life exposures for SMD packages removed from the dry bags will be a function of the ambient environmental conditions. A safe, yet conservative, handling approach is to expose the SMD packages only up to the maximum time limits for each moisture sensitivity level as shown in Table 8. This approach, however, does not work if the factory humidity or temperature are greater than the testing conditions of 30°C/60% RH. A solution for addressing this problem is to derate the exposure times based on the knowledge of moisture diffusion in the component packaging materials (ref. JESD22-A120). Recommended equivalent total floor life exposures can be estimated for a range of humidities and temperatures based on the nominal plastic thickness for each device. Table 10 lists equivalent derated floor lives for humidities ranging from 20–90% RH for three temperatures, 20°C, 25°C, and 30°C. This table is applicable to SMDs molded with novolac, biphenyl or multifunctional epoxy mold compounds. The following assumptions were used in calculating Table 10:

1. Activation Energy for diffusion = 0.35eV (smallest known value).
2. For ≤60% RH, use Diffusivity = 0.121exp (- 0.35eV/kT) mm2/s (this uses smallest known Diffusivity @ 30°C).
3. For >60% RH, use Diffusivity = 1.320exp (- 0.35eV/kT) mm2/s (this uses largest known Diffusivity @ 30°C).

Table 10. Recommended Equivalent Total Floor Life (days) @ 20°C, 25°C & 30°C For ICs with Novolac, Biphenyl and Multifunctional Epoxies (Reflow at same temperature at which the component was classified)

		Maximum Percent Relative Humidity										
Package Type and Body Thickness	Moisture Sensitivity Level	5%	10%	20%	30%	40%	50%	60%	70%	80%	90%	
Body Thickness ≥3.1 mm including PQFPs >84 pins, PLCCs (square) All MQFPs or All BGAs ≥1 mm	Level 2a	∞	∞	∞	60	41	33	28	10	7	6	30°C
		∞	∞	∞	78	53	42	36	14	10	8	25°C
		∞	∞	∞	103	69	57	47	19	13	10	20°C
	Level 3	∞	∞	10	9	8	7	7	5	4	4	30°C
		∞	∞	13	11	10	9	9	7	6	5	25°C
		∞	∞	17	14	13	12	12	10	8	7	20°C
	Level 4	∞	5	4	4	4	3	3	3	2	2	30°C
		∞	6	5	5	5	5	4	3	3	3	25°C
		∞	8	7	7	7	7	6	5	4	4	20°C
	Level 5	∞	4	3	3	2	2	2	2	1	1	30°C
		∞	5	5	4	4	3	3	2	2	2	25°C
		∞	7	7	6	5	5	4	3	3	3	20°C
	Level 5a	∞	2	1	1	1	1	1	1	1	1	30°C
		∞	3	2	2	2	2	2	1	1	1	25°C
		∞	5	4	3	3	3	2	2	2	2	20°C
Body 2.1 mm ≤ Thickness <3.1 mm including PLCCs (rectangular) 18-32 pins SOICs (wide body) SOICs ≥20 pins, PQFPs ≤80 pins	Level 2a	∞	∞	∞	∞	86	39	28	4	3	2	30°C
		∞	∞	∞	∞	148	51	37	6	4	3	25°C
		∞	∞	∞	∞	∞	69	49	8	5	4	20°C
	Level 3	∞	∞	19	12	9	8	7	3	2	2	30°C
		∞	∞	25	15	12	10	9	5	3	3	25°C
		∞	∞	32	19	15	13	12	7	5	4	20°C
	Level 4	∞	7	5	4	4	3	3	2	2	1	30°C
		∞	9	7	5	5	4	4	3	2	2	25°C
		∞	11	9	7	6	6	5	4	3	3	20°C
	Level 5	∞	4	3	3	2	2	2	1	1	1	30°C
		∞	5	4	3	3	3	3	2	1	1	25°C
		∞	6	5	5	4	4	4	3	3	2	20°C
	Level 5a	∞	2	1	1	1	1	1	1	0.5	0.5	30°C
		∞	2	2	2	2	2	2	1	1	1	25°C
		∞	3	2	2	2	2	2	2	2	1	20°C
Body Thickness <2.1 mm including SOICs <18 pins All TQFPs, TSOPs or all BGAs <1 mm body thickness	Level 2a	∞	∞	∞	∞	∞	∞	28	1	1	1	30°C
		∞	∞	∞	∞	∞	∞	∞	2	1	1	25°C
		∞	∞	∞	∞	∞	∞	∞	2	2	1	20°C
	Level 3	∞	∞	∞	∞	∞	11	7	1	1	1	30°C
		∞	∞	∞	∞	∞	14	10	2	1	1	25°C
		∞	∞	∞	∞	∞	20	13	2	2	1	20°C
	Level 4	∞	∞	∞	9	5	4	3	1	1	1	30°C
		∞	∞	∞	12	7	5	4	2	1	1	25°C
		∞	∞	∞	17	9	7	6	2	2	1	20°C
	Level 5	∞	∞	13	5	3	2	2	1	1	1	30°C
		∞	∞	18	6	4	3	3	2	1	1	25°C
		∞	∞	26	8	6	5	4	2	2	1	20°C
	Level 5a	∞	10	3	2	1	1	1	1	1	0.5	30°C
		∞	13	5	3	2	2	2	1	1	1	25°C
		∞	18	6	4	3	2	2	2	2	1	20°C

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