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# FDMS86183

## N-Channel Shielded Gate PowerTrench® MOSFET

100 V, 51 A, 12.8 mΩ

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 12.8 mΩ at  $V_{GS} = 10$  V,  $I_D = 16$  A
- Max  $r_{DS(on)}$  = 34.6 mΩ at  $V_{GS} = 6$  V,  $I_D = 8$  A
- 50% Lower  $Q_{rr}$  than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

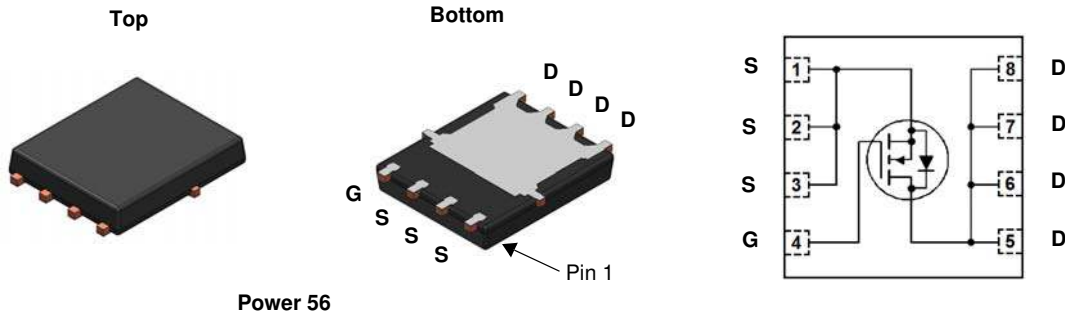


### General Description

This N-Channel MV MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

### Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous	$T_C = 25$ °C (Note 5)	51
	-Continuous	$T_C = 100$ °C (Note 5)	32
	-Continuous	$T_A = 25$ °C (Note 1a)	10
	-Pulsed	(Note 4)	187
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	96
$P_D$	Power Dissipation	$T_C = 25$ °C	63
	Power Dissipation	$T_A = 25$ °C (Note 1a)	2.5
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86183	FDMS86183	Power 56	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		63		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 90\text{ }\mu\text{A}$	2.0	3.2	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 90\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-9		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 16\text{ A}$		9.9	12.8	m $\Omega$
		$V_{GS} = 6\text{ V}$ , $I_D = 8\text{ A}$		17	34.6	
		$V_{GS} = 10\text{ V}$ , $I_D = 16\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		16.6	21.5	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 16\text{ A}$		20		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		1080	1515	pF
$C_{oss}$	Output Capacitance			646	905	pF
$C_{rss}$	Reverse Transfer Capacitance			10	15	pF
$R_g$	Gate Resistance		0.1	0.5	1.5	$\Omega$

### Switching Characteristics

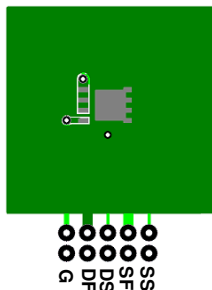
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}$ , $I_D = 16\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		11	20	ns	
$t_r$	Rise Time			3	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			15	27	ns	
$t_f$	Fall Time			3	10	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		15	21	nC
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }6\text{ V}$		10	14	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 50\text{ V}$ , $I_D = 16\text{ A}$		5		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge			3.4		nC	
$Q_{oss}$	Output Charge		$V_{DD} = 50\text{ V}$ , $V_{GS} = 0\text{ V}$		43		nC

### Drain-Source Diode Characteristics

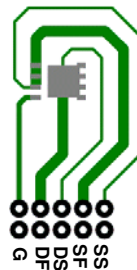
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.1\text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 16\text{ A}$ (Note 2)		0.9	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 8\text{ A}$ , $di/dt = 300\text{ A}/\mu\text{s}$		22	36	ns
$Q_{rr}$	Reverse Recovery Charge			36	58	nC
$t_{rr}$	Reverse Recovery Time	$I_F = 8\text{ A}$ , $di/dt = 1000\text{ A}/\mu\text{s}$		18	33	ns
$Q_{rr}$	Reverse Recovery Charge			79	127	nC

#### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a)  $50\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $125\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

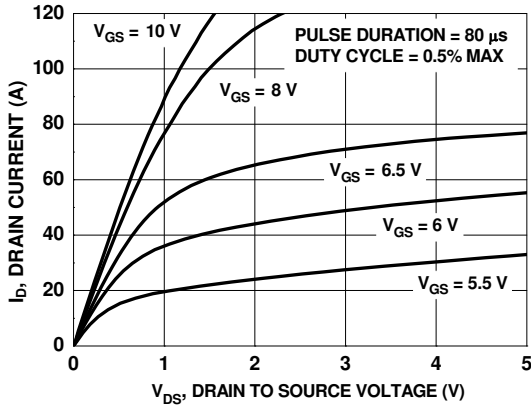
2. Pulse Test: Pulse Width  $< 300\text{ }\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3.  $E_{AS}$  of  $96\text{ mJ}$  is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ; N-ch:  $L = 3\text{ mH}$ ,  $I_{AS} = 8\text{ A}$ ,  $V_{DD} = 100\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.3\text{ mH}$ ,  $I_{AS} = 18\text{ A}$ .

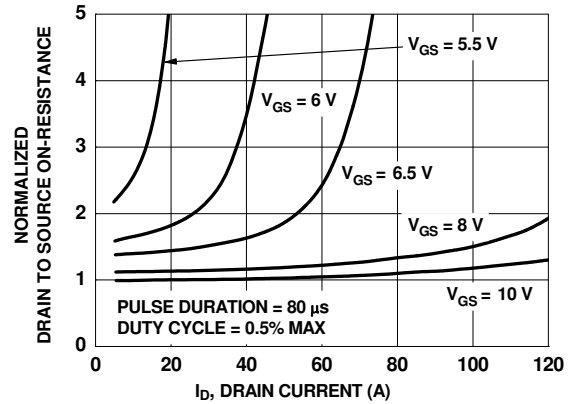
4. Pulsed  $I_d$  please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

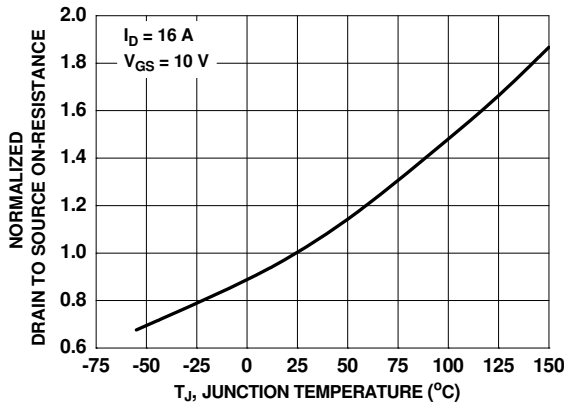
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



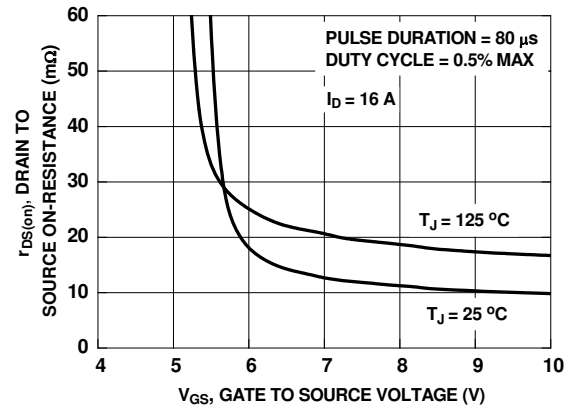
**Figure 1. On-Region Characteristics**



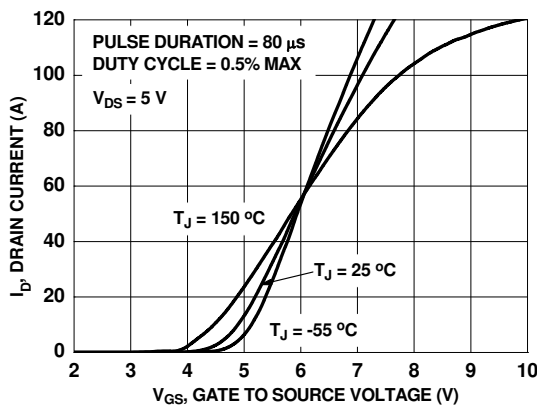
**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**



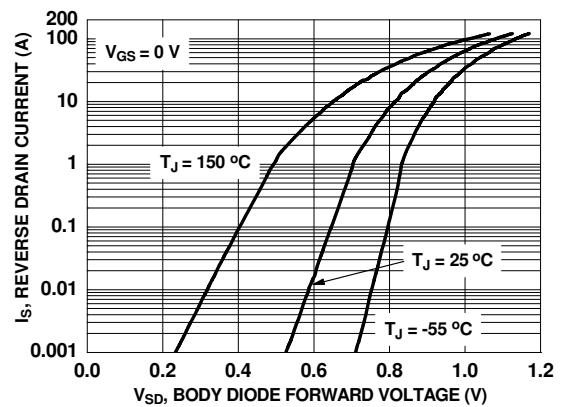
**Figure 3. Normalized On-Resistance vs. Junction Temperature**



**Figure 4. On-Resistance vs. Gate to Source Voltage**

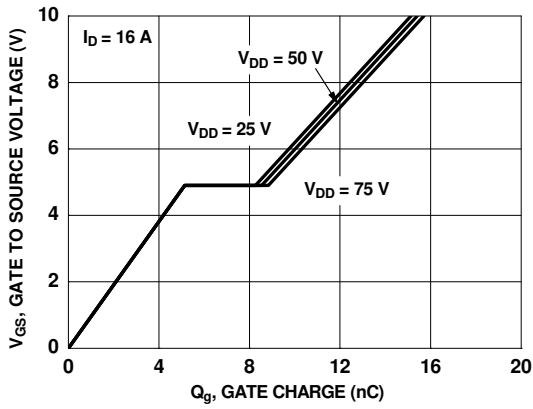


**Figure 5. Transfer Characteristics**

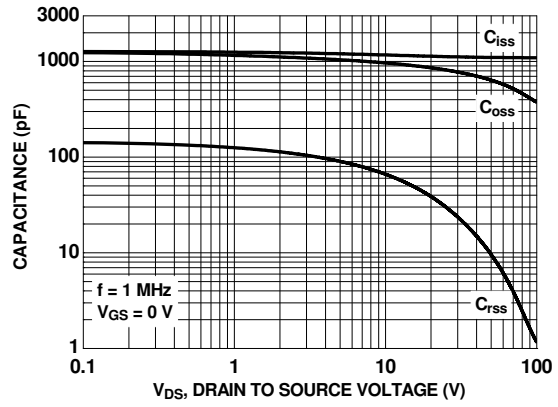


**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

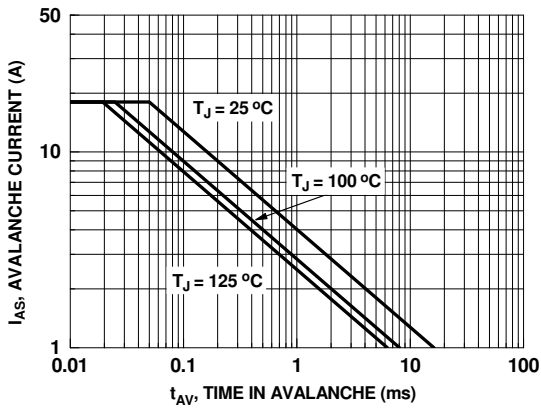
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



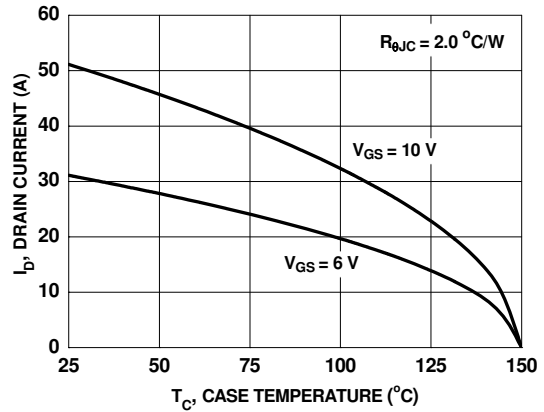
**Figure 7. Gate Charge Characteristics**



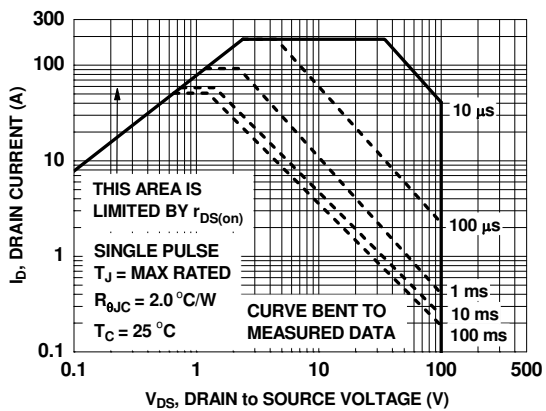
**Figure 8. Capacitance vs. Drain to Source Voltage**



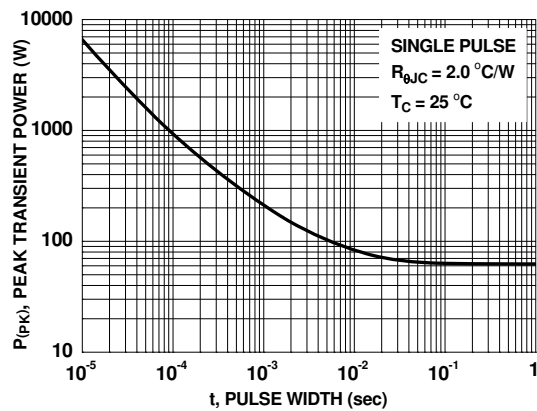
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

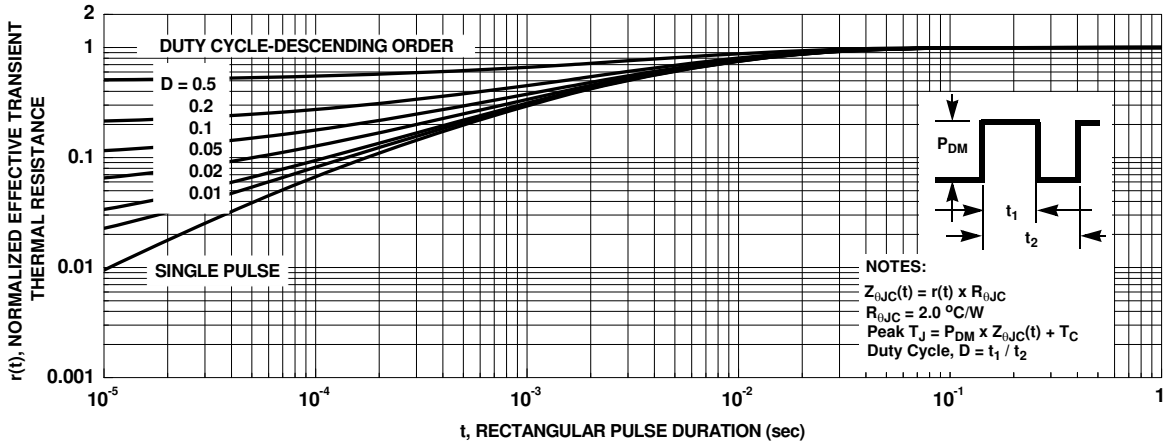


**Figure 11. Forward Bias Safe Operating Area**

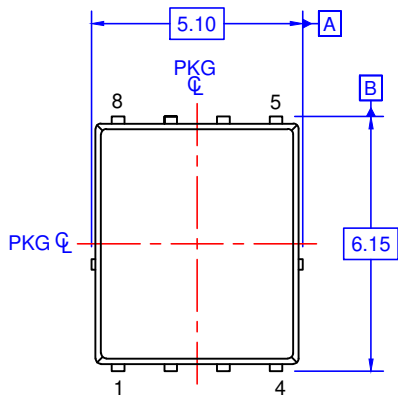


**Figure 12. Single Pulse Maximum Power Dissipation**

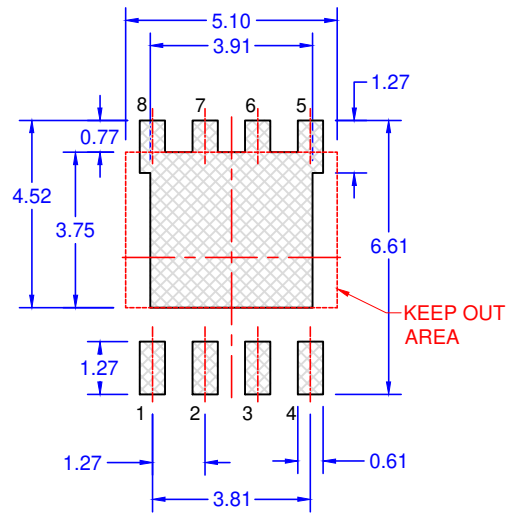
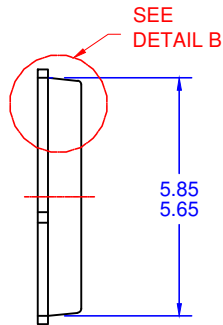
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



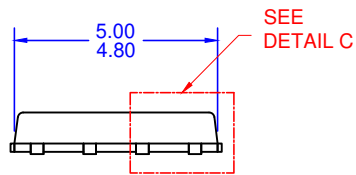
PQFN8 5X6, 1.27P  
CASE 483AE  
ISSUE A



TOP VIEW

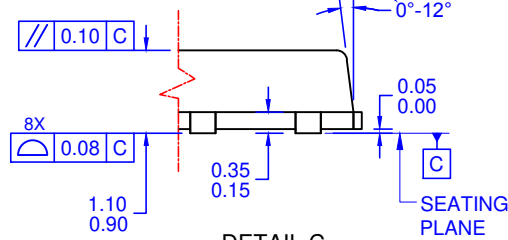


LAND PATTERN RECOMMENDATION

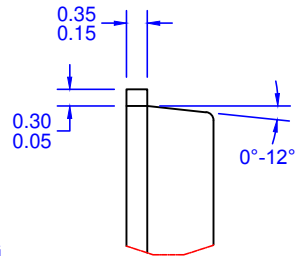


SIDE VIEW

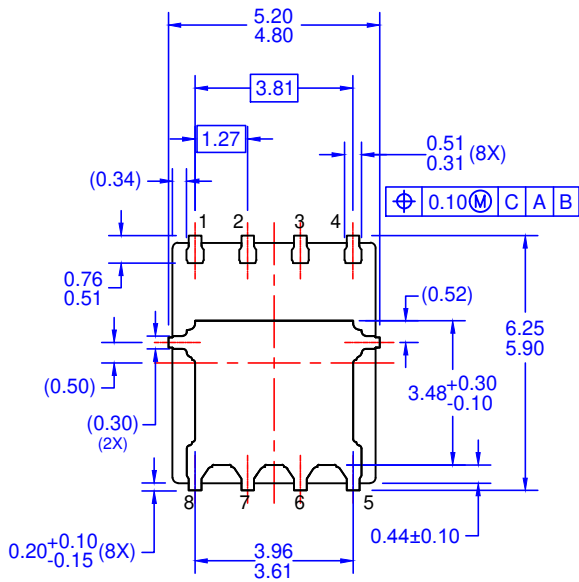
OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C  
SCALE: 2:1



DETAIL B  
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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