

Mobile Pentium II™ System Clock Chip

Recommended Application:

The ICS9248-92 is a fully compliant timing solution for the Intel mobile 440BX/MX chipset requirements.

General Description:

Features include two strong CPU, seven PCI and eight SDRAM clocks. Three reference outputs are available equal to the crystal frequency. Stronger drive CPUCLK outputs typically provide greater than 1 V/ns slew rate into 20pF loads. This device meets rise and fall requirements with 2 loads per CPU output (ie, one clock to CPU and NB chipset, one clock to two L2 cache inputs).

PWR_DWN# pin allows low power mode by stopping crystal OSC and PLL stages. For optional power management, CPU_STOP# can stop CPU (0:1) clocks and PCI_STOP# will stop PCICLK (0:5) clocks

PCICLK outputs typically provide better than 1V/ns slew rate into 30pF loads while maintaining 50±5% duty cycle. The REF clock outputs typically provide better than 0.5V/ns slew rates.

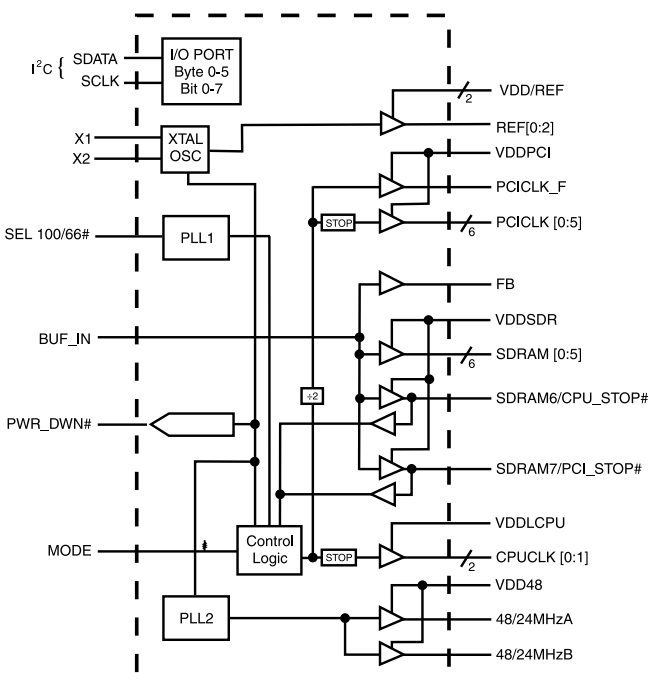
The ICS9248-92 accepts a 14.318MHz reference crystal or clock as its input and runs on a 3.3V core supply.

Features

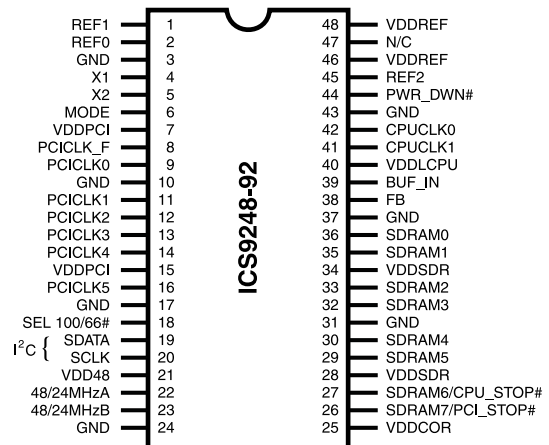
- Generates system clocks for CPU, SDRAM, PCI, plus 14.318 MHz REF(0:2), USB, Plus Super I/O
- I²C serial configuration interface provides output clock disabling and other functions
- MODE input pin selects optional power management input control pins
- Two fixed outputs separately selectable as 24 or 48MHz
- 2.5V outputs: CPU
- 3.3V outputs: SDRAM, PCI, REF, 48/24 MHz
- No power supply sequence requirements
- Uses external 14.318MHz crystal
- 48 pin 240 mil TSSOP package
- Output enable register

for serial port control:
1 = enable
0 = disable

Block Diagram



Pin Configuration



48-Pin TSSOP 240 mil Package

Functionality

Crystal (X1, X2) = 14.31818 MHz

| SEL 100/66# | CPUCLK (MHz) | PCICLK (MHz) |
|-------------|--------------|--------------|
| 0 | 66.6 | 33.3 |
| 1 | 100 | 33.3 |

Pentium is a trademark on Intel Corporation.



Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|------------------------------|--------------|------|--|
| 45, 1, 2 | REF [2:0] | OUT | Reference clock Output |
| 3, 10, 17, 24, 31, 37, 43 | GND | PWR | Ground (common) |
| 4 | X1 | IN | Crystal or reference input, has internal crystal load cap |
| 5 | X2 | OUT | Crystal output, has internal load cap and feedback resistor to X1 |
| 6 | MODE | IN | Input function selection (see table page 3) |
| 7, 15 | VDDPCI | PWR | Supply for PCICLK_F, PCICLK [0:5], nominal 3.3V |
| 8 | PCICLK_F | OUT | Free running PCI clock, not affected by PCI_STOP# |
| 9, 11, 12, 13, 14, 16 | PCICLK [0:5] | OUT | PCI clocks |
| 18 | SEL100/66# | IN | Selects 66.6MHz or 100MHz for SDRAM and CPU (see tables page 1, 3) |
| 19 | SDATA | IN | I ² C data input |
| 20 | SCLK | IN | I ² C clock input |
| 21 | VDD48 | PWR | Supply for 48/24MHzA, 48/24MHzB, nominal 3.3V |
| 22 | 48/24MHzA | OUT | 48/24MHz driver output for USB or Super I/O |
| 23 | 48/24MHzB | OUT | 48/24MHz driver output for USB or Super I/O |
| 25 | VDDCOR | PWR | Supply for PLL core, nominal 3.3V |
| 26 | SDRAM7 | OUT | SDRAM clock output, fanout buffer output from BUF_IN pin |
| | PCI_STOP# | IN | Halts PCI Bus [0:5] at logic "0" level when low |
| 27 | SDRAM6 | OUT | SDRAM clock output, fanout buffer output from BUF_IN pin |
| | CPU_STOP# | IN | Halts CPU clocks at logic "0" level when low |
| 28, 34 | VDDSDR | PWR | Supply for SDRAM [0:5], SDRAM6/CPU_STOP#, SDRAM7/PCI_STOP#, nominal 3.3V |
| 40 | VDDLCPU | PWR | Supply for CPUCLK [0:1] 2.5V nominal |
| 42, 41 | CPUCLK [0:1] | OUT | CPUCLK clock output, powered by VDDL2 |
| 36, 35, 33, 32, 30, 29 | SDRAM [0:5] | OUT | SDRAM clock outputs, fanout buffer outputs from BUF_IN pin |
| 38 | FB | OUT | Feedback out |
| 39 | BUF_IN | IN | Input for SDRAM buffers |
| 44 | PWR_DWN# | IN | When driven active (low) powers down the device into low power state. Internal clocks are disabled, VCO and crystal OSC are stopped. |
| 48, 46 | VDDREF | PWR | Supply for REF [0:2], X1, X2, nominal 3.3V |

Power Groups

VDDCOR = Supply for PLL core

VDDREF = REF [0:2], X1, X2

VDDPCI = PCICLK_F, PCICLK [0:5]

VDDSDR = SDRAM [0:7]

VDD48 = 48/24MHzA, 48/24MHz

VDDLCPU = CPUCLK [0:1]



Power-On Conditions

| SEL 100/66.6# | MODE | PIN # | DESCRIPTION | FUNCTION |
|------------------|------|-----------------------------|-------------|---|
| 1 | 1 | 41, 42 | CPUCLKs | 100 MHz - w/serial config enable/disable |
| | | 16, 14, 13, 12, 11, 9, 8 | PCICLKs | 33.3 MHz - w/serial config enable/disable |
| 0 | 1 | 41, 42 | CPUCLKs | 66.6 MHz - w/serial config enable/disable |
| | | 16, 14, 13, 12, 11, 9, 8 | PCICLKs | 33.3 MHz - w/serial config enable/disable |
| 1 | 0 | 26 | PCI_STOP# | Power Management, PCI [0:5] Clocks Stopped when low |
| | | 27 | CPU_STOP# | Power Management, CPU [0:5] Clocks Stopped when low |
| | | 8 | PCICLK_F | 33.3 MHz - PCI Clock Free running |
| | | 41, 42 | CPUCLKs | 100 MHz - CPU Clocks w/external Stop Control and serial config individual enable/disable. |
| | | 16, 14, 13, 12, 11, 9 | PCICLKs | 33.3 MHz - PCI Clocks w/external Stop control and serial config individual enable/disable. |
| 0 | 0 | 26 | PCI_STOP# | Power Management, PCI [0:5] Clocks Stopped when low |
| | | 27 | CPU_STOP# | Power Management, CPU [0:5] Clocks Stopped when low |
| | | 8 | PCICLK_F | 33.3 MHz - PCI Clock Free running for Power Management |
| | | 41, 42 | CPUCLKs | 66.6 MHz - CPU Clocks w/external Stop control and serial config individual enable/disable. |
| | | 16, 14, 13, 12, 11, 9 | PCICLKs | 33.3 MHz - PCI Clocks w/external Stop control and serial config individual enable/disable. |

Example:

- a) if MODE = 1, pins 26 and 27 are configured as SDRAM7 and SDRAM6 respectively.
- b) if MODE = 0, pins 26 and 27 are configured as PCI_STOP# and CPU_STOP# respectively.

Power-On Default Conditions

At power-up and before device programming, all clocks will default to an enabled and “on” condition. The frequencies that are then produced are on the MODE pin as shown in the table below.

| CLOCK | DEFAULT CONDITION AT POWER-UP |
|-----------|-------------------------------|
| REF (0:2) | 14.31818 MHz |
| 48/24 MHz | 48 MHz |



General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte **one at a time**.
- Controller (host) sends a Stop bit

| How to Write: | |
|------------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D2 _(H) | |
| | ACK |
| Dummy Command Code | |
| | ACK |
| Dummy Byte Count | |
| | ACK |
| Byte 0 | |
| | ACK |
| Byte 1 | |
| | ACK |
| Byte 2 | |
| | ACK |
| Byte 3 | |
| | ACK |
| Byte 4 | |
| | ACK |
| Byte 5 | |
| | ACK |
| Stop Bit | |

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 5**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

| How to Read: | |
|------------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D3 _(H) | |
| | ACK |
| | Byte Count |
| ACK | |
| | Byte 0 |
| ACK | |
| | Byte 1 |
| ACK | |
| | Byte 2 |
| ACK | |
| | Byte 3 |
| ACK | |
| | Byte 4 |
| ACK | |
| | Byte 5 |
| ACK | |
| Stop Bit | |

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



Serial Configuration Command Bitmaps

Byte 0: Functional and Frequency Select Clock Register (default on Bits 7, 6, 5, 4, 1, 0 = 0)

Note: PWD=Power-Up Default (default on Bits 3, 2 = 1)

| BIT | PIN# | DESCRIPTION | PWD | | | | | | | | | | | | | | | |
|----------------|------|---|------|------|--|---|---|-----------|---|---|------------------------|---|---|----------|---|---|------------------|----|
| Bit 7 | - | Reserved | 0 | | | | | | | | | | | | | | | |
| Bit 6 | - | Reserved | 0 | | | | | | | | | | | | | | | |
| Bit 5 | - | In Spread Spectrum, Controls type (0=centered, 1=down spread) | 1 | | | | | | | | | | | | | | | |
| Bit 4 | - | In Spread Spectrum, Controls Spreading (0= $\pm 0.5\%$ 1= $\pm 0.25\%$) | 0 | | | | | | | | | | | | | | | |
| Bit 3 | 23 | 48/24 MHz (Frequency Select) 1=48 MHz, 0=24 MHz | 1 | | | | | | | | | | | | | | | |
| Bit 2 | 22 | 48/24 MHz (Frequency Select) 1=48 MHz, 0=24 MHz | 1 | | | | | | | | | | | | | | | |
| Bit 1 Bit 0 | - | <table border="0"> <tr> <td>Bit1</td> <td>Bit0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Tri-State</td> </tr> <tr> <td>1</td> <td>0</td> <td>Spread Spectrum Enable</td> </tr> <tr> <td>0</td> <td>1</td> <td>Testmode</td> </tr> <tr> <td>0</td> <td>0</td> <td>Normal operation</td> </tr> </table> | Bit1 | Bit0 | | 1 | 1 | Tri-State | 1 | 0 | Spread Spectrum Enable | 0 | 1 | Testmode | 0 | 0 | Normal operation | 10 |
| Bit1 | Bit0 | | | | | | | | | | | | | | | | | |
| 1 | 1 | Tri-State | | | | | | | | | | | | | | | | |
| 1 | 0 | Spread Spectrum Enable | | | | | | | | | | | | | | | | |
| 0 | 1 | Testmode | | | | | | | | | | | | | | | | |
| 0 | 0 | Normal operation | | | | | | | | | | | | | | | | |

Select Functions

| Functionality | CPU | PCI, PCI_F | SDRAM | REF | 24 MHz Selection | 48 MHz Selection |
|---------------|---------------------|---------------------|---------------------|-------------------|---------------------|---------------------|
| Tristate | HI - Z | HI - Z | HI - Z | HI - Z | HI - Z | HI - Z |
| Testmode | TCLK/2 ¹ | TCLK/4 ¹ | TCLK/2 ¹ | TCLK ¹ | TCLK/4 ¹ | TCLK/2 ¹ |

Notes:

1. TCLK is a test clock driven on the X1 (crystal in pin) input during test mode.



Byte 1: CPU, 24/48 MHz Clock Register

| BIT | PIN# | PWD | DESCRIPTION |
|-------|------|-----|-----------------------|
| Bit 7 | 23 | 1 | 48/24 MHz (Act/Inact) |
| Bit 6 | 22 | 1 | 48/24 MHz (Act/Inact) |
| Bit 5 | - | 1 | Reserved |
| Bit 4 | - | 1 | Reserved |
| Bit 3 | - | 1 | Reserved |
| Bit 2 | - | 1 | Reserved |
| Bit 1 | 41 | 1 | CPUCLK1 (Act/Inact) |
| Bit 0 | 42 | 1 | CPUCLK0 (Act/Inact) |

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 2: PCICLK Clock Register

| BIT | PIN# | PWD | DESCRIPTION |
|-------|------|-----|----------------------|
| Bit 7 | - | 1 | Reserved |
| Bit 6 | 8 | 1 | PCICLK_F (Act/Inact) |
| Bit 5 | 16 | 1 | PCICLK5 (Act/Inact) |
| Bit 4 | 14 | 1 | PCICLK4 (Act/Inact) |
| Bit 3 | 13 | 1 | PCICLK3 (Act/Inact) |
| Bit 2 | 12 | 1 | PCICLK2 (Act/Inact) |
| Bit 1 | 11 | 1 | PCICLK1 (Act/Inact) |
| Bit 0 | 9 | 1 | PCICLK0 (Act/Inact) |

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 3: SDRAM Clock Register

| BIT | PIN# | PWD | DESCRIPTION |
|-------|------|-----|--------------------|
| Bit 7 | 26 | 1 | SDRAM7 (Act/Inact) |
| Bit 6 | 27 | 1 | SDRAM6 (Act/Inact) |
| Bit 5 | 29 | 1 | SDRAM5 (Act/Inact) |
| Bit 4 | 30 | 1 | SDRAM4 (Act/Inact) |
| Bit 3 | 32 | 1 | SDRAM3 (Act/Inact) |
| Bit 2 | 33 | 1 | SDRAM2 (Act/Inact) |
| Bit 1 | 35 | 1 | SDRAM1 (Act/Inact) |
| Bit 0 | 36 | 1 | SDRAM0 (Act/Inact) |

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 4: SDRAM Clock Register

| BIT | PIN# | PWD | DESCRIPTION |
|-------|------|-----|-------------|
| Bit 7 | - | 1 | Reserved |
| Bit 6 | - | 1 | Reserved |
| Bit 5 | - | 1 | Reserved |
| Bit 4 | - | 1 | Reserved |
| Bit 3 | - | 1 | Reserved |
| Bit 2 | - | 1 | Reserved |
| Bit 1 | - | 1 | Reserved |
| Bit 0 | - | 1 | Reserved |

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 5: Peripheral Clock Register

| BIT | PIN# | PWD | DESCRIPTION |
|-------|------|-----|------------------|
| Bit 7 | - | 1 | Reserved |
| Bit 6 | - | 1 | Reserved |
| Bit 5 | - | 1 | Reserved |
| Bit 4 | - | 1 | Reserved |
| Bit 3 | - | 1 | Reserved |
| Bit 2 | 45 | 1 | REF2 (Act/Inact) |
| Bit 1 | 1 | 1 | REF1 (Act/Inact) |
| Bit 0 | 2 | 1 | REF0 (Act/Inact) |

Notes: 1 = Enabled; 0 = Disabled, outputs held low
PWD = Power-Up Default

Byte 6: Optional Register for Future

| BIT | PIN# | PWD | DESCRIPTION |
|-------|------|-----|-------------|
| Bit 7 | - | 1 | Reserved |
| Bit 6 | - | 1 | Reserved |
| Bit 5 | - | 1 | Reserved |
| Bit 4 | - | 1 | Reserved |
| Bit 3 | - | 1 | Reserved |
| Bit 2 | - | 1 | Reserved |
| Bit 1 | - | 1 | Reserved |
| Bit 0 | - | 1 | Reserved |

Notes:
1. Byte 6 is reserved by Integrated Circuit Systems for future applications.

Note: PWD = Power-Up Default



Power Management

Clock Enable Configuration

| CPU_STOP# | PCI_STOP# | PWR_DWN# | CPUCLK | PCICLK | Other Clocks, SDRAM, REF, 48/24 MHz A 48/24 MHz B | Crystal | VCOs |
|-----------|-----------|----------|--------------|----------|---|---------|---------|
| X | X | 0 | Low | Low | Stopped | Off | Off |
| 0 | 0 | 1 | Low | Low | Running | Running | Running |
| 0 | 1 | 1 | Low | 33.3 MHz | Running | Running | Running |
| 1 | 0 | 1 | 100/66.6 MHz | Low | Running | Running | Running |
| 1 | 1 | 1 | 100/66.6 MHz | 33.3 MHz | Running | Running | Running |

Full clock cycle timing is guaranteed at all times after the system has initially powered up except where noted. During power up and power down operations using the PWR PD# select pin will not cause clocks of a short or longer pulse than that of the running clock. The first clock pulse coming out of a stopped clock condition may be slightly distorted due to clock network charging circuitry. Board routing and signal loading may have a large impact on the initial clock distortion also.

ICS9248-92 Power Management Requirements

| SIGNAL | SIGNAL STATE | Latency No. of rising edges of free running PCICLK |
|-----------|-----------------------------------|--|
| CPU_STOP# | 0 (Disabled) ² | 1 |
| | 1 (Enabled) ¹ | 1 |
| PCI_STOP# | 0 (Disabled) ² | 1 |
| | 1 (Enabled) ¹ | 1 |
| PWR_DWN# | 1 (Normal Operation) ³ | 3mS |
| | 0 (Power Down) ⁴ | 2max |

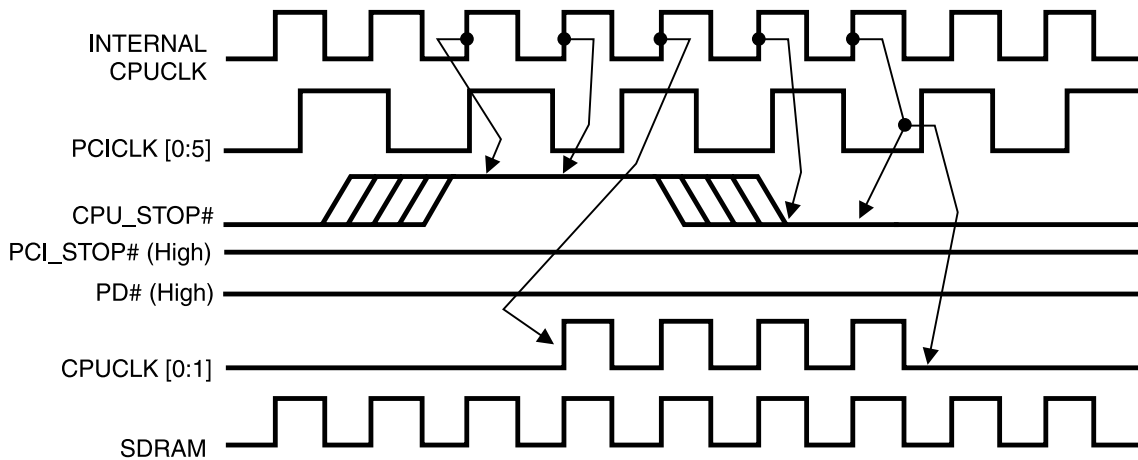
Notes.

1. Clock on latency is defined from when the clock enable goes active to when the first valid clock comes out of the device.
2. Clock off latency is defined from when the clock enable goes inactive to when the last clock is driven low out of the device.
3. Power up latency is when PD# goes inactive (high) to when the first valid clocks are output by the device.
4. Power down has controlled clock counts applicable to CPUCLK, SDRAM, PCICLK only.
The REF will be stopped independent of these.



CPU_STOP# Timing Diagram

CPUSTOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the ICS9248-92. The minimum that the CPUCLK is enabled (CPU_STOP# high pulse) is 100 CPUCLKs. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.



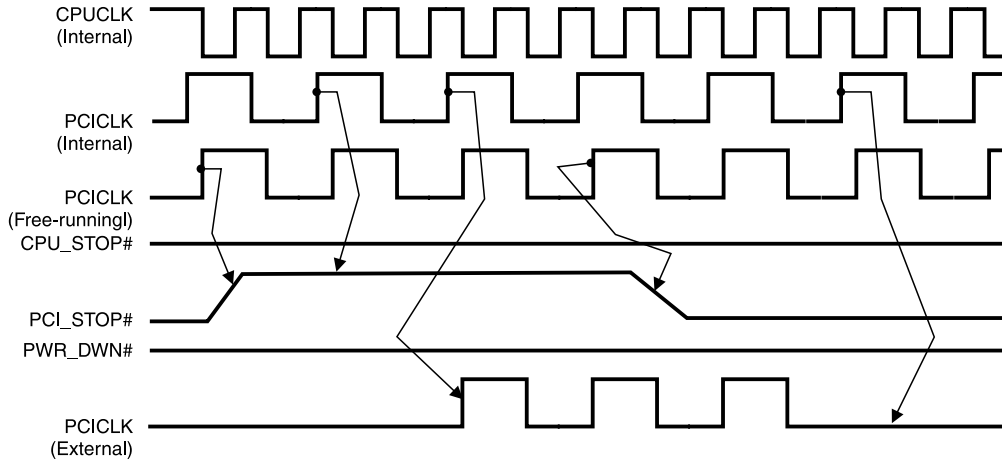
Notes:

- 1. All timing is referenced to the internal CPUCLK.
- 2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the ICS9248-92.
- 3. All other clocks continue to run undisturbed.
- 4. PD# and PCI_STOP# are shown in a high (true) state.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the ICS9248-92. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the ICS9248-92 internally. The minimum that the PCICLK (0:5) clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK (0:5) clocks. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.

(Drawing shown on next page.)

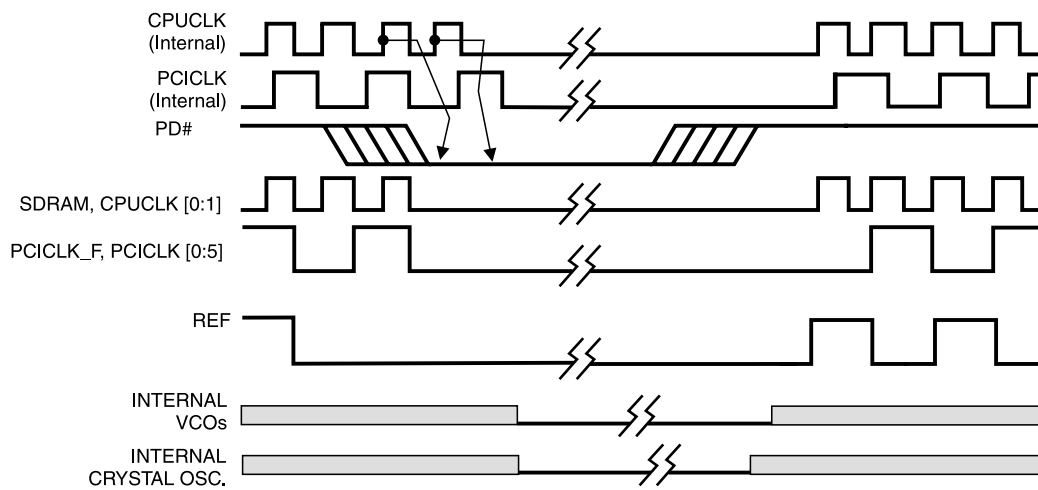


Notes:

- 1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
- 2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248.
- 3. All other clocks continue to run undisturbed.
- 4. PD# and CPU_STOP# are shown in a high (true) state.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal is synchronized internal by the ICS9248-92 prior to its control action of powering down the clock synthesizer. Internal clocks will not be running after the device is put in power down state. When PD# is active (low) all clocks are driven to a low state and held prior to turning off the VCOs and the Crystal oscillator. The power on latency is guaranteed to be less than 3mS. The power down latency is less than three CPUCLK cycles. PCI_STOP# and CPU_STOP# are don't care signals during the power down operations.



Notes:

- 1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
- 2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the ICS9248.
- 3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.



Absolute Maximum Ratings

| | |
|-------------------------------------|-------------------------------------|
| Supply Voltage | 5.5 V |
| Logic Inputs | GND-0.5 V to V _{DD} +0.5 V |
| Ambient Operating Temperature | 0°C to +70°C |
| Case Temperature | 115°C |
| Storage Temperature | -65°C to +150°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5% V_{DDL} = 2.5V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|----------------------|---|----------------------|--------|----------------------|-------|
| Input High Voltage | V _{IH} | | 2 | | V _{DD} +0.3 | V |
| Input Low Voltage | V _{IL} | | V _{SS} -0.3 | | 0.8 | V |
| Supply Current | I _{DD} | C _L = 0 pF; Select @ 66M | | 77 | 180 | mA |
| | I _{DDL2.5} | | | 2.8 | 25 | mA |
| Input frequency | F _i | V _{DD} = 3.3 V; | | 14.318 | | MHz |
| Input Capacitance ¹ | C _{IN} | Logic Inputs | | | 5 | pF |
| | C _{INX} | X1 & X2 pins | 27 | 36 | 45 | ps |
| Transition Time ¹ | T _{trans} | To 1st crossing of target Freq. | | 1.5 | 3 | ms |
| Clk Stabilization ¹ | T _{STAB} | From V _{DD} = 3.3 V to 1% target Freq. | | | 3 | ms |
| Skew ¹ | T _{CPU-PCI} | V _{TPCI} = 1.5 V; V _{TCPU} = 1.25 V | 1.5 | 2.2 | 4.0 | ns |

¹Guarenteed by design, not 100% tested in production.



Electrical Characteristics - CPUCLK

$T_A = 0 - 70^\circ \text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$, $V_{DDL} = 2.5 \text{ V} \pm 5\%$; $C_L = 20 \text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|-----------------|---|-----|------|------|-------|
| Period | period(norm) | $V_T = 1.25 \text{ V}$; 100MHz | 10 | 10 | 10.5 | ns |
| Output High Voltage | V_{OH2B} | $I_{OH} = -12.0 \text{ mA}$ | 1.8 | 2.3 | | V |
| Output Low Voltage | V_{OL2B} | $I_{OL} = 12 \text{ mA}$ | | 0.31 | 0.4 | V |
| Output High Current | I_{OH2B} | $V_{OH} = 1.7 \text{ V}$ | | | -27 | mA |
| Output Low Current | I_{OL2B} | $V_{OL} = 0.7 \text{ V}$ | 27 | | | mA |
| Rise Time | t_{r2B}^1 | $V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.0 \text{ V}$ | | | 1.6 | ns |
| Fall Time | t_{f2B}^1 | $V_{OH} = 2.0 \text{ V}$, $V_{OL} = 0.4 \text{ V}$ | | 1 | 1.6 | ns |
| Duty Cycle | d_{t2B}^1 | $V_T = 1.25 \text{ V}$ | 45 | 50 | 55 | % |
| Skew | t_{sk2B}^1 | $V_T = 1.25 \text{ V}$ | | 30 | 95 | ps |
| Jitter | $t_{cyc-cyc}^1$ | $V_T = 1.25 \text{ V}$ | | 186 | 250 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, 48MHz,24MHz

$T_A = 0 - 70^\circ \text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$, $V_{DDL} = 2.5 \text{ V} \pm 5\%$; $C_L = 20 \text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------|-------------|---|-----|------|-----|-------|
| Output High Voltage | V_{OH5} | $I_{OH} = -14 \text{ mA}$ | 2 | 3.21 | | V |
| Output Low Voltage | V_{OL5} | $I_{OL} = 6.0 \text{ mA}$ | | 0.21 | 0.4 | V |
| Output High Current | I_{OH5} | $V_{OH} = 2.0 \text{ V}$ | | | -23 | mA |
| Output Low Current | I_{OL5} | $V_{OL} = 0.8 \text{ V}$ | 29 | | | mA |
| Rise Time ¹ | t_{r5} | $V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$ | 1 | 2.5 | 4 | ns |
| Fall Time ¹ | t_{f5} | $V_{OH} = 2.4 \text{ V}$, $V_{OL} = 0.4 \text{ V}$ | 1 | 2.5 | 4 | ns |
| Duty Cycle ¹ | d_{t5} | $V_T = 1.5 \text{ V}$ | 45 | 52 | 55 | % |
| Jitter, Absolute ¹ | t_{jabs5} | $V_T = 1.5 \text{ V}$, REF | | 385 | 800 | ps |
| Jitter, Absolute ¹ | t_{jabs5} | $V_T = 1.5 \text{ V}$, 48 MHz | | 469 | 800 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - PCICLK

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 30\text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|-----------------|---|------|------|-----|-------|
| Output High Voltage | V_{OH1} | $I_{OH} = -18\text{ mA}$ | 2.1 | 3.3 | | V |
| Output Low Voltage | V_{OL1} | $I_{OL} = 9.4\text{ mA}$ | | 0.17 | 0.4 | V |
| Output High Current | I_{OH1} | $V_{OH} = 2.0\text{ V}$ | | | -24 | mA |
| Output Low Current | I_{OL1} | $V_{OL} = 0.8\text{ V}$ | 30 | | | mA |
| Rise Time ¹ | t_{r1} | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$ | 0.5 | 1.6 | 2 | ns |
| Fall Time ¹ | t_{f1} | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$ | 0.5 | 1.8 | 2 | ns |
| Duty Cycle ¹ | d_{t1} | $V_T = 1.5\text{ V}$ | 45 | 50 | 55 | % |
| Skew ¹ | t_{sk1} | $V_T = 1.5\text{ V}$ | | 222 | 500 | ps |
| Jitter, Absolute ¹ | t_{jabs1} | $V_T = 1.5\text{ V}$ | -250 | | 250 | ps |
| Jitter, Cycle-to-cycle ¹ | $t_{jeyc-eyc1}$ | $V_T = 1.5\text{ V}$ | | 227 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 30\text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-----------|---|-----|------|-----|-------|
| Output High Voltage | V_{OH1} | $I_{OH} = -28\text{ mA}$ | 2.2 | 3.18 | | V |
| Output Low Voltage | V_{OL1} | $I_{OL} = 19\text{ mA}$ | | 0.35 | 0.4 | V |
| Output High Current | I_{OH1} | $V_{OH} = 2.0\text{ V}$ | | -74 | -46 | mA |
| Output Low Current | I_{OL1} | $V_{OL} = 0.8\text{ V}$ | 54 | | | mA |
| Rise Time ¹ | t_{r1} | $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.4\text{ V}$ | 0.5 | 1.54 | 1.6 | ns |
| Fall Time ¹ | t_{f1} | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$ | 0.5 | 1.51 | 1.6 | ns |
| Duty Cycle ¹ | d_{t1} | $V_T = 1.5\text{ V}$ | 45 | 51 | 55 | % |
| Skew ¹ | t_{sk1} | $V_T = 1.5\text{ V}$ | | 200 | 250 | ps |
| Propagation Delay ¹ | t_{p1} | $V_T = 1.5\text{ V}$ | 1 | 3.5 | 5 | ns |

¹Guaranteed by design, not 100% tested in production.



General Layout Precautions:

- 1) Use a ground plane on the top routing layer of the PCB in all areas not used by traces.
- 2) Make all power traces and ground traces as wide as the via pad for lower inductance.

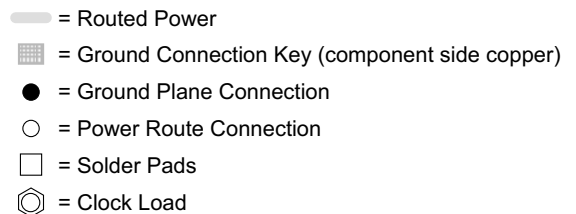
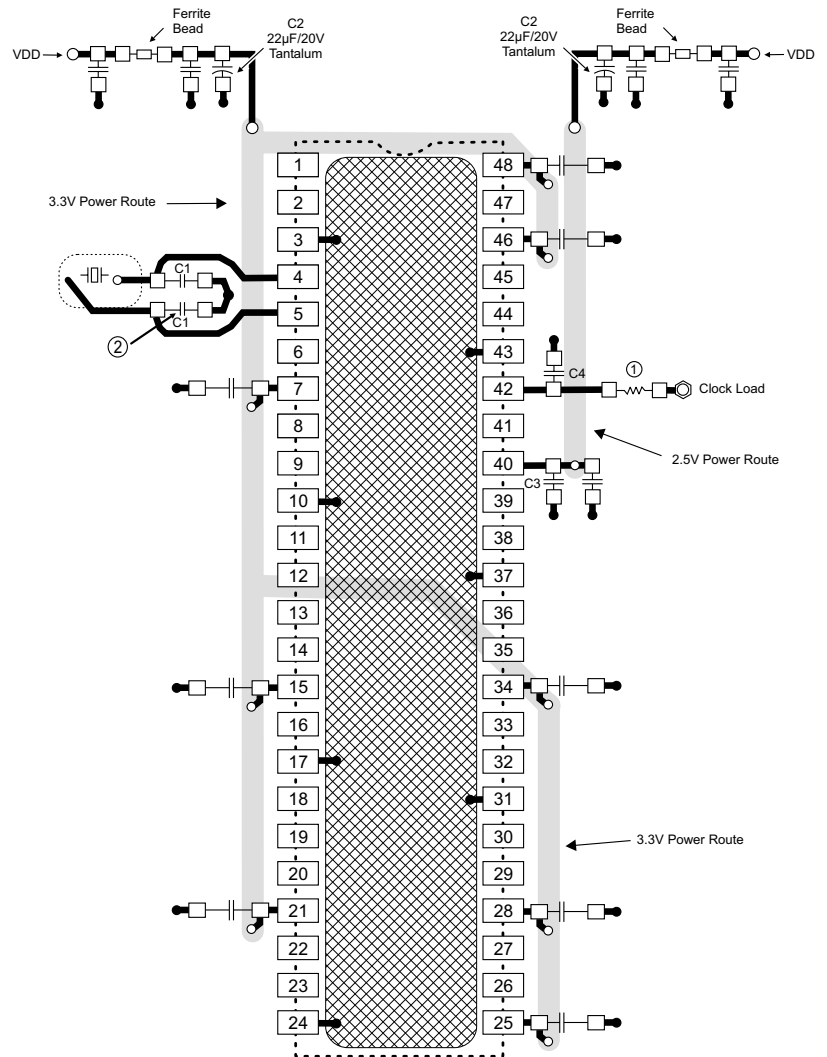
Notes:

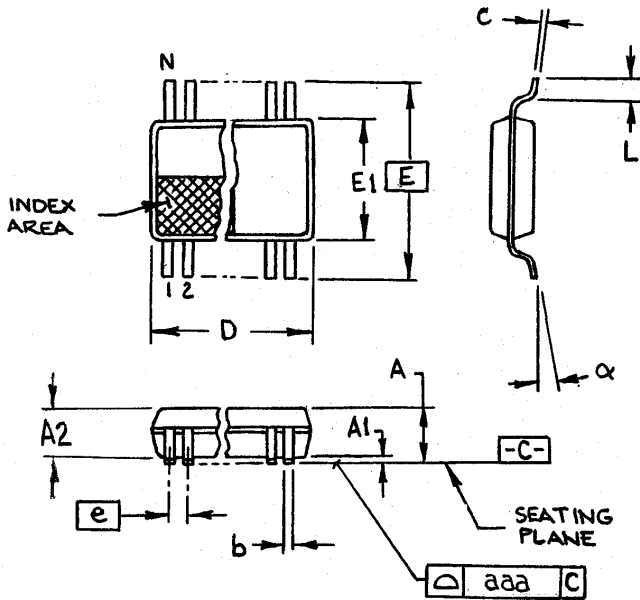
- ① All clock outputs should have provisions for a 15pf capacitor between the clock output and series terminating resistor. Not shown in all places to improve readability of diagram.
- ② Optional crystal load capacitors are recommended. They should be included in the layout but not inserted unless needed.

Component Values:

C1 : Crystal load values determined by user
 C2 : 22 F/20V/D case/Tantalum
 AVX TAJD226M020R
 C3 : 15pF capacitor
 FB = Fair-Rite products 2512066017X1
 All unmarked capacitors are 0.01 F ceramic

Connections to VDD:





6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (0.020 mil)

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|----------|-------------------------------------|------|--------------------------------|------|
| | MIN | MAX | MIN | MAX |
| A | - | 1.20 | - | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.17 | 0.27 | .007 | .011 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 8.10 BASIC | | 0.319 | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.50 BASIC | | 0.020 BASIC | |
| L | 0.45 | 0.75 | .018 | .30 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |
| aaa | - | 0.10 | - | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 48 | 12.40 | 12.60 | .488 | .496 |

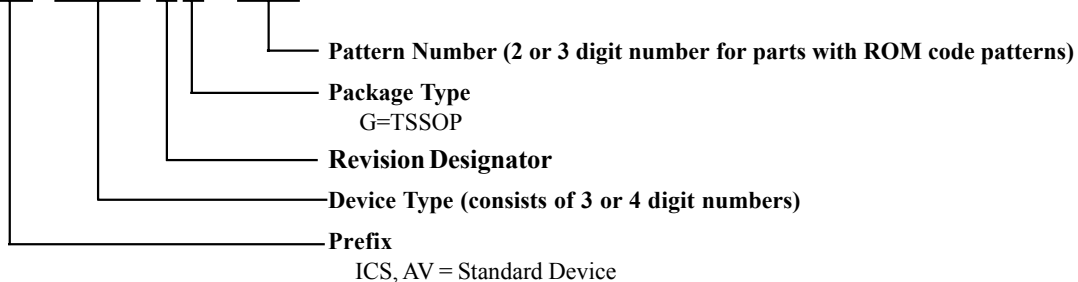
MO-153 JEDEC 7/8/00 Rev B
Doc.# 10-0039

Ordering Information

ICS9248yG-92

Example:

ICS XXXX y G - PPP



ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.