PMCXB1000UE

30 V, complementary N/P-channel Trench MOSFET

27 June 2016 | Product data sheet

1. General description

Complementary N/P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010B-6 (SOT1216) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Very low threshold voltage for portable applications: $V_{GS(th)}$ = 0.7 V
- Leadless ultra small and ultra thin SMD plastic package: 1.1 × 1.0 × 0.37 mm
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- Relay driver
- High-speed line driver
- Level shifter
- Power management in battery-driven portables

4. Quick reference data

Table 1. Quick reference data

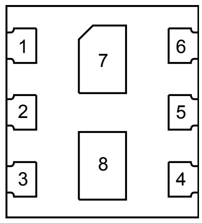
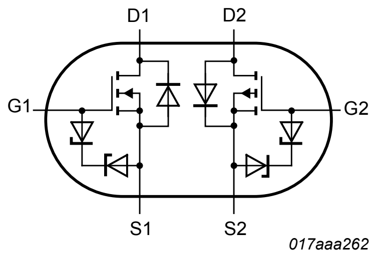
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1 (N-channel), Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 590 mA; T_j = 25 °C		-	550	670	mΩ
TR2 (P-channel), Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -410 mA; T_j = 25 °C		-	1.2	1.4	Ω
TR1 (N-channel)							
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	30	V
I_D	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C	[1]	-	-	590	mA
TR2 (P-channel)							
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	-30	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-	-410	mA

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2.

nexperia

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 Transparent top view **DFN1010B-6 (SOT1216)**	
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMCXB1000UE	DFN1010B-6	DFN1010B-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1216

7. Marking

Table 4. Marking codes

Type number	Marking code
PMCXB1000UE	B 101

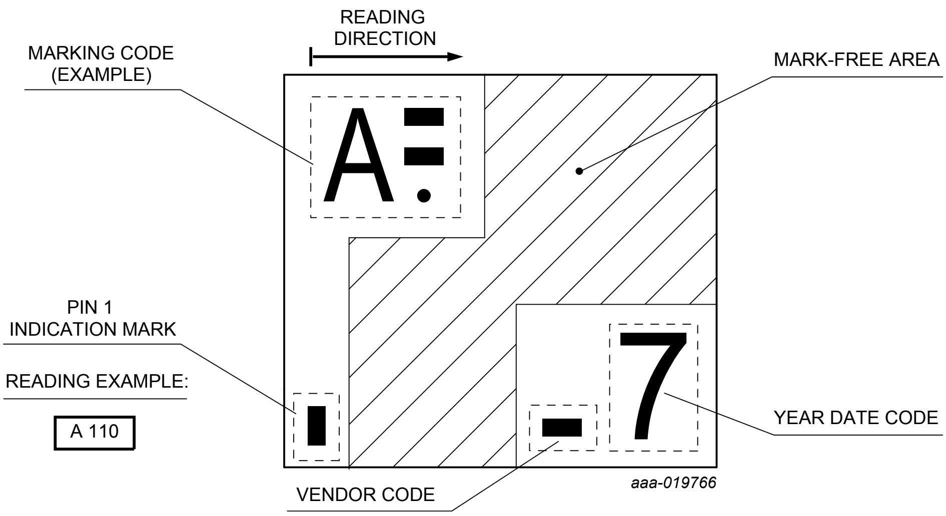


Fig. 1. DFN1010B-6 (SOT1216) binary marking code description

8. Limiting values

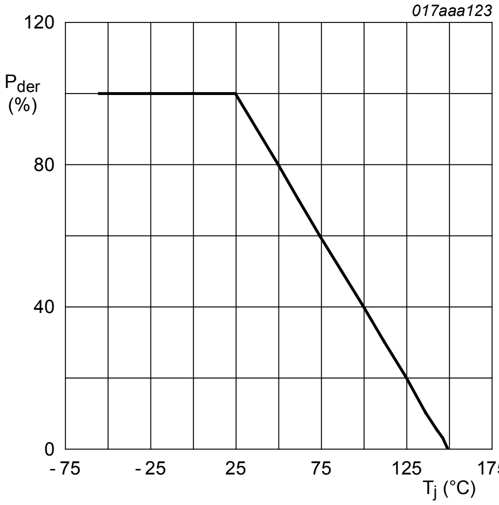
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
TR1 (N-channel)						
V_{DS}	drain-source voltage	T_j = 25 °C		-	30	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C	[1]	-	590	mA
		V_{GS} = 4.5 V; T_{amb} = 100 °C	[1]	-	370	mA
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 µs		-	2.3	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	285	mW
			[1]	-	410	mW
		T_{sp} = 25 °C		-	4	W
TR2 (P-channel)						
V_{DS}	drain-source voltage	T_j = 25 °C		-	-30	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-410	mA
		V_{GS} = -4.5 V; T_{amb} = 100 °C	[1]	-	-260	mA
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 µs		-	-1.7	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	285	mW
			[1]	-	410	mW
		T_{sp} = 25 °C		-	4	W
Per device						
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
TR1 (N-channel), Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	380	mA
TR2 (P-channel), Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	-410	mA

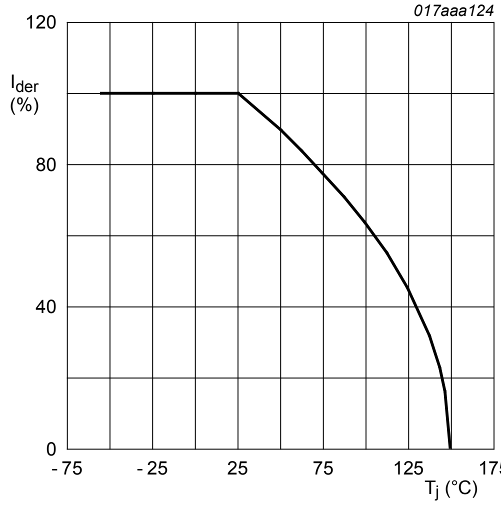
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig. 2. MOSFET transistor: Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

Fig. 3. MOSFET transistor: Normalized continuous drain current as a function of junction temperature

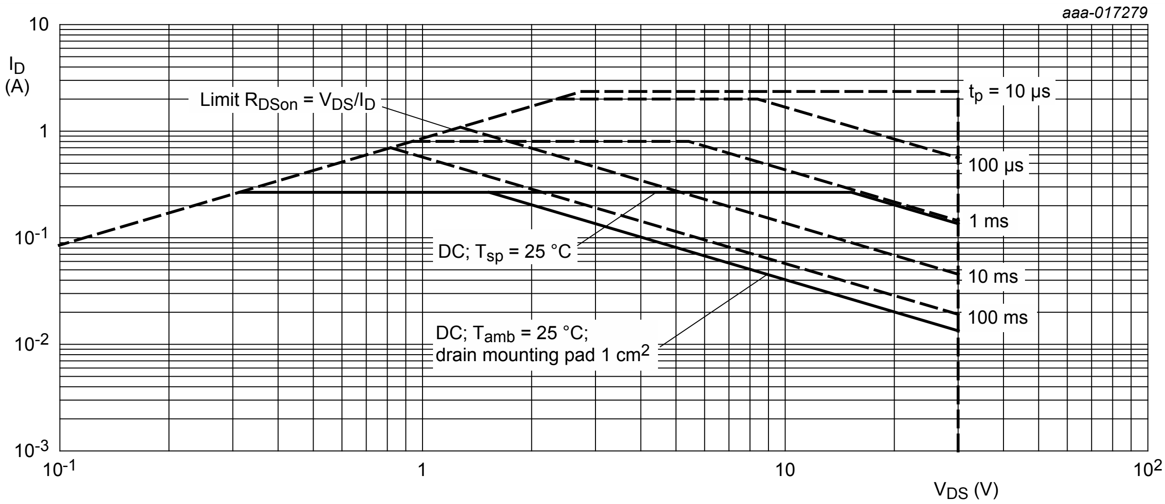


Fig. 4. TR1: Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

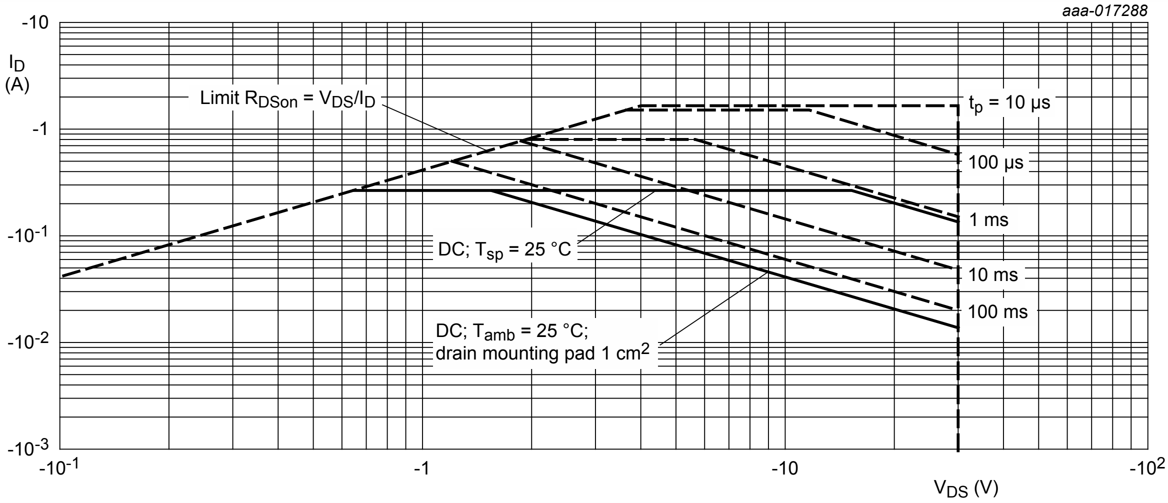


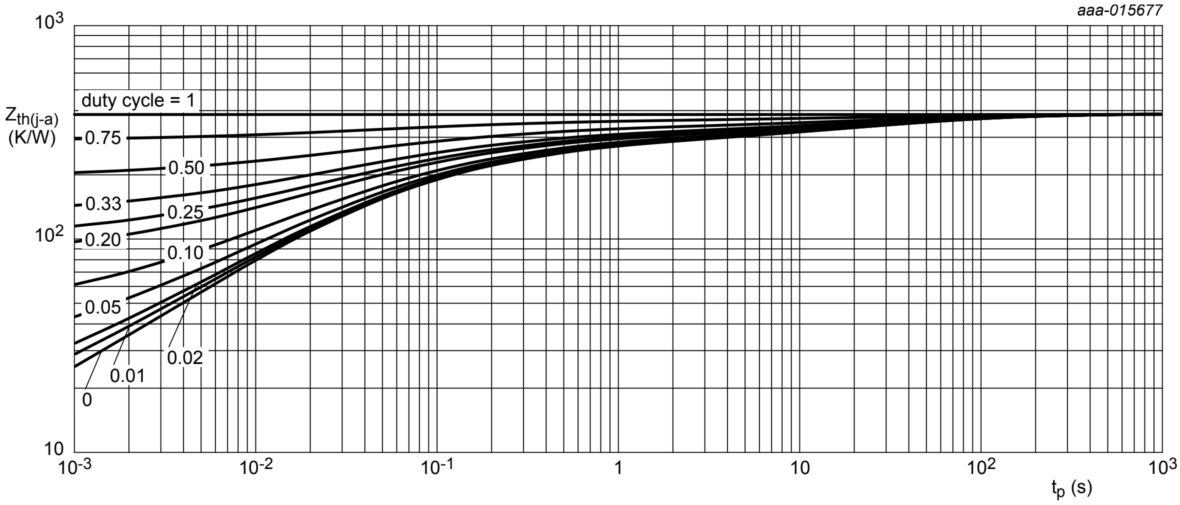
Fig. 5. TR2: Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

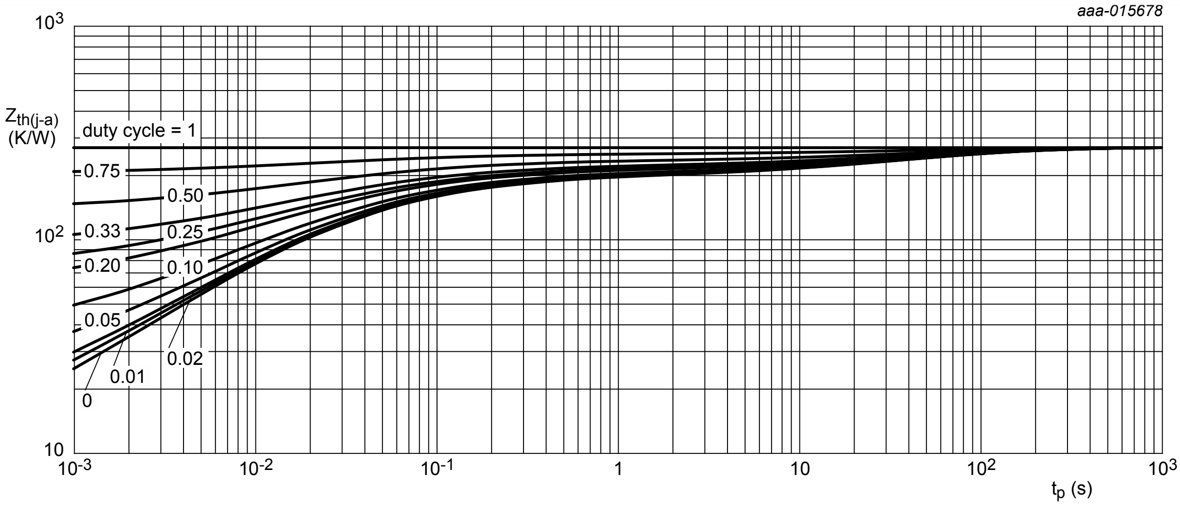
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1 (N-channel)							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	380	440	K/W
			[2]	-	275	305	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	27	31	K/W
TR2 (P-channel)							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	380	440	K/W
			[2]	-	275	305	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	27	31	K/W

[1] Device mounted on an FR4 PCB, single-sided copper; tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2.



FR4 PCB, standard footprint

Fig. 6. TR1 and TR2: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm^2

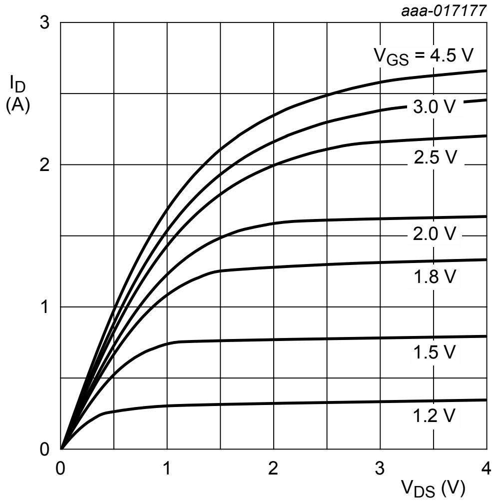
Fig. 7. TR1 and TR2: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

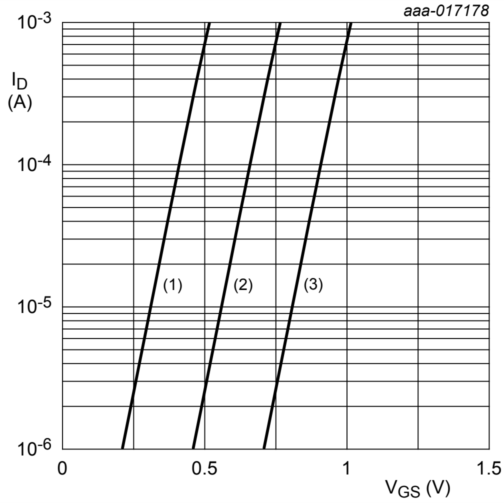
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1 (N-channel), Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		30	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 250 µA; V_{DS}=V_{GS}; T_j = 25 °C		0.45	0.7	0.95	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
I_{GSS}	gate leakage current	V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C		-	-	5	µA
		V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-5	µA
		V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-1	µA
		V_{GS} = 2.5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -2.5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 590 mA; T_j = 25 °C		-	550	670	mΩ
		V_{GS} = 4.5 V; I_D = 590 mA; T_j = 150 °C		-	960	1170	mΩ
		V_{GS} = 2.5 V; I_D = 590 mA; T_j = 25 °C		-	660	900	mΩ
		V_{GS} = 1.8 V; I_D = 80 mA; T_j = 25 °C		-	770	1120	mΩ
		V_{GS} = 1.5 V; I_D = 10 mA; T_j = 25 °C		-	890	1500	mΩ
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 590 mA; T_j = 25 °C		-	600	-	mS
TR2 (P-channel), Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -250 µA; V_{GS} = 0 V; T_j = 25 °C		-30	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = -250 µA; V_{DS}=V_{GS}; T_j = 25 °C		-0.45	-0.7	-0.95	V
I_{DSS}	drain leakage current	V_{DS} = -30 V; V_{GS} = 0 V; T_j = 25 °C		-	-	-1	µA
I_{GSS}	gate leakage current	V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C		-	-	5	µA
		V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-5	µA
		V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{GS} = -4.5 V; T_j = 25 °C		-	-	-1	µA
		V_{GS} = 2.5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -2.5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -410 mA; T_j = 25 °C		-	1.2	1.4	Ω
		V_{GS} = -4.5 V; I_D = -410 mA; T_j = 150 °C		-	2	2.4	Ω
		V_{GS} = -2.5 V; I_D = -320 mA; T_j = 25 °C		-	1.7	2.3	Ω
		V_{GS} = -1.8 V; I_D = -80 mA; T_j = 25 °C		-	2.1	3.1	Ω
		V_{GS} = -1.5 V; I_D = -10 mA; T_j = 25 °C		-	3	5.1	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
g_{fs}	forward transconductance	V_{DS} = -10 V; I_D = -410 mA; T_j = 25 °C		-	820	-	mS
TR1 (N-channel), Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DS} = 15 V; I_D = 590 mA; V_{GS} = 4.5 V; T_j = 25 °C		-	0.6	1.05	nC
Q_{GS}	gate-source charge			-	0.1	-	nC
Q_{GD}	gate-drain charge			-	0.1	-	nC
C_{iss}	input capacitance	V_{DS} = 15 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	30.3	-	pF
C_{oss}	output capacitance			-	5.8	-	pF
C_{rss}	reverse transfer capacitance			-	4.2	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; I_D = 590 mA; V_{GS} = 4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C		-	4	-	ns
t_r	rise time			-	7	-	ns
$t_{d(off)}$	turn-off delay time			-	12	-	ns
t_f	fall time			-	3	-	ns
TR2 (P-channel), Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DS} = -15 V; I_D = -410 mA; V_{GS} = -4.5 V; T_j = 25 °C		-	0.7	1.2	nC
Q_{GS}	gate-source charge			-	0.17	-	nC
Q_{GD}	gate-drain charge			-	0.16	-	nC
C_{iss}	input capacitance	V_{DS} = -15 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	43.2	-	pF
C_{oss}	output capacitance			-	5.9	-	pF
C_{rss}	reverse transfer capacitance			-	4.2	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = -15 V; I_D = -410 mA; V_{GS} = -4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C		-	3	-	ns
t_r	rise time			-	4	-	ns
$t_{d(off)}$	turn-off delay time			-	14	-	ns
t_f	fall time			-	5	-	ns
TR1 (N-channel), Source-drain diode characteristics							
V_{SD}	source-drain voltage	I_S = 380 mA; V_{GS} = 0 V; T_j = 25 °C		-	0.86	1.2	V
TR2 (P-channel), Source-drain diode characteristics							
V_{SD}	source-drain voltage	I_S = -410 mA; V_{GS} = 0 V; T_j = 25 °C		-	-0.95	-1.2	V



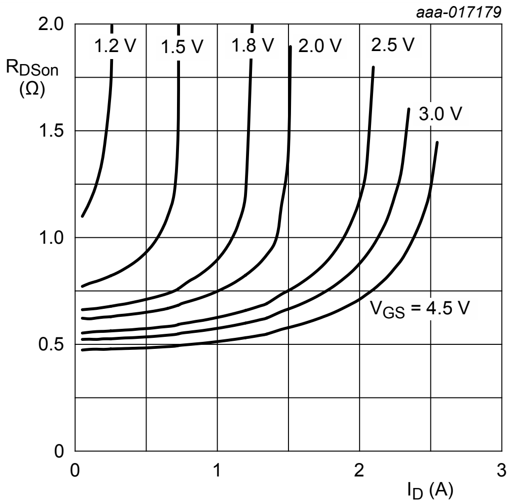
T_j = 25 °C

Fig. 8. TR1: Output characteristics: drain current as a function of drain-source voltage; typical values



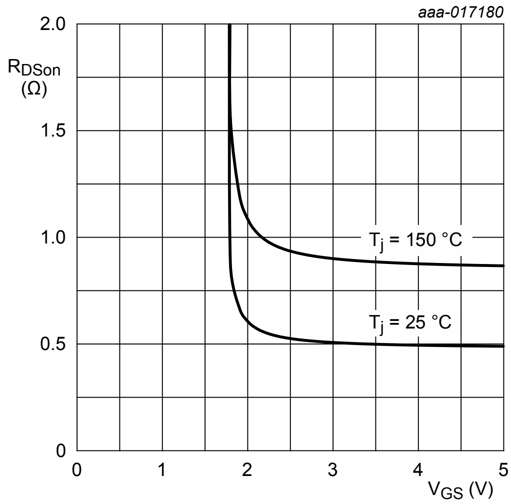
T_j = 25 °C; V_{DS} = 5 V
(1) minimum values
(2) typical values
(3) maximum values

Fig. 9. TR1: Sub-threshold drain current as a function of gate-source voltage



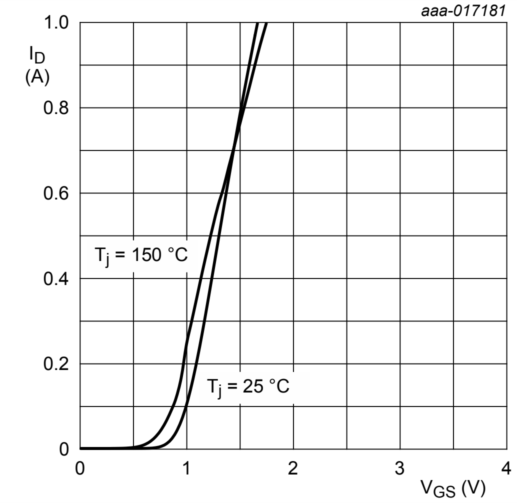
T_j = 25 °C

Fig. 10. TR1: Drain-source on-state resistance as a function of drain current; typical values



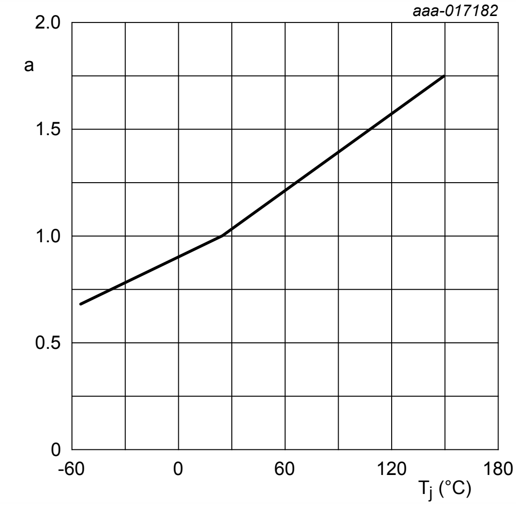
I_D = 1 A

Fig. 11. TR1: Drain-source on-state resistance as a function of gate-source voltage; typical values



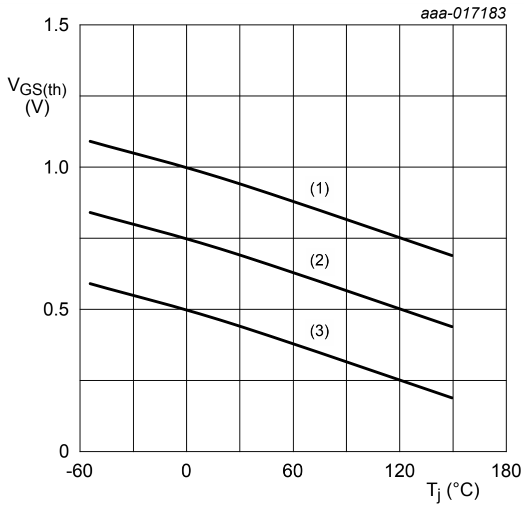
$V_{DS} > I_D \times R_{DSon}$

Fig. 12. TR1: Transfer characteristics: drain current as a function of gate-source voltage; typical values



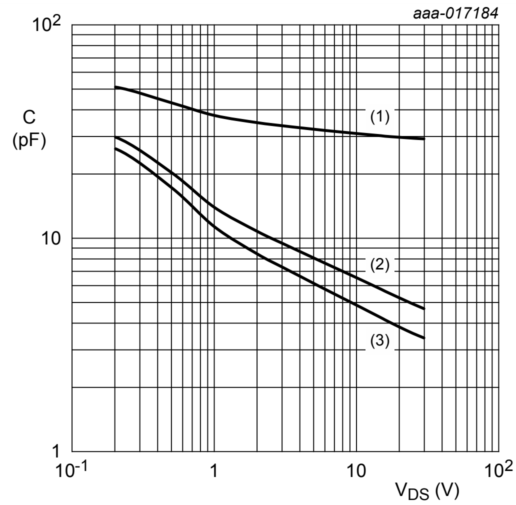
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 13. TR1: Normalized drain-source on-state resistance as a function of junction temperature; typical values



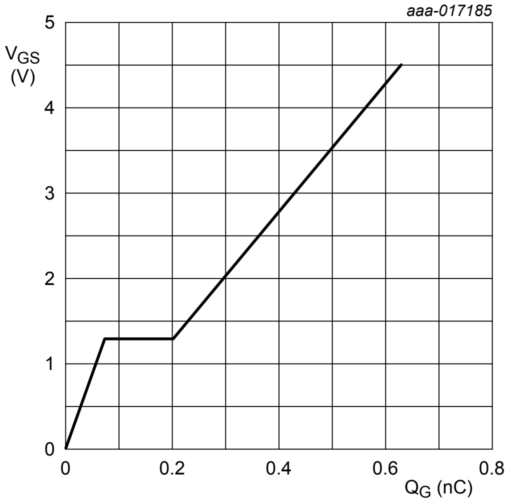
I_D = 0.25 mA; $V_{DS} = V_{GS}$
(1) maximum values
(2) typical values
(3) minimum values

Fig. 14. TR1: Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V
(1) C_{iss}
(2) C_{oss}
(3) C_{rss}

Fig. 15. TR1: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



I_D = 0.6 A; V_{DS} = 15 V; T_{amb} = 25 °C

Fig. 16. TR1: Gate-source voltage as a function of gate charge; typical values

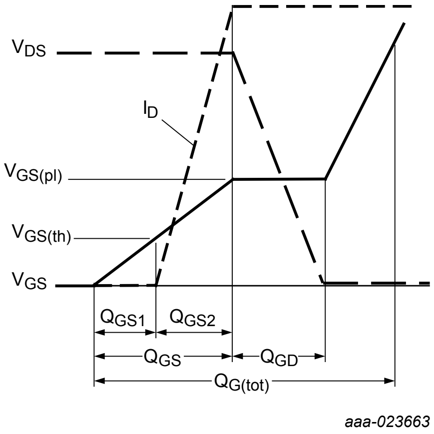
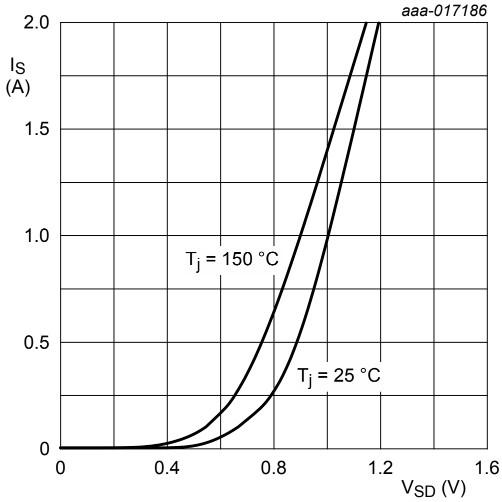
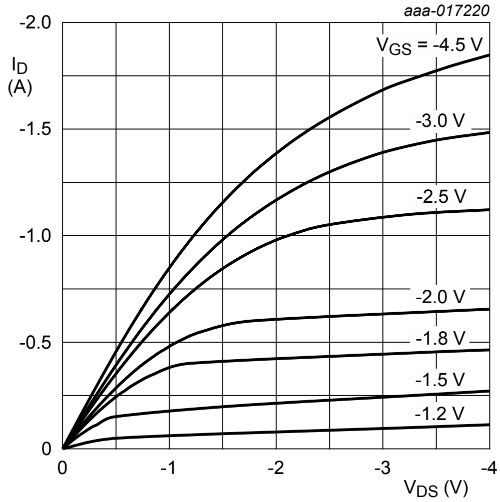


Fig. 17. TR1: Gate charge waveform definitions



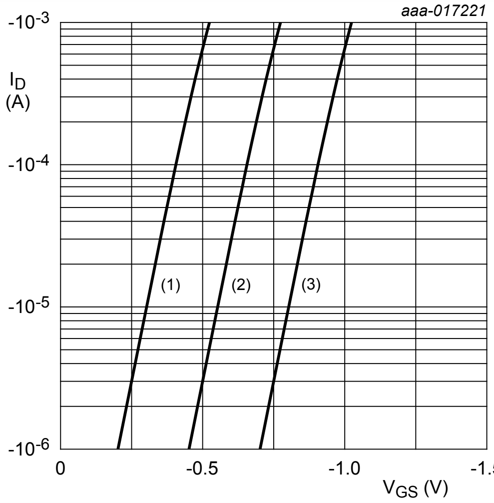
V_{GS} = 0 V

Fig. 18. TR1: Source current as a function of source-drain voltage; typical values



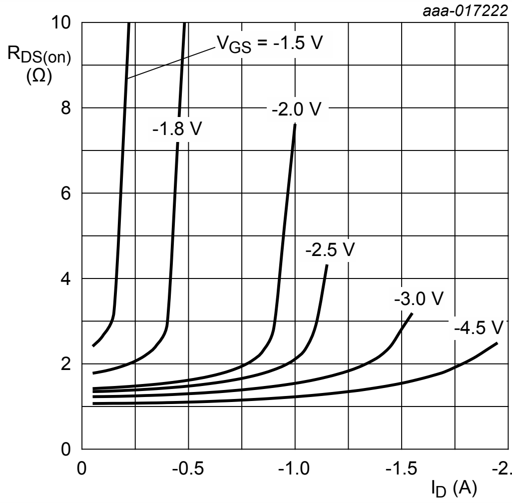
T_j = 25 °C

Fig. 19. TR2: Output characteristics: drain current as a function of drain-source voltage; typical values



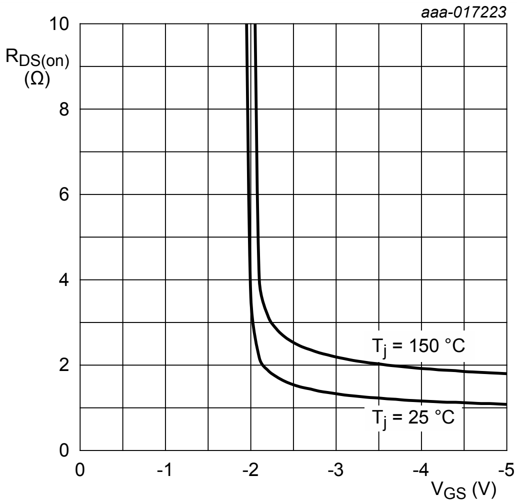
V_{DS} = -5 V
T_j = 25 °C
(1) minimum values
(2) typical values
(3) maximum values

Fig. 20. TR2: Sub-threshold drain current as a function of gate-source voltage



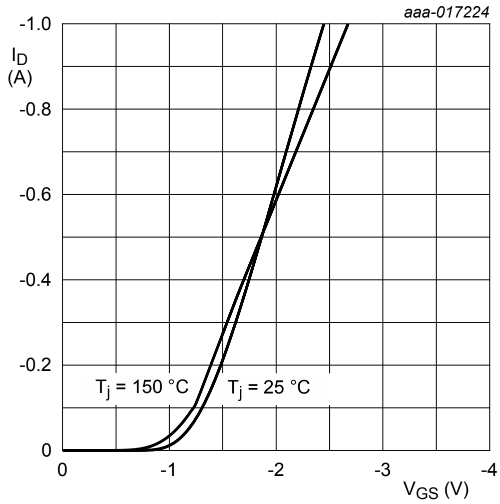
T_j = 25 °C

Fig. 21. TR2: Drain-source on-state resistance as a function of drain current; typical values



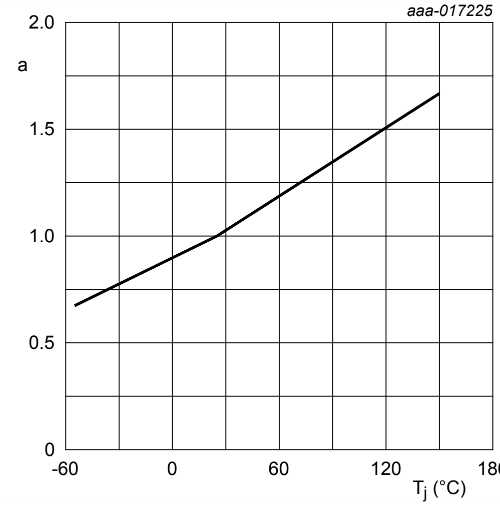
I_D = -0.4 A

Fig. 22. TR2: Drain-source on-state resistance as a function of gate-source voltage; typical values



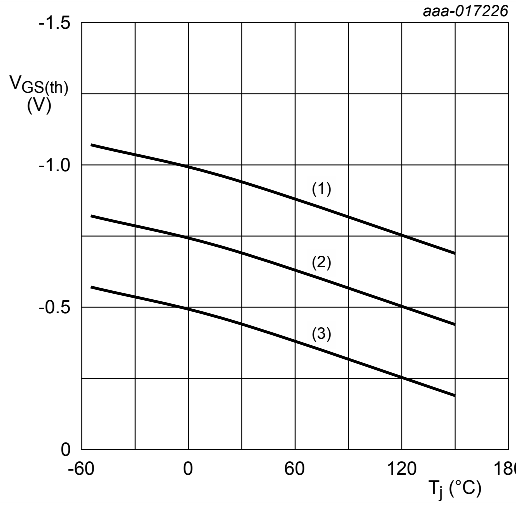
$V_{DS} > I_D \times R_{DSon}$

Fig. 23. TR2: Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 24. TR2: Normalized drain-source on-state resistance as a function of ambient temperature; typical values



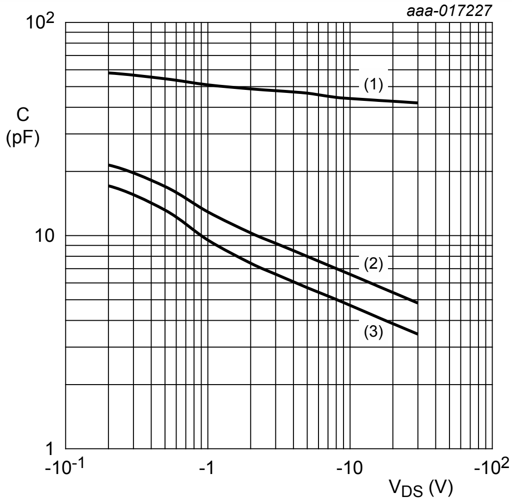
I_D = -250 µA; V_{DS} = V_{GS}

(1) maximum values

(2) typical values

(3) minimum values

Fig. 25. TR2: Gate-source threshold voltage as a function of junction temperature



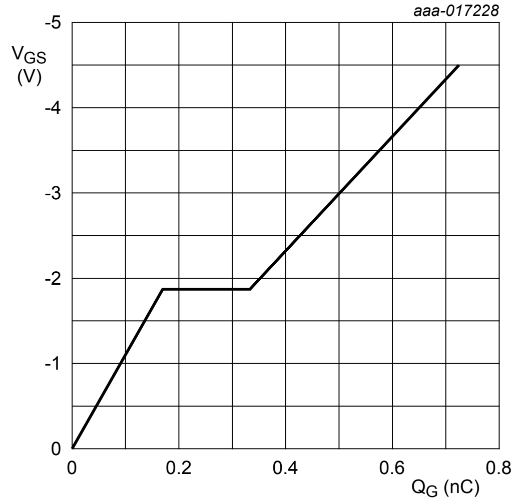
f = 1 MHz; V_{GS} = 0 V

(1) C_{iss}

(2) C_{oss}

(3) C_{rss}

Fig. 26. TR2: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{DS} = -15 V; I_D = -410 mA T_{amb} = 25 °C

Fig. 27. TR2: Gate-source voltage as a function of gate charge; typical values

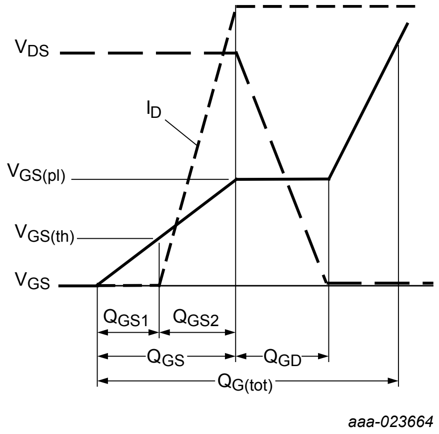
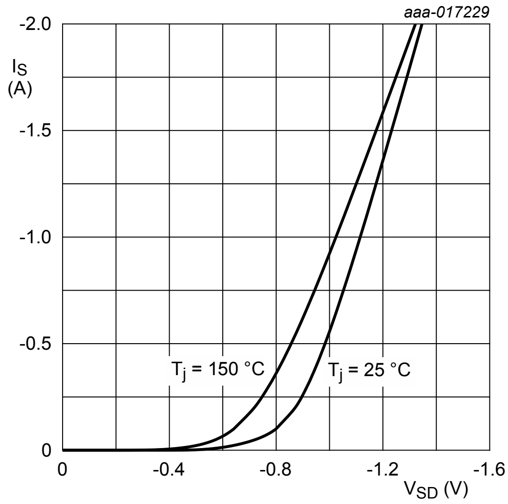


Fig. 28. TR2: Gate charge waveform definitions



$V_{GS} = 0$ V

Fig. 29. TR2: Source current as a function of source-drain voltage; typical values

11. Test information

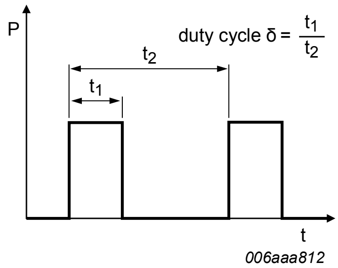
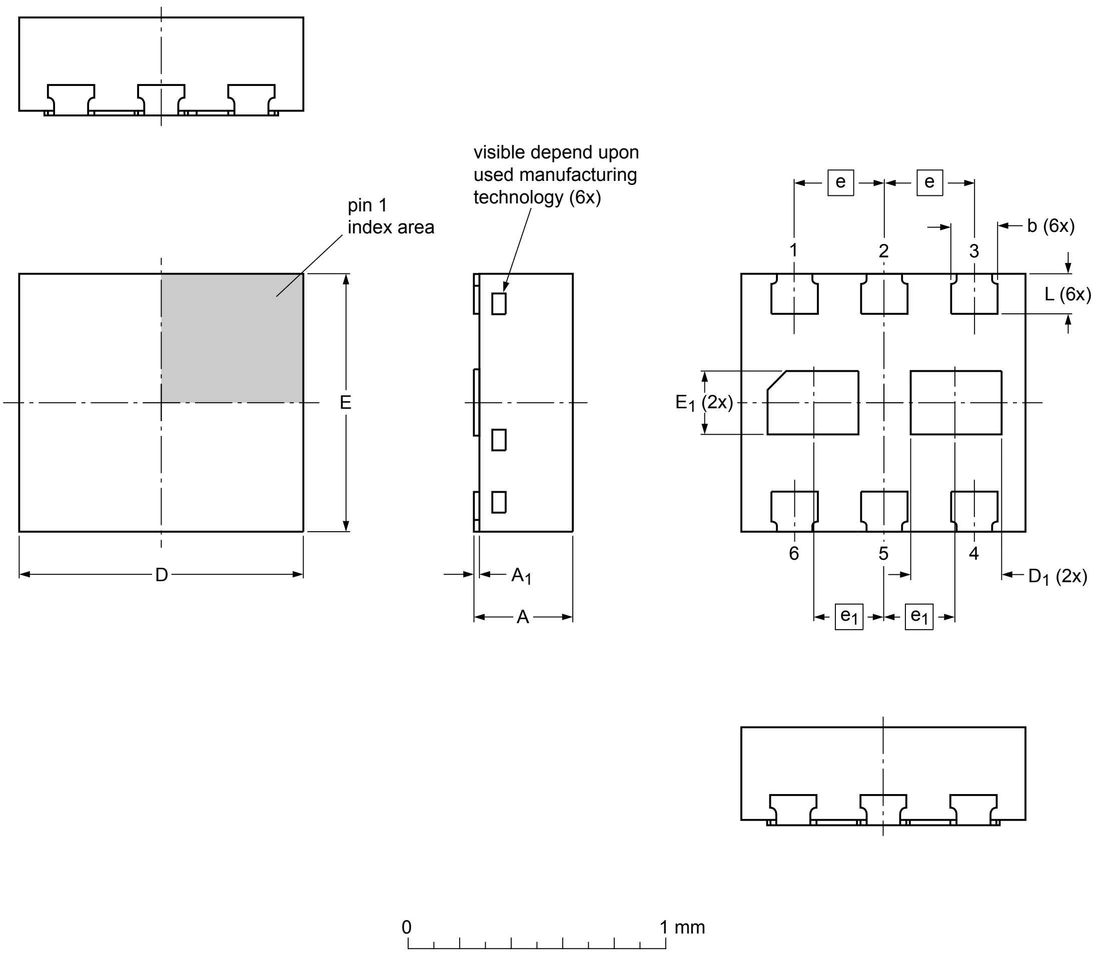


Fig. 30. Duty cycle definition

12. Package outline

DFN1010B-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body: 1.1 x 1.0 x 0.37 mm **SOT1216**



scale

Dimensions (mm are the original dimensions)

Unit		A	A_1	b	D	D_1	E	E_1	e	e_1	L
mm	min	0.34		0.15	1.05	0.32	0.95	0.22			0.125
	nom	0.37		0.18	1.10	0.35	1.00	0.25	0.35	0.275	0.155
	max	0.40	0.04	0.23	1.15	0.40	1.05	0.30			0.205

Note
1. Dimension A is including plating thickness.

sot1216_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1216						~~13-03-05~~ 13-03-06

Fig. 31. Package outline DFN1010B-6 (SOT1216)

13. Soldering

Footprint information for reflow soldering of DFN1010B-6 package **SOT1216**

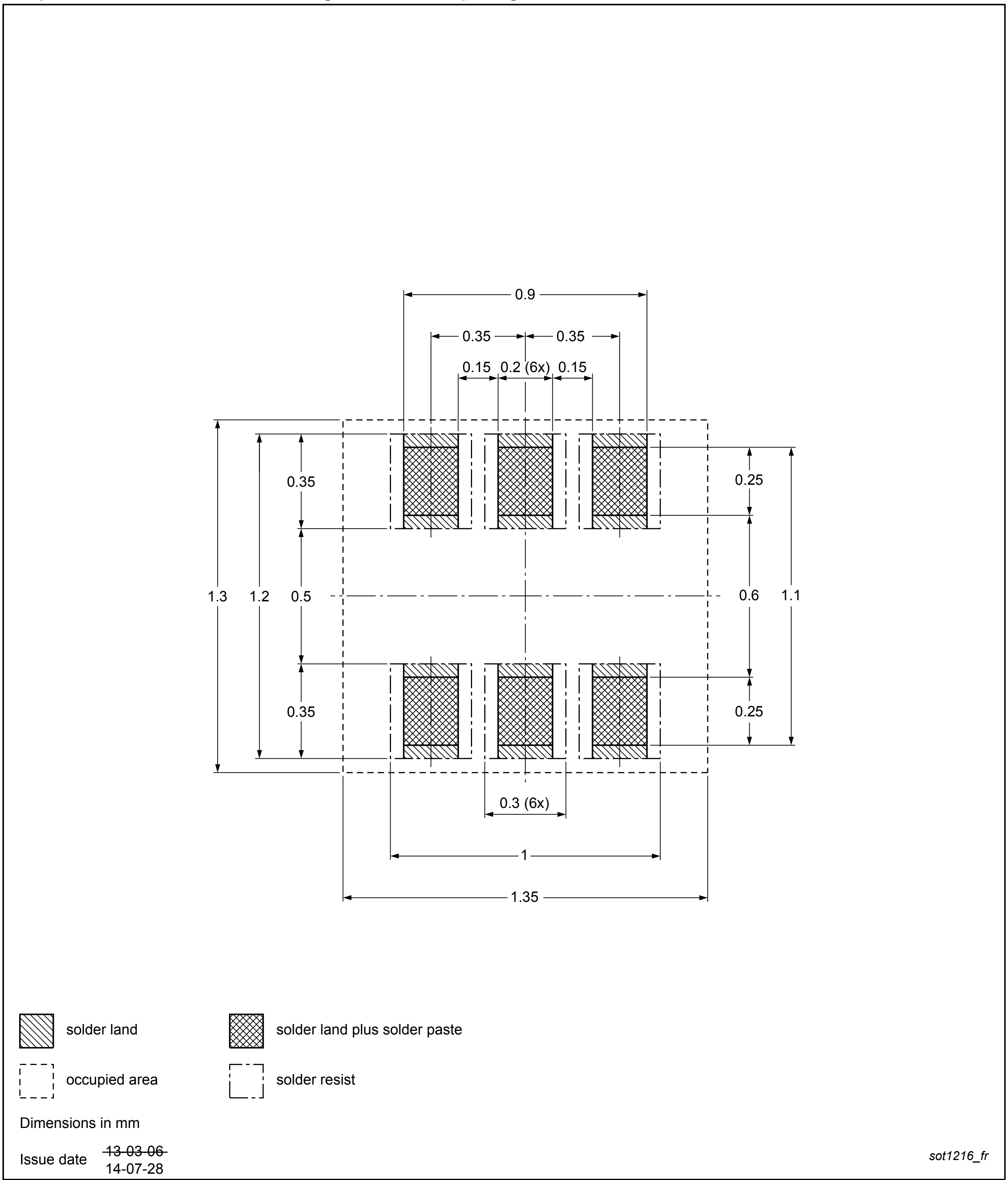


Fig. 32. Reflow soldering footprint for DFN1010B-6 (SOT1216)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMCXB1000UE v.1	20160627	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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16. Contents

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Date of release: 27 June 2016