19-1579; Rev 5; 8/10

10-Bit, 40MHz, Current/Voltage-Output DACs

General Description

The MAX5181 is a 10-bit, current-output digital-to-analog converter (DAC) designed for superior performance in signal reconstruction or arbitrary waveform generation applications requiring analog signal reconstruction with low distortion and low-power operation. The MAX5184 provides equal specifications, with on-chip precision resistors for voltage-output operation. The MAX5181/MAX5184 are designed for a 10pVs glitch operation to minimize unwanted spurious signal components at the output. An on-board 1.2V bandgap circuit provides a well-regulated, low-noise reference that can be disabled for external reference operation.

The devices are designed to provide a high level of signal integrity for the least amount of power dissipation. They operate from a single 2.7V to 3.3V supply. Additionally, these DACs have three modes of operation: normal, low-power standby, and full shutdown, which provides the lowest possible power dissipation with a 1µA (max) shutdown current. A fast wake-up time (0.5µs) from standby mode to full DAC operation facilitates power conservation by activating the DAC only when required.

The MAX5181/MAX5184 are available in 24-pin QSOP packages and are specified for the extended (-40°C to +85°C) temperature range. Additionally, the MAX5184 is also available in a 24-pin TQFN with exposed pad (EP) and is specified for the extended (-40°C to +85°C) temperature range. For lower resolution, 8-bit versions, refer to the MAX5187/MAX5190 data sheet.

Applications

Signal Reconstruction

Arbitrary Waveform Generators (AWGs)

Direct Digital Synthesis

Imaging Applications

Features

- ♦ **2.7V to 3.3V Single-Supply Operation**
- ♦ **Wide Spurious-Free Dynamic Range: 70dB at f_{OUT} = 2.2MHz**
- ♦ **Fully Differential Output**
- ♦ **Low-Current Standby or Full Shutdown Modes**
- ♦ **Internal 1.2V, Low-Noise Bandgap Reference**
- ♦ **Small 24-Pin QSOP and Thin QFN Packages**

Ordering Information

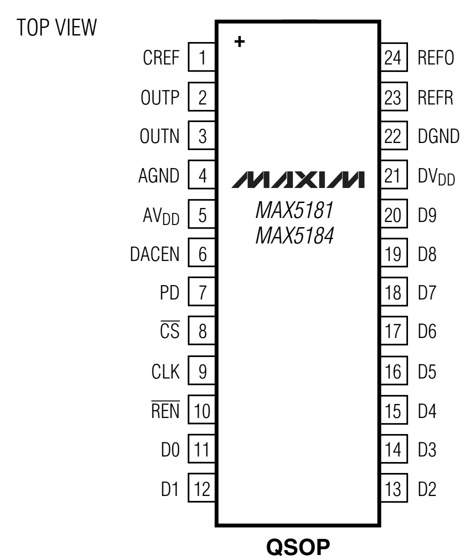
PART	TEMP RANGE	PIN-PACKAGE
MAX5181BEEG+	-40°C to +85°C	24 QSOP
MAX5184BEEG+	-40°C to +85°C	24 QSOP
MAX5184ETG+	-40°C to +85°C	24 TQFN-EP*
MAX5184ETG/V+	-40°C to +85°C	24 TQFN-EP*

*EP = Exposed pad.

+Denotes a lead(Pb)-free/RoHS-compliant package.

/V denotes an automotive qualified part.

Pin Configurations



Pin Configurations continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

AV_{DD}, DV_{DD} to AGND, DGND ....-0.3V to +6V
Digital Inputs to DGND..-0.3V to +6V
OUTP, OUTN, CREF to AGND ....-0.3V to +6V
V_{REF} to AGND ....-0.3V to +6V
AGND to DGND...-0.3V to +0.3V
AV_{DD} to DV_{DD}.. ±3.3V
Maximum Current into Any Pin...50mA

Continuous Power Dissipation (T_A = +70°C)
24-Pin QSOP (derate 9.50mW/°C above +70°C) 762mW
24-Pin TQFN
(derate 20.8mW/°C above +70°C) 1667mW
Operating Temperature Range
MAX518_BEEG...-40°C to +85°C
MAX5184ETG ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = 3V, V_{AGND} = V_{DGND} = 0V, f_{CLK} = 40MHz, I_{FS} = 1mA, 400Ω differential output, C_L = 5pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			10			Bits
Integral Nonlinearity	INL			-2	±0.5	+2	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic		-1	±0.5	1	LSB
Zero-Scale Error		MAX5181		-2		+2	LSB
		MAX5184		-8		+8	
Full-Scale Error		(Note 1)		-40	±15	+40	LSB
DYNAMIC PERFORMANCE							
Output Settling Time		To ±0.5LSB error band			25		ns
Glitch Impulse					10		pVs
Spurious-Free Dynamic Range to Nyquist	SFDR		f_{CLK} = 40MHz, f_{OUT} = 500kHz		72		dBc
			f_{CLK} = 40MHz, f_{OUT} = 2.2MHz, T_A = +25°C	57	70		
Total Harmonic Distortion to Nyquist	THD	MAX518_BEEG	f_{CLK} = 40MHz, f_{OUT} = 500kHz		-70		dBc
			f_{CLK} = 40MHz, f_{OUT} = 2.2MHz, T_A = +25°C		-68	-63	
		MAX5184ETG	f_{CLK} = 40MHz, f_{OUT} = 2.2MHz, T_A = +25°C		-68	-57	
Signal-to-Noise Ratio to Nyquist	SNR	MAX518_BEEG	f_{CLK} = 40MHz, f_{OUT} = 500kHz		61		dB
			f_{CLK} = 40MHz, f_{OUT} = 2.2MHz, T_A = +25°C	56	59		
		MAX5184ETG	f_{CLK} = 40MHz, f_{OUT} = 2.2MHz		59		
Clock and Data Feedthrough		All 0s to all 1s			50		nVs
Output Noise					10		pA/√Hz
ANALOG OUTPUT							
Full-Scale Output Voltage	V_{FS}				400		mV
Voltage Compliance of Output				-0.3		0.8	V
Output Leakage Current		DACEN = 0, MAX5181 only		-1		1	µA

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = 3V, V_{AGND} = V_{DGND} = 0V, f_{CLK} = 40MHz, I_{FS} = 1mA, 400Ω differential output, C_L = 5pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Full-Scale Output Current	I_{FS}	MAX5181 only	0.5	1	1.5	mA
DAC External Output Resistor load	R_L	MAX5181 only		400		Ω
REFERENCE						
Output Voltage Range	V_{REF}		1.12	1.2	1.28	V
Output Voltage Temperature Drift	TCV_{REF}			50		ppm/°C
Reference Output Drive Capability	I_{REFOUT}			10		µA
Reference Supply Rejection				0.5		mV/V
Current Gain (I_{FS} / I_{REF})				8		mA/mA
POWER REQUIREMENTS						
Analog Power-Supply Voltage	AV_{DD}		2.7		3.3	V
Analog Supply Current	I_{AVDD}	PD = 0, DACEN = 1, digital inputs at 0V or DV_{DD}		1.7	4.0	mA
Digital Power-Supply Voltage	DV_{DD}		2.7		3.3	V
Digital Supply Current	I_{DVDD}	PD = 0, DACEN = 1, digital inputs at 0V or DV_{DD}		4.2	5.0	mA
Standby Current	$I_{STANDBY}$	PD = 0, DACEN = 0, digital inputs at 0V or DV_{DD}		1.0	1.5	mA
Shutdown Current	I_{SHDN}	PD = 1, DACEN = X,digital inputs at 0V or DV_{DD} (X = don't care)		0.5	1	µA
LOGIC INPUTS AND OUTPUTS						
Digital Input Voltage High	V_{IH}		2			V
Digital Input Voltage Low	V_{IL}				0.8	V
Digital Input Current	I_{IN}	V_{IN} = 0V or DV_{DD}			±1	µA
Digital Input Capacitance	C_{IN}			10		pF
TIMING CHARACTERISTICS						
DAC DATA to CLK Rise Setup Time	t_{DS}		10			ns
DAC CLK Rise to DATA Hold Time	t_{DH}		0			ns
$\overline{CS}$ Fall to CLK Rise Time				5		ns
$\overline{CS}$ Fall to CLK Fall Time				5		ns
DACEN Rise Time to V_{OUT}				0.5		µs
PD Fall Time to V_{OUT}				50		µs
Clock Period	t_{CLK}		25			ns
Clock High Time	t_{CH}		10			ns
Clock Low Time	t_{CL}		10			ns

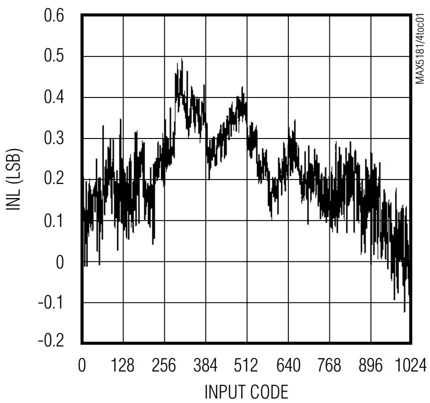
Note 1: Excludes reference and reference resistor (MAX5184) tolerance.

10-Bit, 40MHz, Current/Voltage-Output DACs

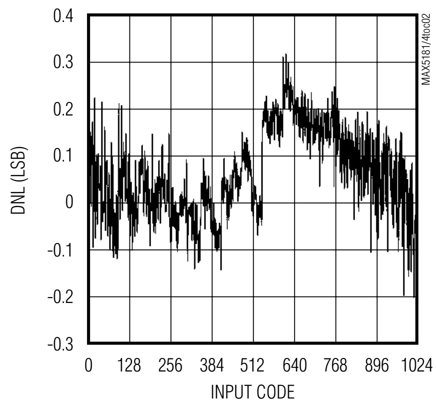
Typical Operating Characteristics

($AV_{DD} = DV_{DD} = 3V$, $V_{AGND} = V_{DGND} = 0V$, $I_{FS} = 1mA$, 400Ω differential output, $C_L = 5pF$, $T_A = +25°C$, unless otherwise noted.)

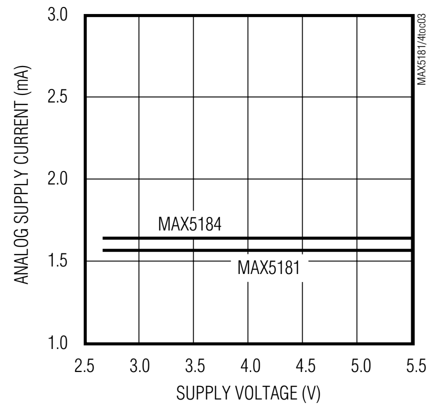
INTEGRAL NONLINEARITY vs. INPUT CODE



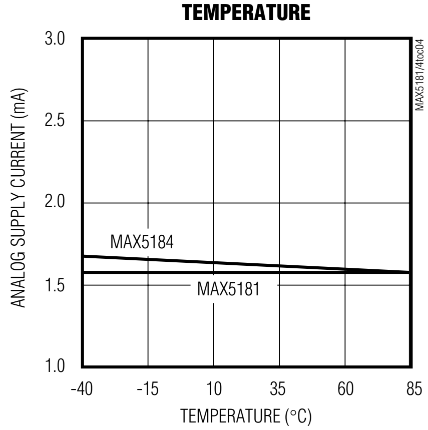
DIFFERENTIAL NONLINEARITY vs. INPUT CODE



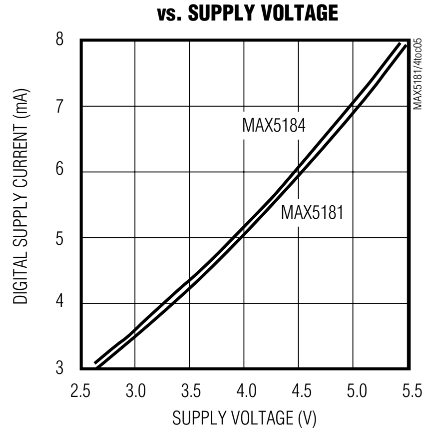
ANALOG SUPPLY CURRENT vs. SUPPLY VOLTAGE



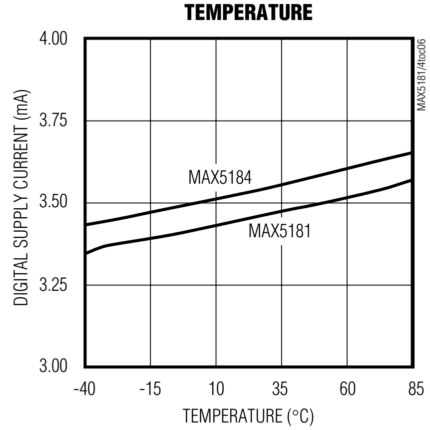
ANALOG SUPPLY CURRENT vs. TEMPERATURE



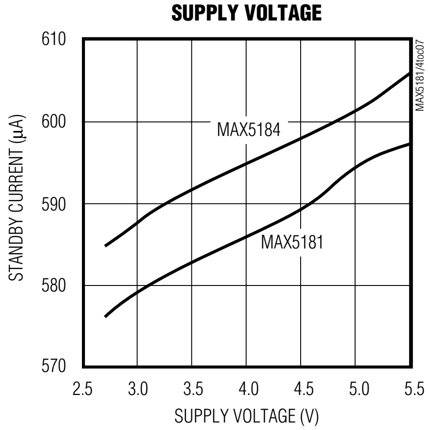
DIGITAL SUPPLY CURRENT vs. SUPPLY VOLTAGE



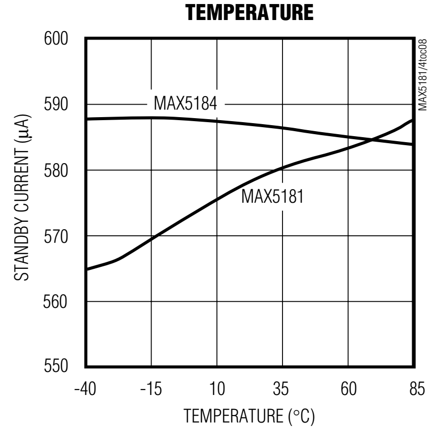
DIGITAL SUPPLY CURRENT vs. TEMPERATURE



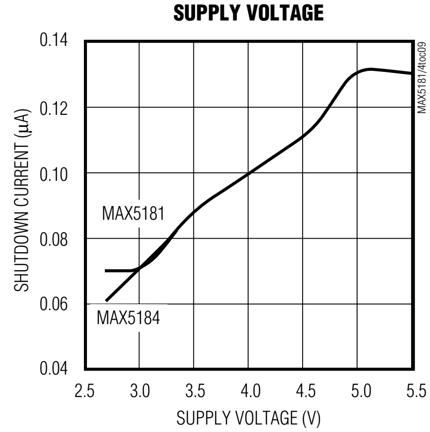
STANDBY CURRENT vs. SUPPLY VOLTAGE



STANDBY CURRENT vs. TEMPERATURE



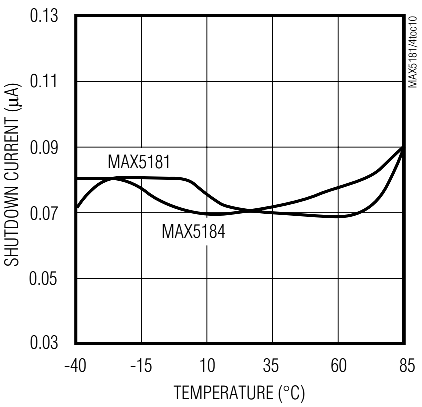
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



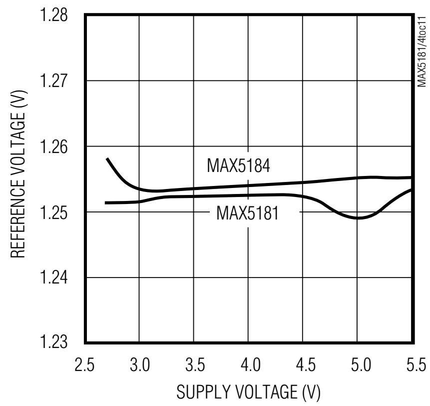
Typical Operating Characteristics (continued)

($AV_{DD} = DV_{DD} = 3V$, $V_{AGND} = V_{DGND} = 0V$, $I_{FS} = 1mA$, 400Ω differential output, $C_L = 5pF$, $T_A = +25°C$, unless otherwise noted.)

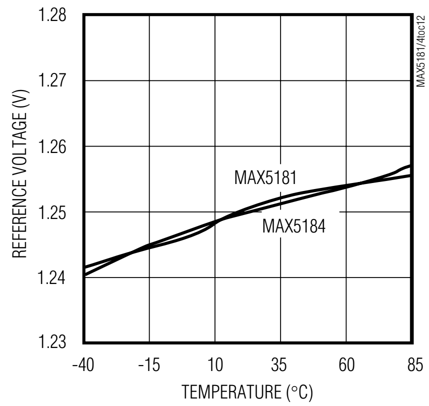
SHUTDOWN CURRENT vs. TEMPERATURE



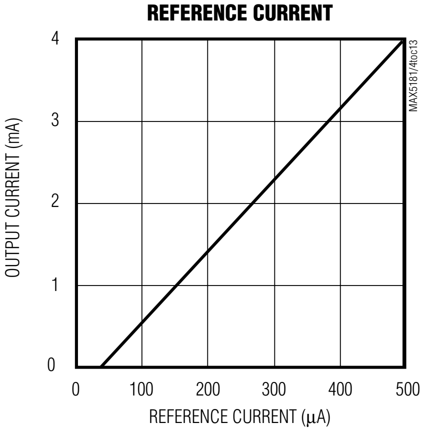
INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



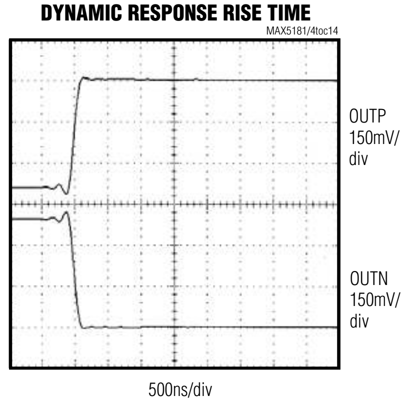
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



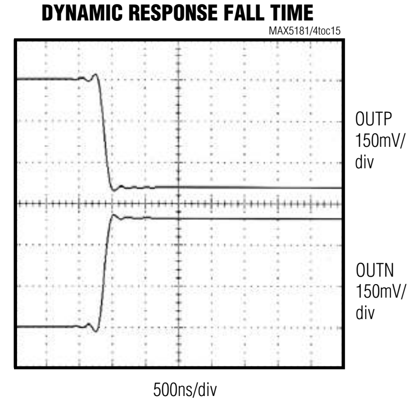
OUTPUT CURRENT vs. REFERENCE CURRENT



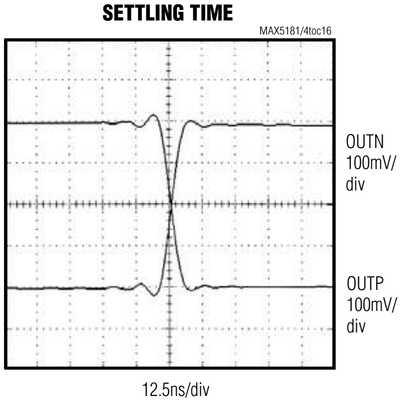
DYNAMIC RESPONSE RISE TIME



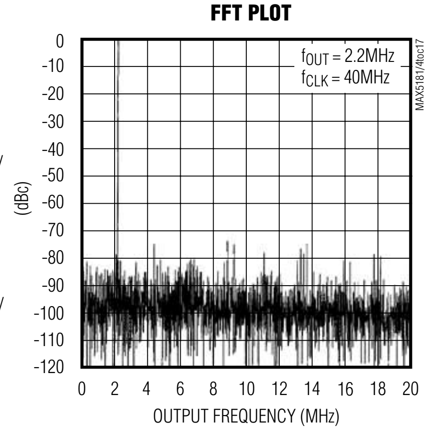
DYNAMIC RESPONSE FALL TIME



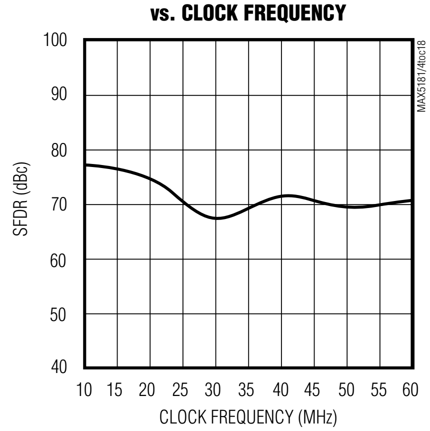
SETTLING TIME



FFT PLOT

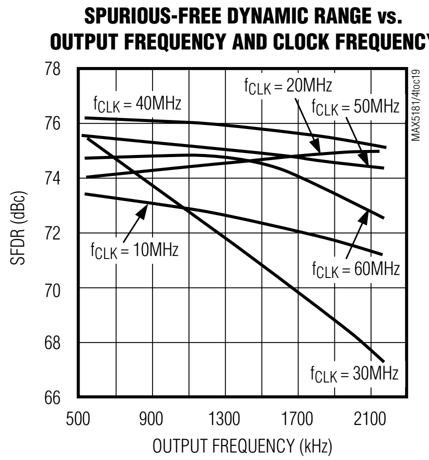


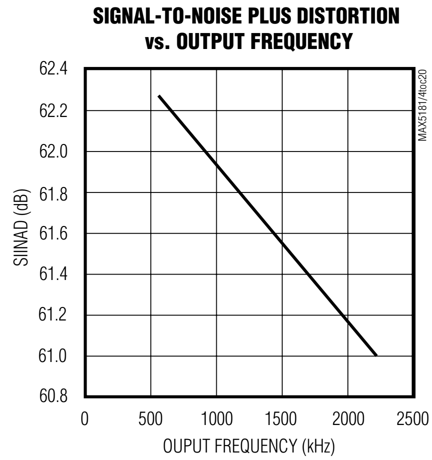
SPURIOUS-FREE DYNAMIC RANGE vs. CLOCK FREQUENCY

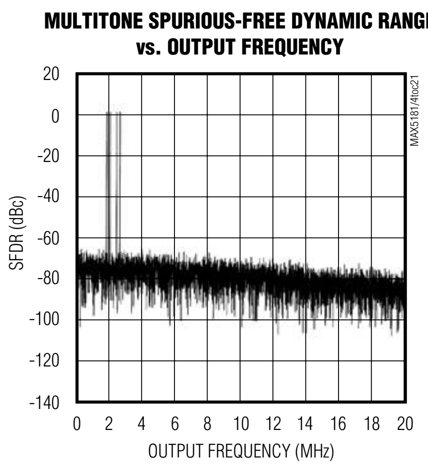


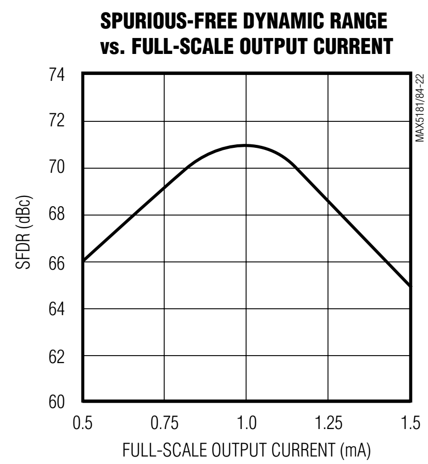
Typical Operating Characteristics (continued)

($AV_{DD} = DV_{DD} = 3V$, $V_{AGND} = V_{DGND} = 0V$, $I_{FS} = 1mA$, 400Ω differential output, $C_L = 5pF$, $T_A = +25°C$, unless otherwise noted.)









Pin Description

PIN		NAME	FUNCTION
QSOP	TQFN		
1	22	CREF	REFO
2	23	OUTP	Positive Analog Output. Current output for MAX5181; voltage output for MAX5184.
3	24	OUTN	Negative Analog Output. Current output for MAX5181; voltage output for MAX5184.
4	1	AGND	Analog Ground
5	2	AV_{DD}	Analog Positive Supply, 2.7V to 3.3V
6	3	DACEN	DAC Enable, Digital Input 0: Enter DAC standby mode with PD = DGND 1: Power-up DAC with PD = DGND X: Enter shutdown mode with PD = DVDD (X = don't care)
7	4	PD	Power-Down Select 0: Enter DAC standby mode (DACEN = DGND) or power-up DAC (DACEN = DVDD) 1: Enter shutdown mode
8	5	$\overline{CS}$	Active-Low Chip Select
9	6	CLK	Clock Input
10	7	$\overline{REN}$	Active-Low Reference Enable. Connect to DGND to activate on-chip 1.2V reference.
11	8	D0	Data Bit D0 (LSB)
12–19	9–16	D1–D8	Data Bits D1–D8
20	17	D9	Data Bit D9 (MSB)
21	18	DV_{DD}	Digital Supply, 2.7V to 3.3V
22	19	DGND	Digital Ground
23	20	REFR	Reference Input
24	21	REFO	Reference Output
—	—	EP	Exposed Pad (TQFN Only). Internally connected to AGND. Connected to the analog ground plane (AGND).

Detailed Description

The MAX5181/MAX5184 are 10-bit digital-to-analog converters (DACs) capable of operating with clock speeds up to 40MHz. Each converter consists of separate input and DAC registers, followed by a current source array capable of generating up to 1.5mA full-scale output current (Figure 1). An integrated 1.2V voltage reference and control amplifier determine the data converters' full-scale output currents/voltages. Careful reference design ensures close gain matching and excellent drift characteristics. The MAX5184's voltage output operation features matched 400Ω on-chip resistors that convert the current-array current into a voltage.

Internal Reference and Control Amplifier

The MAX5181/MAX5184 provide an integrated 50ppm/°C, 1.2V, low-noise bandgap reference that can be disabled and overridden by an external reference voltage. REFO serves either as an external reference input or an integrated reference output. If $\overline{REN}$ is connected to DGND, the internal reference is selected and REFO provides a 1.2V output. Due to its limited 10µA output drive capability, REFO must be buffered with an external amplifier, if heavier loading is required.

The MAX5181/MAX5184 also employ a control amplifier designed to regulate simultaneously the full-scale output current (I_{FS}) for both outputs of the devices. The output current is calculated as follows:

$$I_{FS} = 8 \times I_{REF}$$

where I_{REF} is the reference output current (I_{REF} = V_{REFO}/R_{SET}) and I_{FS} is the full-scale output current. R_{SET} is the reference resistor that determines the amplifier's output current on the MAX5181 (Figure 2). This current is mirrored into the current source array, where it is equally distributed between matched current segments and summed to valid output current readings for the DACs.

The MAX5184 converts this output current into a differential output voltage (V_{OUT}) with two internal, ground-referenced 400Ω load resistors. Using the internal 1.2V reference voltage, the MAX5184's integrated

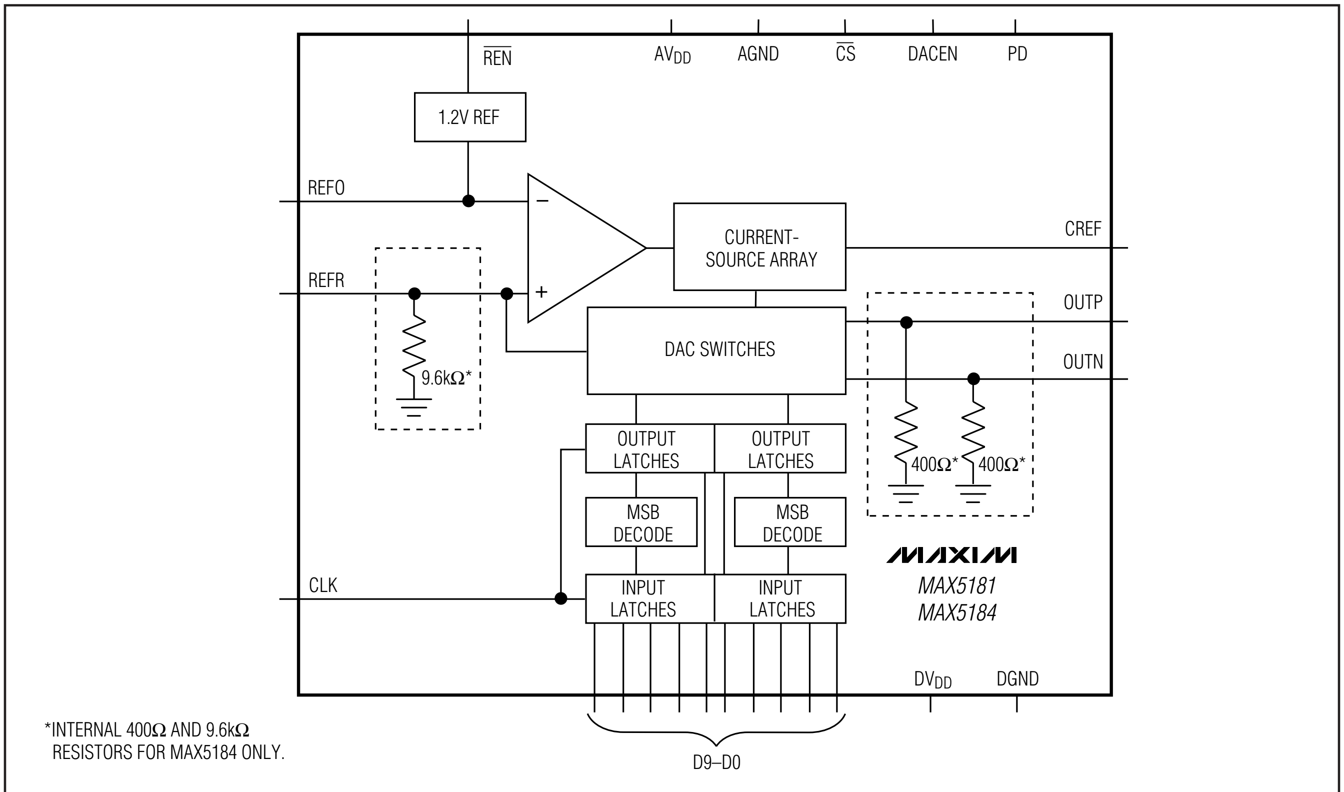


Figure 1. Functional Diagram

reference output-current resistor (R_{SET} = 9.6kΩ) sets I_{REF} to 125µA and I_{FS} to 1mA.

External Reference

To disable the MAX5181/MAX5184's internal reference, connect $\overline{REN}$ to DV_{DD}. A temperature-stable, external reference may now be applied to drive the REFO pin to set the full-scale output (Figure 3). Choose a reference capable of supplying at least 150µA to drive the bias circuit that generates the cascode current for the current array. For improved accuracy and drift performance, choose a fixed output voltage reference such as the 1.2V, 25ppm/°C MAX6520 bandgap reference.

Standby Mode

To enter the lower-power standby mode, connect digital inputs PD and DACEN to DGND. In standby, both the reference and the control amplifier are active with the current array inactive. To exit this condition, DACEN must be pulled high with PD held at DGND. The MAX5181/MAX5184 typically require 50µs to wake up and let both outputs and the reference settle.

Shutdown Mode

For lowest power consumption, the MAX5181/MAX5184 provide a power-down mode in which the reference, control amplifier, and current array are inactive and the DAC supply current is reduced to 1µA. To enter this mode, connect PD to DV_{DD}. To return to active mode, connect PD to DGND and DACEN to DV_{DD}. About 50µs are required for the parts to leave shutdown mode and settle to their outputs' values prior to shutdown. Table 1 lists the power-down mode selection.

Timing Information

Figure 4 shows a detailed timing diagram for the MAX5181/MAX5184. With each high transition of the clock, the input latch is loaded with the digital value set by bits D9 through D0. The content of the input latch is then shifted to the DAC register, and the output updates at the rising edge of the next clock.

Outputs

The MAX5181 output is designed to supply full-scale output currents of 1mA into 400Ω loads in parallel with a capacitive load of 5pF. The MAX5184 features integrated 400Ω resistors that restore the array current to proportional, differential voltages of 400mV. These differential output voltages can then be used to drive a balun transformer or a low-distortion, high-speed operational amplifier to convert the differential voltage into a single-ended voltage.

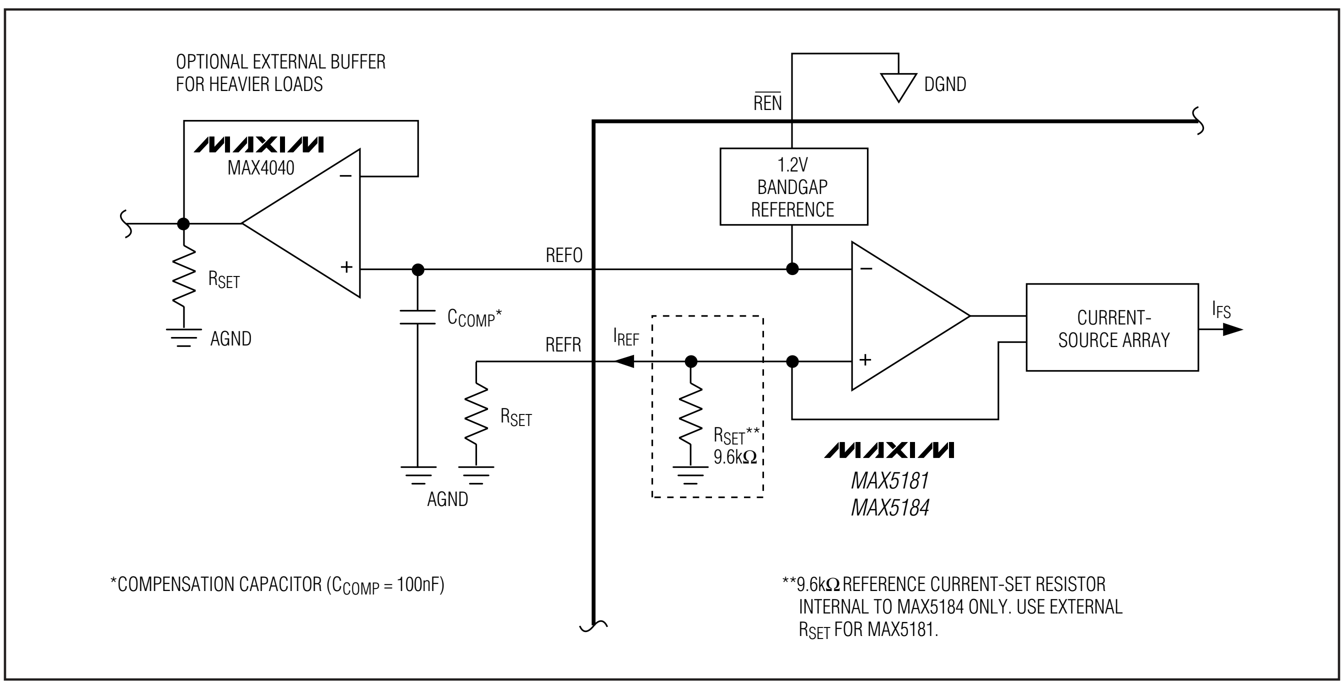


Figure 2. Setting I_{FS} with the Internal 1.2V Reference and the Control Amplifier

Table 1. Power-Down Mode Selection

PD (POWER-DOWN SELECT)	DACEN (DAC ENABLE)	POWER-DOWN MODE	OUTPUT STATE	
0	0	Standby	MAX5181	High-Z
			MAX5184	AGND
0	1	Wake-Up	Last state prior to standby mode	
1	X	Shutdown	MAX5181	High-Z
			MAX5184	AGND

X = Don't care.

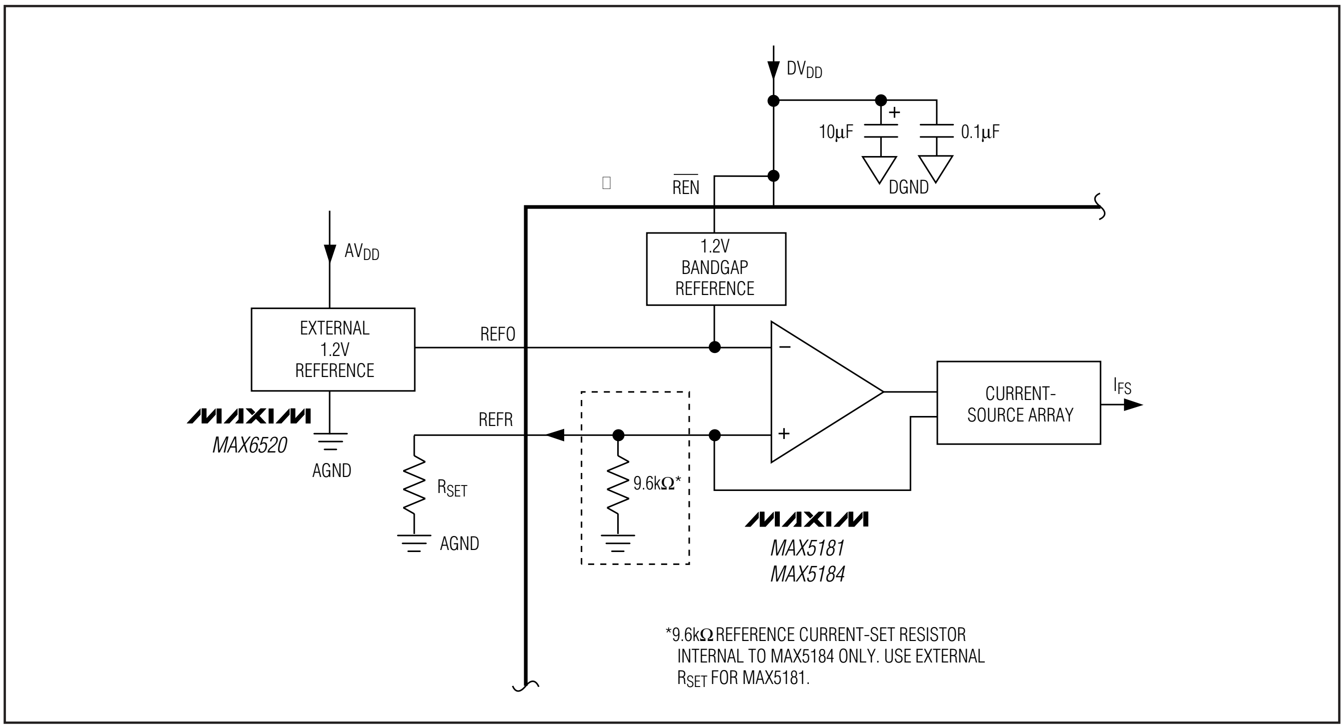


Figure 3. MAX5181/MAX5184 with External Reference

Applications Information

Static and Dynamic Performance Definitions

Integral Nonlinearity

Integral nonlinearity (INL) (Figure 5a) is the deviation of the values on an actual transfer function from either a best-straight-line fit (closest approximation to the actual transfer curve) or a line drawn between the endpoints of the transfer function once offset and gain errors have been nullified. For a DAC, the deviations are measured every single step.

Differential Nonlinearity

Differential nonlinearity (DNL) (Figure 5b) is the difference between an actual step height and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

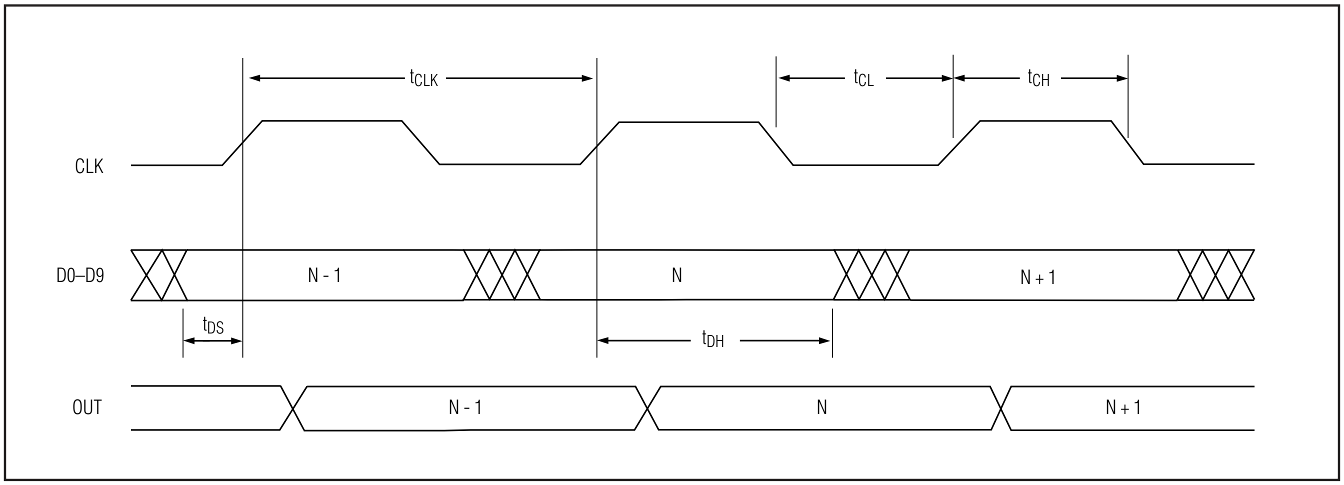


Figure 4. Timing Diagram

Offset Error

Offset error (Figure 5c) is the difference between the ideal and the actual offset point. For a DAC, the offset point is the step value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated by trimming.

Gain Error

Gain error (Figure 5d) is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Settling Time

Settling time is the amount of time required from the start of a transition until the DAC output settles its new output value to within the converter's specified accuracy.

Digital Feedthrough

Digital feedthrough is the noise generated on a DAC's output when any digital input transitions. Proper board layout and grounding will significantly reduce this noise, but there will always be some feedthrough caused by the DAC itself.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the input signal's first four harmonics to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2)}}{V_1}\right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component.

Differential to Single-Ended Conversion

The MAX4108 low-distortion, high-input bandwidth amplifier may be used to generate a voltage from the array current output of the MAX5181. The differential voltage across OUTP and OUTN is converted into a single-ended voltage by designing an appropriate operational amplifier configuration (Figure 6).

I/Q Reconstruction in a QAM Application

The low-distortion performance of two MAX5181/MAX5184s supports analog reconstruction of in-phase (I) and quadrature (Q) carrier components typically used in quadrature amplitude modulation (QAM) architectures where two separate buses carry the I and Q data. A QAM signal is both amplitude (AM) and phase modulated, created by summing two independently modulated carriers of identical frequency but different phase (90° phase difference).

In a typical QAM application (Figure 7), the modulation occurs in the digital domain, and two DACs such as the MAX5181/MAX5184 may be used to reconstruct the analog I and Q components.

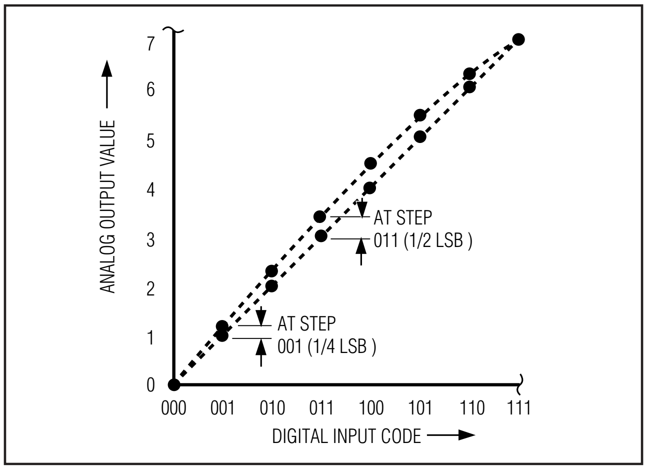


Figure 5a. Integral Nonlinearity

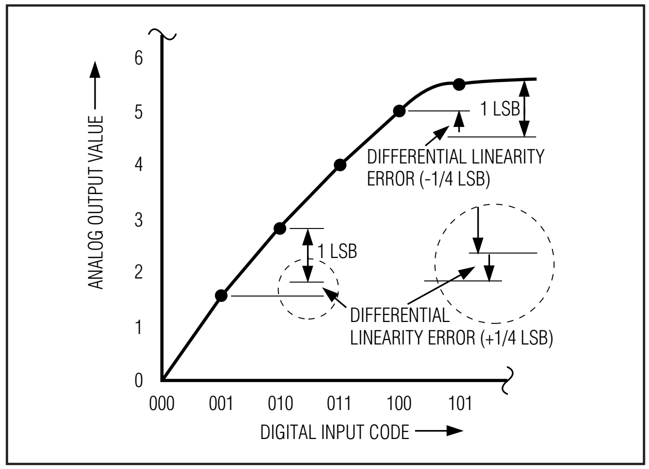


Figure 5b. Differential Nonlinearity

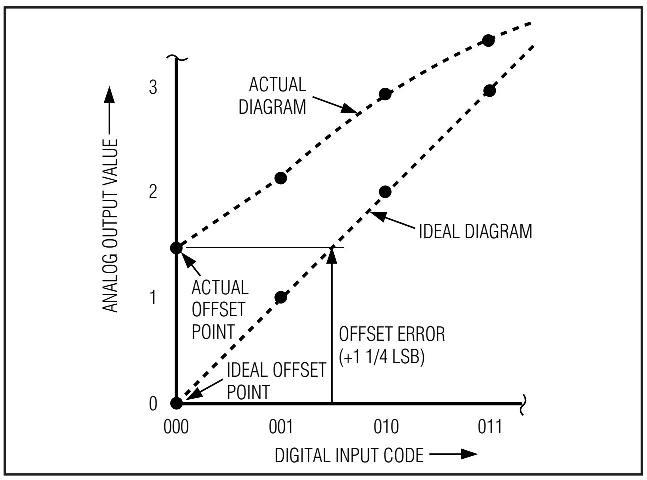


Figure 5c. Offset Error

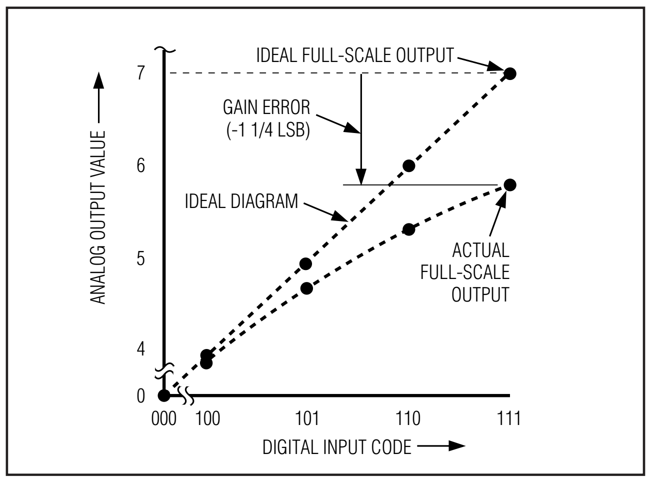


Figure 5d. Gain Error

The I/Q reconstruction system is completed by a quadrature modulator that combines the reconstructed components with in-phase and quadrature carrier frequencies and then sums both outputs to provide the QAM signal.

Using the MAX5181/MAX5184 for Arbitrary Waveform Generation

Designing a traditional arbitrary waveform generator (AWG) requires five major functional blocks (Figure 8a): clock generator, counter, waveform memory, DAC for waveform reconstruction, and output filter. The waveform memory contains the sequentially stored digital replica of the desired analog waveforms. This memory shares a common clock with the DAC.

For each clock cycle, a counter adds one count to the address for the waveform memory. The memory then loads the next value to the DAC, which generates an analog output voltage corresponding to that data value. A DAC output filter can either be a simple or complex lowpass filter, depending on the AWG requirements for waveform function and frequencies. The main limitations of the AWG's flexibility are DAC resolution and dynamic performance, memory length, clock frequency, and the filter characteristics.

Although the MAX5181/MAX5184 offer high-frequency operation and excellent dynamics, they are suitable for relaxed requirements in resolution (10-bit AWGs). To increase an AWG's high-frequency accuracy, tempera-

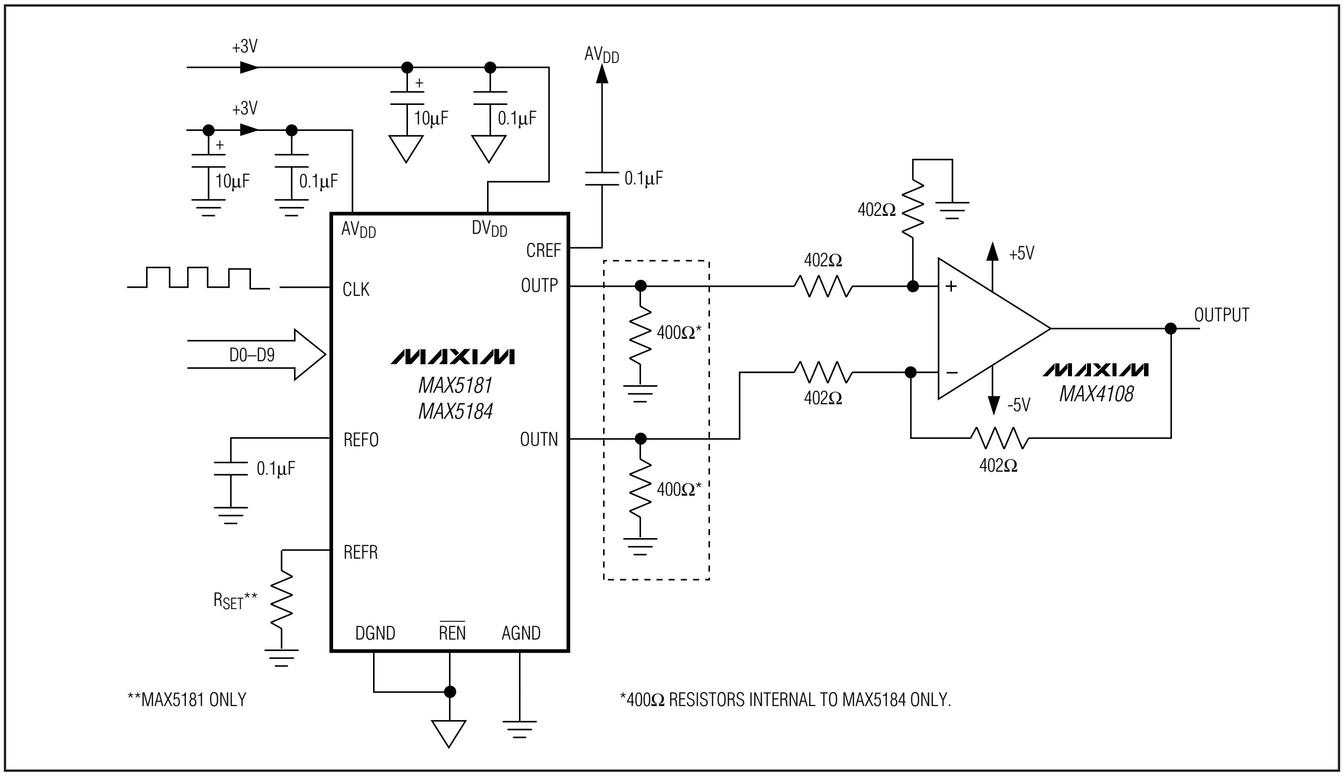


Figure 6. Differential to Single-Ended Conversion Using a Low-Distortion Amplifier

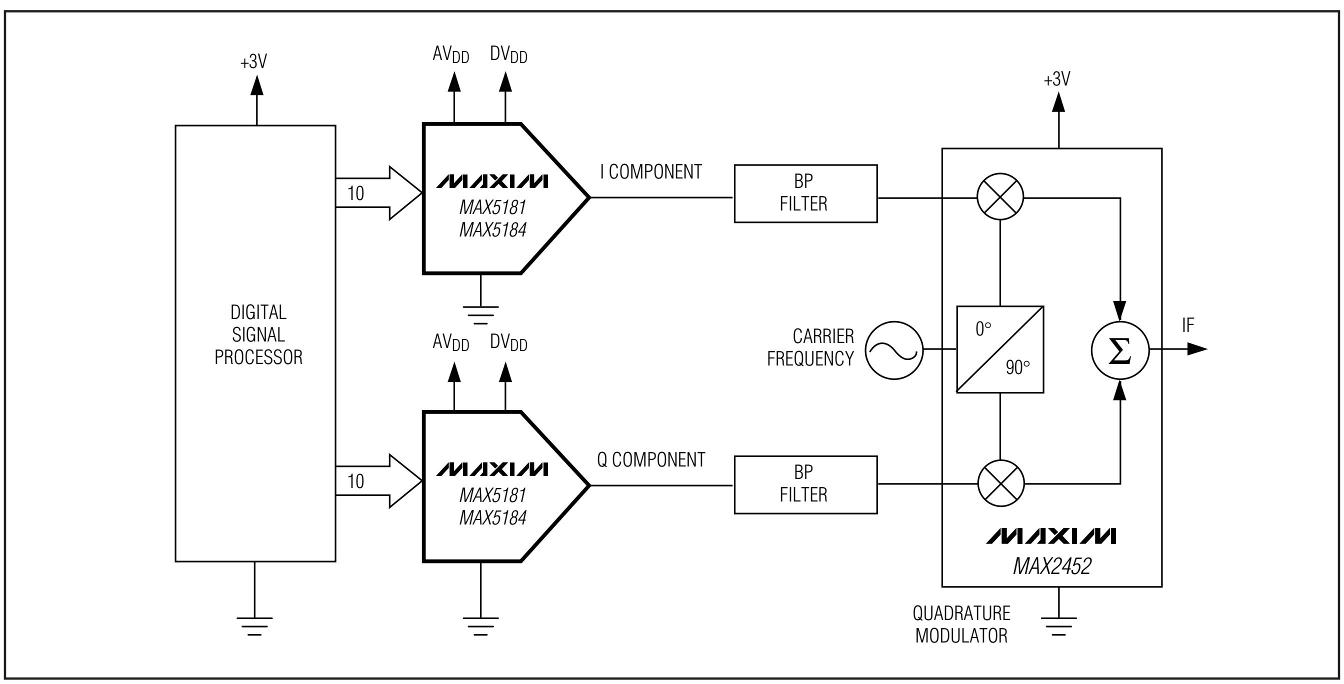


Figure 7. Using the MAX5181/MAX5184 for I/Q Signal Reconstruction

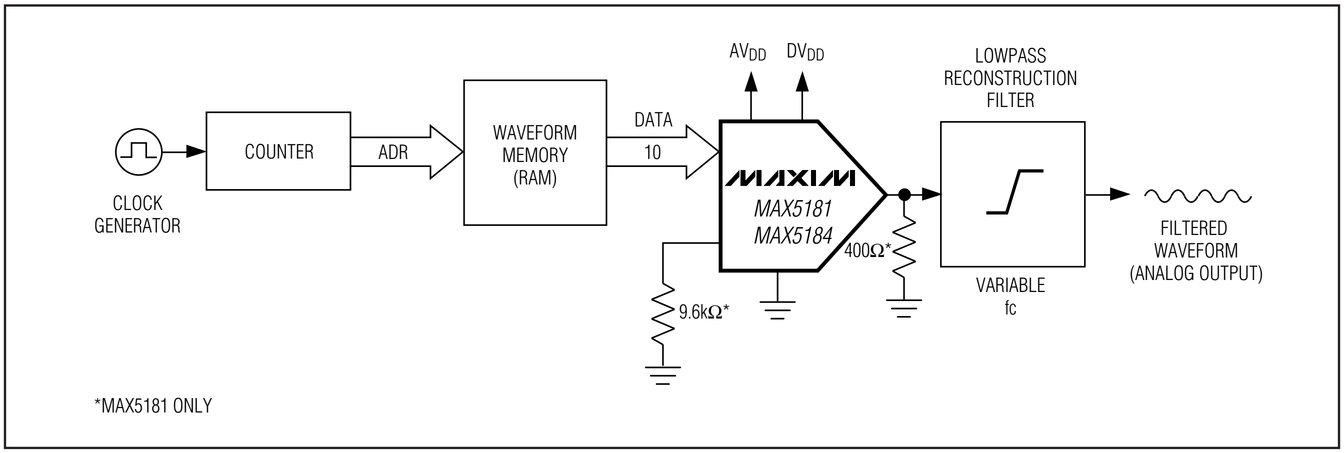


Figure 8a. Traditional Arbitrary Waveform Generation

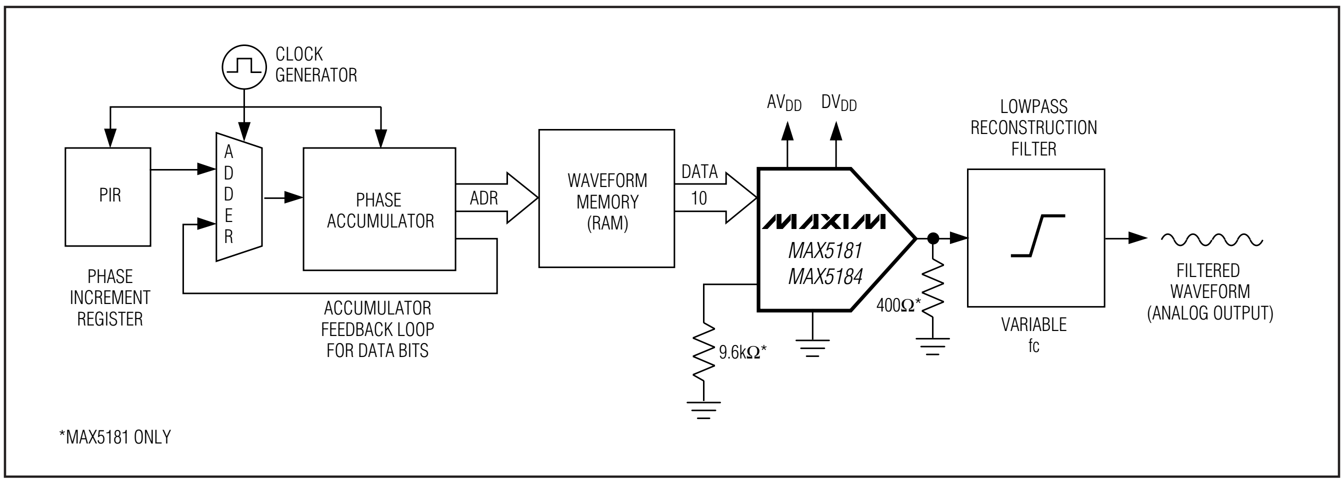


Figure 8b. Direct Digital Synthesis AWG

ture stability, wide-band tuning, and past phase-continuos frequency switching, the user may approach a direct digital synthesis (DDS) AWG (Figure 8b). This DDS loop supports standard waveforms that are repetitive, such as sine, square, TTL, and triangular waveforms. DDS allows for precise control of the data-stream input to the DAC. Data for one complete output waveform cycle is sequentially stored in a RAM. As the RAM addresses are changing, the DAC converts the incoming data bits into a corresponding voltage waveform. The resulting output signal frequency is proportional to the frequency rate at which the RAM addresses are changed.

Grounding and Power-Supply Decoupling

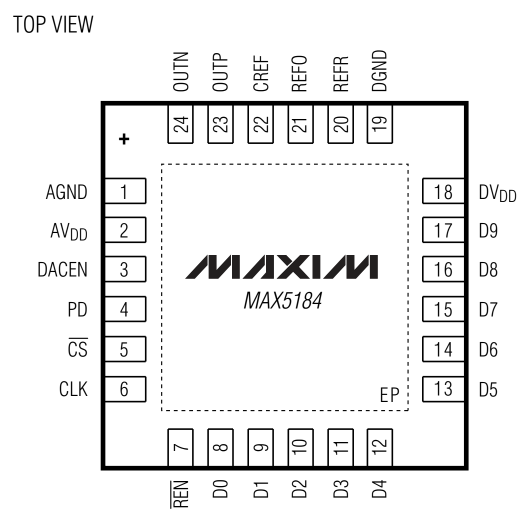
Grounding and power-supply decoupling strongly influence the MAX5181/MAX5184's performance. Unwanted digital crosstalk may couple through the input, reference, power-supply, and ground connections, which may affect dynamic specifications like SNR or SFDR. In addition, electromagnetic interference (EMI) can either couple into or be generated by the MAX5181/ MAX5184. Therefore, grounding and power-supply decoupling guidelines for high-speed, high-frequency applications should be closely followed.

First, a multilayer PC board with separate ground and power-supply planes is recommended. High-speed signals should be run on controlled impedance lines directly above the ground plane. Since the MAX5181/MAX5184 have separate analog and digital ground buses (AGND and DGND, respectively), the PC board should also have separate analog and digital ground sections with only one point connecting the two. Digital signals should run above the digital ground plane, and analog signals should run above the analog ground plane.

Both devices have two power-supply inputs: analog V_{DD} (AV_{DD}) and digital V_{DD} (DV_{DD}). Each AV_{DD} input should be decoupled with parallel 10µF and 0.1µF ceramic-chip capacitors. These capacitors should be as close to the pin as possible, and their opposite ends should be as close as possible to the ground plane. The DV_{DD} pins should also have separate 10µF and 0.1µF capacitors adjacent to their respective pins. Try to minimize analog load capacitance for proper operation. For best performance, bypass with low-ESR 0.1µF capacitors to AV_{DD}.

The power-supply voltages should also be decoupled with large tantalum or electrolytic capacitors at the point they enter the PC board. Ferrite beads with additional decoupling capacitors forming a pi network can also improve performance.

Pin Configurations (continued)



TQFN-EP

Chip Information

SUBSTRATE CONNECTED TO AGND

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO
24 QSOP	E24+1	**21-0055**	**90-0172**
24 TQFN	T2444+4	**21-0139**	**90-0222**

10-Bit, 40MHz, Current/Voltage-Output DACs

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	4/03	—	—
5	8/10	Added lead-free and automotive qualified parts to *Ordering Information*	1