- **1.0-to 1.6-Gigabits Per Second (Gbps) Serializer/Deserializer**
- **Low Power Consumption < 250 mW at 1.25 Gbps**
- **PECL Compatible Differential I/O on High-Speed Interface**
- **Single Monolithic PLL Design**
- **Support for 10-Bit Interface (TBI) or Reduced Interface 5-Bit Double Data Rate (DDR) Clocking**
- **Receiver Differential Input Thresholds 200 mV Minimum**
- **IEEE 802.3 (Gigabit Ethernet) Compliant**
- **Advanced 0.25-μm CMOS Technology**
- **Interfaces to Backplane, Copper Cables, or Optical Modules**
- **No External Filter Capacitors Required**
- **Comprehensive Suite of Built-In Testability**
- **IEEE 1149.1 JTAG Support**
- **2.5-V Supply for Lowest Power Operation**
- **3.3-V Tolerant on TTL Inputs**
- **Hot Plug Protection**
- **ESD Protection 2-kV HBM**
- **5 mm × 5 mm Footprint Removes Space Limitations With Small Form-Factor MicroStar Junior™ BGA Packaging**

description

The TLK2201AJR is a member of the transceiver family of multigigabit transceivers, optimized for use with small form-factor optical transceivers that require footprints smaller than 14 mm. The TLK2201AJR gigabit ethernet transceiver is fully compliant with IEEE 802.3 requirements for serializer/deserializer functions at 1.25 Gbps. The TLK2201AJR supports a wide range of serial data rates from 1.0 Gbps to 1.6 Gbps.

The primary application of this device is to provide building blocks for point-to-point baseband data transmission over controlled impedance media of 50 Ω or 75 Ω. The transmission media can be printed-circuit board traces, copper cables, or fiber-optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

	A	B	C	D	E	F	G	H	J	
9	RD1	RD2	RD3	RD4	RD5	RD6	RD7	RD8	RD9	9
8	RD0	VDD	VDD	JTMS	JTRSTN	JTDI	VDD	VDD	SYNC/PASS	8
7	RXN	VDDA	GNDA	GNDA	GND	GND	GND	RBC MODE	RBC0	7
6	RXP	VDDA	GNDA	GNDA	GND	GND	GND	TEST EN	RBC1	6
5	LOS	VDDA	GNDA	GNDA	GNDA	GND	GND	JTCLK	JTDO	5
4	TXN	VDDA	GND	GND	GND	GND	GND	PRBS EN	SYNC EN	4
3	TXP	VDD PLL	Open	GND	GND	GND	GND	MODE SEL	REF CLK	3
2	TD0	VDD	VDD	VDD	VDD	ENABLE	VDD	VDD	LOOP EN	2
1	TD1	TD2	TD3	TD4	TD5	TD6	TD7	TD8	TD9	1
	A	B	C	D	E	F	G	H	J	

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

MicroStar Junior is a trademark of Texas Instruments.

description (continued)

The TLK2201AJR performs the data serialization, deserialization, and clock extraction functions for a physical layer interface device. The transceiver operates at 1.25 Gbps (typical), providing up to 1.0 Gbps of data bandwidth over a copper or optical media interface.

The TLK2201AJR supports both the defined 10-bit interface (TBI) and a reduced 5-bit interface with double data rate (DDR) clocking. In the TBI mode the serializer/deserializer (serdes) accepts 10-bit wide 8-bit/10-bit (8b/10b) parallel encoded data bytes. The parallel data bytes are serialized and transmitted differentially at PECL compatible voltage levels. The serdes extracts clock information from the input serial stream and deserializes the data, outputting a parallel 10-bit data byte.

In the DDR mode the parallel interface accepts 5-bit wide 8-bit/10-bit encoded data aligned to both the rising and falling edge of the reference clock. The data is clocked most significant bit first (i.e., bits 0−4 of the 8-bit/10-bit encoded data) on the rising edge of the clock, and the least significant bits (i.e., bits 5−9 of the 8-bit/10-bit encoded data) are clocked on the falling edge of the clock.

The transceiver automatically locks onto incoming data without the need to prelock.

The TLK2201AJR provides a comprehensive series of built-in tests for self-test purposes including loopback and PRBS generation and verification. An IEEE 1149.1 JTAG port is also supported.

The TLK2201AJR is housed in a high-performance, thermally enhanced, 80-pin land grid array (LGA) MicroStarJr package. Use of the MicroStarJr™ package does not require any special considerations. All ac performance specifications in this data sheet are measured with the MicroStarJr™ soldered to the test board.

The TLK2201AJR is characterized for operation from 0°C to 70°C.

The TLK2201AJR uses a 2.5-V supply. The I/O section is 3.3-V compatible. With the 2.5-V supply the chipset is very power efficient dissipating less than 250 mW typical power when operating at 1.25 Gbps.

The TLK2201AJR is designed to be hot plug capable. A power-on reset holds RCB0 and RCB1 low. The parallel side output pins, TXP and TXN go to high-impedance during power up.

differences between TLK2201AJR and TNETE2201

The TLK2201AJR is a functional equivalent of the TNETE2201B. There are several differences between the two devices as noted below.

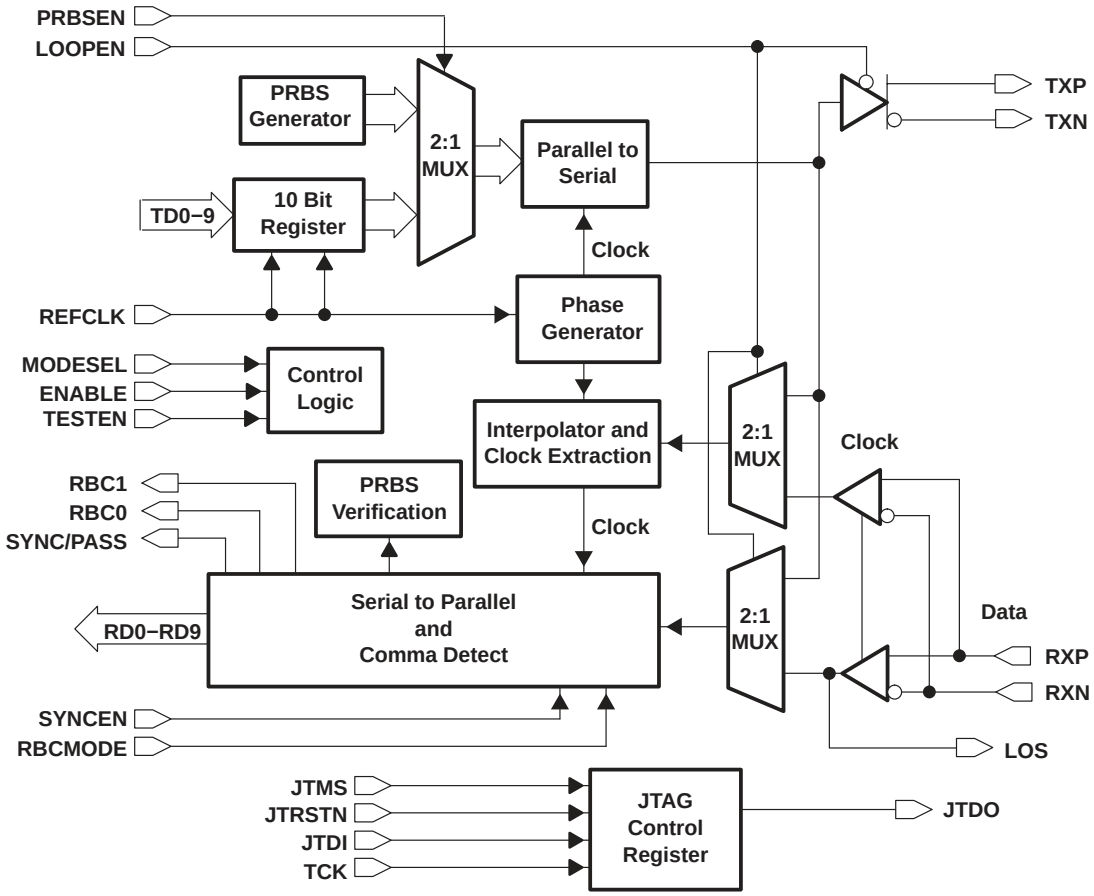
- The V_{CC} is 2.5 V for the TLK2201AJR versus 3.3 V for TNETE2201.
- The PLL filter capacitors on pins 16, 17, 48, and 49 of the TNETE2201 are no longer required.
- No pulldown resistors are required on the TXP/TXN outputs.

transceiver family

The TLK2201AJR is a member of the transceiver family of CMOS multigigabit transceivers intended for use in high-speed bidirectional point-to-point data transmission systems. Other members of the the transceiver family include:

- **TLK1501** − A 0.6-Gbps to 1.5-Gbps transceiver with on-chip 8-bit/10-bit ENDEC providing up to 1.28 Gbps of data bandwidth, packaged in a 64-pin VQFP PowerPAD™ package.
- **TLK2500/TLK2501** − A 1.6-Gbps to 2.5-Gbps transceiver with on-chip 8-bit/10-bit ENDEC, providing up to 2 Gbps of data bandwidth, packaged in a 64-pin VQFP PowerPAD package.
- **TLK2701** − A 2.5-Gbps to 2.7-Gbps transceiver with on-chip 8-bit/10-bit ENDEC, providing up to 2.16 Gbps of data bandwidth with k-character control, packaged in a 64-pin VQFP PowerPAD package.
- **TLK3101** − A 2.5-Gbps to 3.125-Gbps transceiver with on-chip 8-bit/10-bit ENDEC, providing up to 2.5 Gbps of data bandwidth, packaged in a 64-pin VQFP PowerPAD package.
- **TLK3104SC** − A 3-Gbps to 3.125-Gbps quad transceiver with on-chip 8-bit/10-bit ENDEC and a 16-bit low voltage differential signaling (LVDS) parallel interface, packaged in 289 pin PBGA.
- **TLK3104SA** − A 3-Gbps to 3.125-Gbps quad transceiver with on-chip 8-bit/10-bit ENDEC, an IEEE 802.3ae defined XGMII parallel interface with SSTL_2 I/O, packaged in 289 pin PBGA.

functional block diagram



PowerPAD is a trademark of Texas Instruments.

detailed description

data transmission

The TLK2201AJR supports both the defined 10-bit interface (TBI) and a reduced 5-bit interface with DDR clocking. When MODESEL is low, the TBI mode is selected. When MODESEL is high, the DDR mode is selected.

In the TBI mode, the transmitter portion registers incoming 10-bit wide data words (8b/10b encoded data, TD0−TD9) on the rising edge of REFCLK. The REFCLK is also used by the serializer, which multiplies the clock by a factor of 10, providing a signal that is fed to the shift register. The 8b/10b encoded data is transmitted sequentially bit 0 through 9 over the differential high-speed I/O channel.

In the DDR mode, the transmitter accepts 5-bit wide 8-b/10-b encoded data on pins TD0−TD4. In this mode data is aligned to both the rising and falling edges of REFCLK. The data is then formed into a 10-bit wide word and sent to the serializer. The data is clocked most significant bit first (i.e. the bits 0−4 of the 8-b/10-b encoded data).

transmission latency

The data transmission latency of the TLK2201AJR is defined as the delay from the initial 10-bit word load to the serial transmission of bit 9. The minimum latency in TBI mode is 19 bit times. The maximum latency in TBI mode is 20 bit times. The minimum latency in DDR mode is 29 bit times, and maximum latency in DDR mode is 30 bit times.

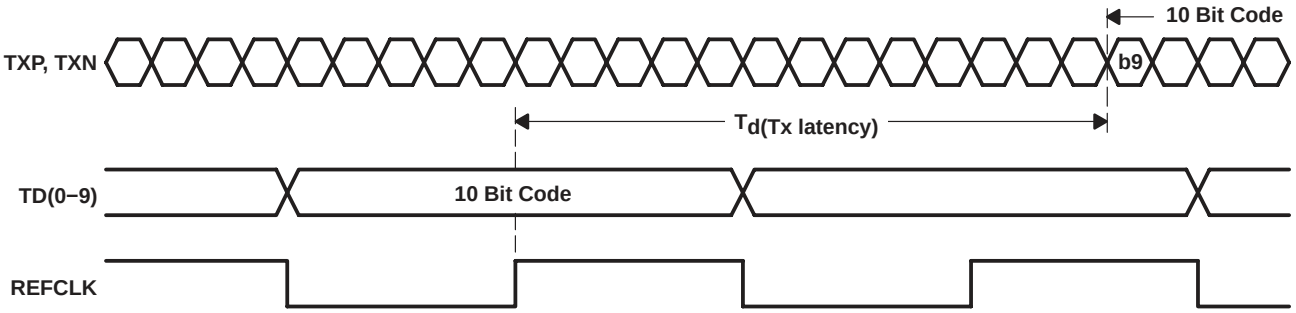


Figure 1. Transmitter Latency Full Rate Mode

data reception

The receiver portion of the TLK2201AJR deserializes the differential serial data. The serial data is retimed based on an interpolated clock generated from the reference clock. The serial data is then aligned to the 10-bit word boundaries and presented to the protocol controller along with receive byte clocks (RBC0, RBC1).

detailed description (continued)

receiver clock select mode

The TLK2201AJR provides two modes of operation for the parallel busses. 1)The 10-bit (TBI) mode and 2) 5-bit (DDR) mode. When in TBI mode, there are two user-selectable clock modes that are controlled by the RBCMODE pin:1) Full-rate clock on RBC0 and 2) Half-rate clocks on RBC0 and RBC1. When in the DDR mode, only a full-rate clock is available on RBC0. Table 1 shows the mode selection.

Table 1. Mode Selection

MODESEL	RBCMODE	MODE	FREQUENCY
0	0	TBI half-rate	100−125 MHz
0	1	TBI full-rate	100−160 MHz
1	0	DDR	100−125 MHz
1	1	DDR	100−125 MHz

In the half-rate mode, two receive byte clocks (RBC0 and RBC1) are 180 degrees out of phase and operate at one-half the data rate. The clocks are generated by dividing down the recovered clock. The received data is output with respect to the two receive byte clocks (RBC0, RBC1), allowing a protocol device to clock the parallel bytes using the RBC0 and RBC1 rising edges. The TLK2201AJR outputs to the protocol device. Byte 0 of the received data is valid on the rising edge of RBC1. Figure 2 shows the timing diagram.

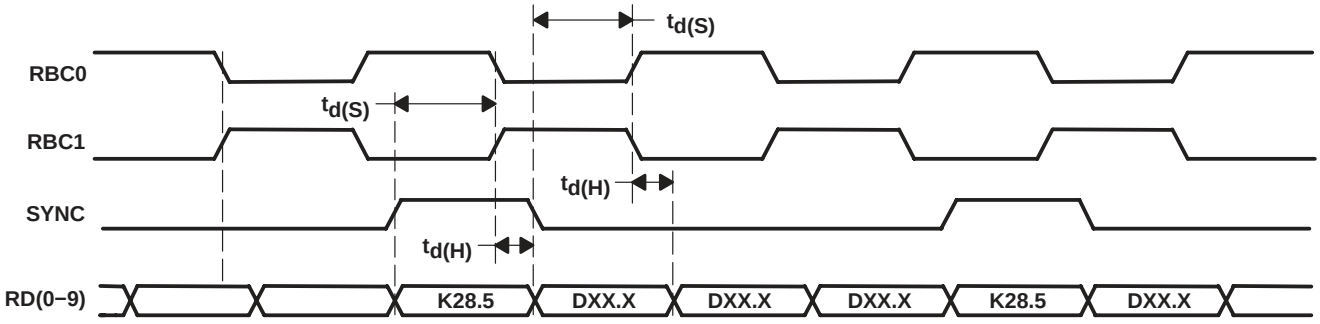


Figure 2. Synchronous Timing Characteristics Waveforms (TBI Half-Rate Mode)

In the normal-rate mode, only RBC0 is used, and it operates at full data rate (i.e., 1.25-Gbps data rate produces a 125-MHz clock). The received data is output with respect to the rising edge of RBC0. RBC1 is low in this mode. Figure 3 shows the synchronous timing characteristics waveforms (TBI full-rate mode).

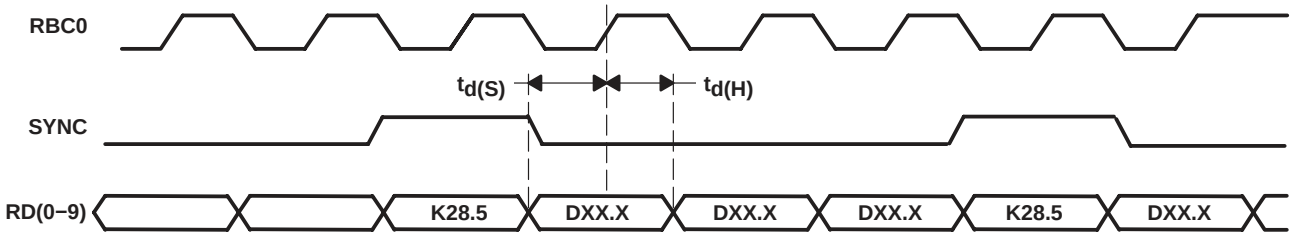


Figure 3. Synchronous Timing Characteristics Waveforms (TBI Full-Rate Mode)

In the double data rate mode, the receiver presents the data on both the rising and falling edges of RBC0. RBC1 is low impedance. The data is clocked bit-0 first, and aligned to the rising edge of RBC0. Figure 4 shows the synchronous timing characteristics waveforms (DDR mode).

receiver clock select mode (continued)

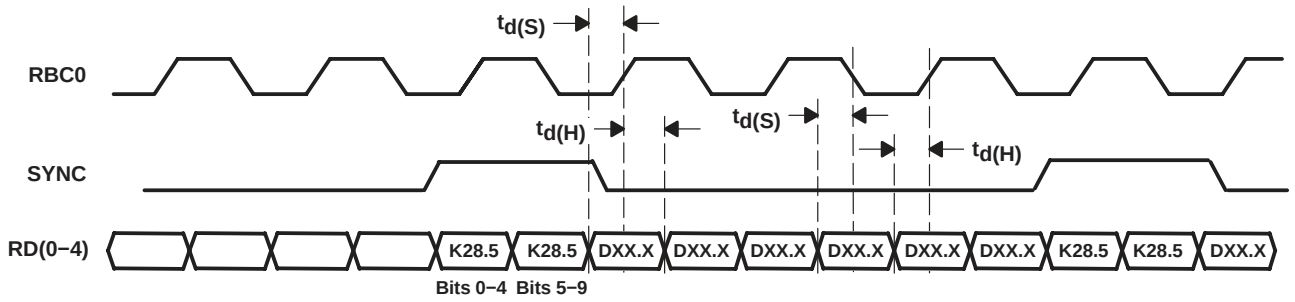


Figure 4. Synchronous Timing Characteristics Waveforms (DDR Mode)

The receiver clock interpolator can lock to the incoming data without the need for a lock-to-reference preset. The received serial data rate (RXP and RXN) must be at the same baud rate as the transmitted data stream, ±0.02% (200 PPM) for proper operation (see page 11).

receiver word alignment

The TLK2201AJR uses the IEEE 802.3 Gigabit Ethernet defined 10-bit K28.5 character (comma character) word alignment scheme. The following sections explain how this scheme works and how it realigns itself.

comma character on expected boundary

The TLK2201AJR provides 10-bit K28.5 character recognition and word alignment. The 10-bit word alignment is enabled by forcing the SYNCEN terminal high. This enables the function that examines and compares serial input data to the seven-bit synchronization pattern. The K28.5 character is defined by 8-bit/10-bit coding scheme as a pattern consisting of 0011111010 (a negative number beginning with disparity) with the 7 MSBs (0011111) referred to as the comma character. The K28.5 character was implemented specifically for aligning data words. As long as the K28.5 character falls within the expected 10-bit boundary, the received 10-bit data is properly aligned and data realignment is not required. Figure 2 shows the timing characteristics of RBC0, RBC1, SYNC, and RD0−RD9 while synchronized. (Note: the K28.5 character is valid on the rising edge of RBC1).

comma character not on expected boundary

If synchronization is enabled and a K28.5 character straddles the expected 10-bit word boundary, then word realignment is necessary. Realignment or shifting the 10-bit word boundary truncates the character following the misaligned K28.5, but the following K28.5 and all subsequent data is aligned properly as shown in Figure 5. The RBC0 and RBC1 pulse width is stretched or stalled in their current state during realignment. With this design the maximum stretch that occurs is 20 bit times. This occurs during a worst case scenario when the K28.5 is aligned to the falling edge of RBC1 instead of the rising edge. Figure 5 shows the timing characteristics of the data realignment.

comma character not on expected boundary (continued)

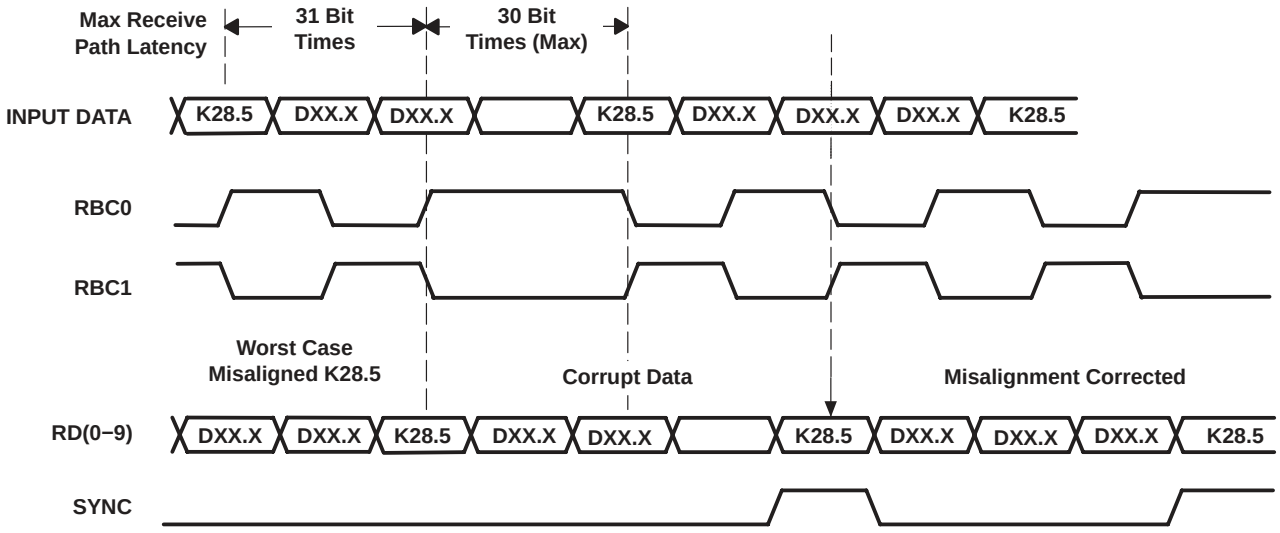


Figure 5. Word Realignment Timing Characteristics Waveforms

Systems that do not require framed data may disable byte alignment by tying SYNCEN low.

When a SYNC character is detected, the SYNC signal is brought high and is aligned with the K28.5 character. The duration of the SYNC pulse is equal to the duration of the data when in TBI mode. When in DDR mode, the SYNC pulse is present for the entire RBC0 period.

data reception latency

The serial to parallel data latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word with RD0 received as first bit. The minimum latency in TBI mode is 22 bit times and the maximum latency is 31 bit times. The minimum latency in DDR mode is 28 bit times and maximum latency is 34 bit times.

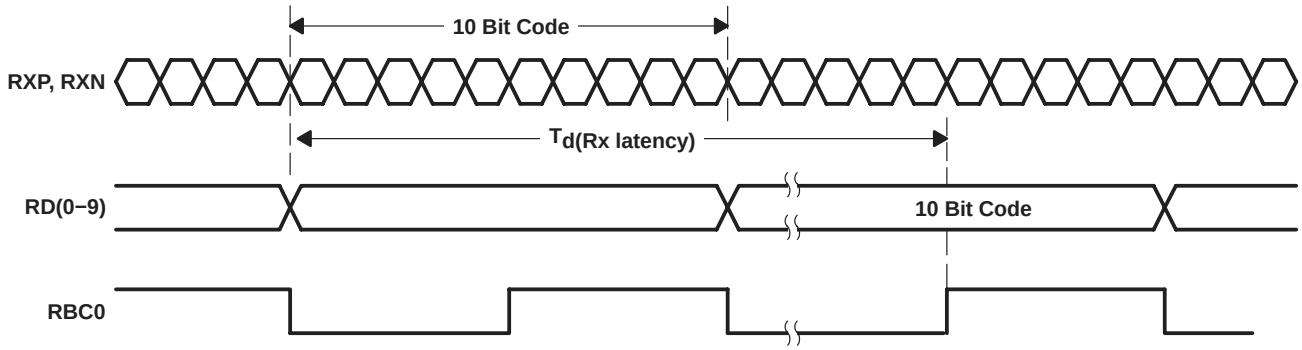


Figure 6. Receiver Latency-TBI Normal Mode Shown

loss of signal detection

The TLK2201AJR has a loss of signal (LOS) detection circuit for conditions where the incoming signal no longer has sufficient voltage level to keep the clock recovery circuit in lock. The LOS is intended to be an indication of gross signal error conditions, such as a detached cable or no signal being transmitted, and not an indication of signal coding health. Under a PRBS serial input pattern, LOS is high for signal amplitudes greater than 150 mV. The LOS is low for all amplitudes below 50 mV. Between 50 mV and 150 mV, LOS is undetermined.

detailed description (continued)

testability

The loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The enable function allows for all circuitry to be disabled so that an Iddq test can be performed. The PRBS function also allows for a BIST(built-in self test). The terminal setting, TESTEN high, enables the test mode. The terminal TESTEN has an internal pulldown resistor, so it defaults to normal operation. The TESTEN is only used for factory testing, and is not intended for the end-user.

loopback testing

The transceiver can provide a self-test function by enabling (LOOPEN to high level) the internal loopback path. Enabling this function cause serial transmitted data to be routed internally to the receiver. The parallel data output can be compared to the parallel input data for functional verification. (The external differential output is held in a high-impedance state during the loopback testing.)

enable function

When held low, enable disables all quiescent power in both the analog and digital circuitry. This allows an ultralow-power idle state when the link is not active.

PRBS function

The TLK2201AJR has a built-in 2^7-1 PRBS function. When the PRBSEN control bit is set high, the PRBS test is enabled. A PRBS is generated and fed into the 10-bit parallel transmitter input bus. Data from the normal parallel input source is ignored during PRBS test mode. The PBRS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a (BERT) bit error rate tester or to the receiver of another TLK2201AJR. Since the PRBS is not really random and is really a predetermined sequence of ones and zeros, the data can be captured and checked for errors by a BERT. The TLK2201AJR also has a built-in BERT function on the receiver side that is enabled by PRBSEN. It can receive a PRBS pattern and check for errors, and then reports the errors by forcing the SYNC/PASS terminal low. When PRBS is enabled, RBCMODE is ignored. MODESEL must be low for the PRBS verifier to function correctly. The PRBS testing supports two modes (normal and latched), which are controlled by the SYNC enable input. When SYNCEN is low, the result of the PRBS bit error rate test is passed to the SYNC/PASS terminal. When SYNCEN is high the result of the PRBS verification is latched on the SYNC/PASS output (i.e., a single failure forces SYNC/PASS to remain low).

Terminal Functions

TERMINAL NAME	TERMINAL NO. GQE	TERMINAL NO. RCP†	I/O	DESCRIPTION
SIGNAL				
TXP TXN	A3 A4	62 61	PECL O	Differential output transmit. TXP and TXN are differential serial outputs that interface to a copper or an optical I/F module. TXP and TXN are put in a high-impedance state when LOOPEN is high and are active when LOOPEN is low.
RXP RXN	A6 A7	54 52	PECL I	Differential input receive. RXP and RXN together are the differential serial input interface from a copper or an optical I/F module.
REFCLK	J3	22	I	Reference clock. REFCLK is an external input clock that synchronizes the receiver and transmitter interface (100 MHz to 160 MHz). The transmitter uses this clock to register the input data (TD0−TD9) for serialization. In the TBI mode that data is registered on the rising edge of REFCLK. In the DDR mode, the data is registered on both the rising and falling edges of REFCLK with the most significant bits aligned to the rising edge of REFCLK.
TD0−TD9	A1, A2, B1, C1, D1, E1, F1, G1, H1, J1	2−4, 6−9, 11−13	I	Transmit data. When in the TBI mode (MODESEL = low) these inputs carry 10-bit parallel data output from a protocol device to the transceiver for serialization and transmission. This 10-bit parallel data is clocked into the transceiver on the rising edge of REFCLK and transmitted as a serial stream with TD0 sent as the first bit. When in the DDR mode (MODESEL = high) only TD0−TD4 are valid. The 5-bit parallel data is clocked into the transceiver on the rising and falling edge of REFCLK and transmitted as a serial stream with TD0 sent as the first bit.
RD0−RD9	A8, A9, B9, C9, D9, E9, F9, G9, H9, J9	45, 44, 43, 41, 40, 39, 38, 36, 35, 34	O	Receive data. When in TBI mode (MODESEL = low) these outputs carry 10-bit parallel data output from the transceiver to the protocol layer. The data is referenced to terminals RBC0 and RBC1, depending on the receive clock mode selected. RD0 is the first bit received. When in the DDR mode (MODESEL = high) only RD0−RD4 are valid. RD5−RD9 are held low. The 5-bit parallel data is clocked out of the transceiver on the rising edge of RBC0.
RBC0 RBC1	J7 J6	31 30	O	Receive byte clock. RBC0 and RBC1 are recovered clocks used for synchronizing the 10-bit output data on RD0−RD9. The operation of these clocks dependant upon the receive clock mode selected. In the half-rate mode, the 10-bit output data words are valid on the rising edges of RBC0 and RBC1. These clocks are adjusted to half-word boundaries in conjunction with synchronous detect. The clocks are always expanded during data realignment and never slivered or truncated. RBC0 registers bytes 1 and 3 of received data. RBC1 registers bytes 0 and 2 of received data. In the normal rate mode, only RBC0 is valid and operates at 1/10 the serial data rate. Data is aligned to the rising edge. In the DDR mode, only RBC0 is valid and operates at 1/10 the serial data rate. Data is aligned to both the rising and falling edges.
RBCMODE	H7	32	I P/D‡	Receive clock mode select. When RBCMODE and MODESEL are low, half-rate clocks are output on RBC0 and RBC1. When MODESEL is low and RBCMODE is high, a full baud-rate clock is output on RBC0 and RBC1 is held low. When MODESEL is high, RBCMODE is ignored and a full baud-rate clock is output on RBC0 and RBC1 is held low.
SYNCEN	J4	24	I P/U§	Synchronous function enable. When SYNCEN is asserted high, the internal synchronization function is activated. When this function is enabled, the transceiver detects the K28.5 comma character (0011111 negative beginning disparity) in the serial data stream and realigns data on byte boundaries if required. When SYNCEN is low, serial input data is unframed in RD0−RD9.
SYNC/PASS	J8	47	O	Synchronous detect. The SYNC output is asserted high upon detection of the comma pattern in the serial data path. SYNC pulses are output only when SYNCEN is activated (asserted high). In PRBS test mode (PRBSEN=high), SYNC/PASS outputs the status of the PRBS test results (high=pass).
LOS	A5	26	O	Loss of signal. Indicates a loss of signal on the high-speed differential inputs RXP and RXN. If magnitude of RXP−RXN > 150 mV, LOS = 1, valid input signal If magnitude of RXP−RXN < 150 mV and > 50 mV, LOS is undefined If magnitude of RXP−RXN < 50 mV, LOS = 0, loss of signal

† For cross reference to TLK2201 RCP package only.
‡ P/D = pulldown
§ P/U = pullup

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO. GQE	TERMINAL NO. RCP†	I/O	DESCRIPTION
MODESEL	H3	15	I P/D‡	Mode select. This terminal selects between the 10-bit interface and a reduced 5-bit DDR interface. When low the 10-bit interface (TBI) is selected. When pulled high, the 5-bit DDR mode is selected. The default mode is the TBI.
TEST				
LOOPEN	J2	19	I P/D‡	Loop enable. When LOOPEN is high (active), the internal loop-back path is activated. The transmitted serial data is directly routed to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The TXP and TXN outputs are held in a high-impedance state during the loop-back test. LOOPEN is held low during standard operational state with external serial outputs and inputs active.
JTCLK/TCK	H5	49	I	Test clock. IEEE1149.1 (JTAG)
JTDI	F8	48	I P/U§	Test data input. IEEE1149.1 (JTAG)
JTDO	J5	27	O	Test data output. IEEE1149.1 (JTAG)
JTRSTN	E8	56	I P/U§	Reset signal. IEEE1149.1 (JTAG)
JTMS	D8	55	I P/U§	Test mode select. IEEE1149.1 (JTAG)
ENABLE	F2	28	I P/U§	When this terminal is low, the device is disabled for Iddq testing. RD0−RD9, RBC, TXP, and TXN are high-impedance. The pullup and pulldown resisters on any input are disabled. When ENABLE is high, the device operates normally.
PRBSEN	H4	16	I P/D§	PRBS enable. When PRBSEN is high, the PRBS generation circuitry is enabled. The PRBS verification circuit in the receive side is also enabled. A PRBS signal can be fed to the receive inputs and checked for errors that are reported by the SYNC/PASS terminal indicating low.
TESTEN	H6	17	I P/D‡	Manufacturing test terminal.
POWER				
VDD	B8, C8, G8, H8, B2, C2, D2, E2, G2, H2	5, 10, 20, 23, 29, 37, 42, 50, 63	Supply	Digital logic power. Provides power for all digital circuitry and digital I/O buffers.
VDDA	B7, B6, B5, B4	53, 57, 59, 60	Supply	Analog power. VDDA provides power for the high-speed analog circuits, receiver, and transmitter
VDDPLL	B3	18	Supply	PLL power. Provides power for the PLL circuitry. This terminal requires additional filtering.
GROUND				
GNDA	C7, D7, C6, D6, C5, D5, E5	51,58	Ground	Analog ground. GNDA provides a ground for the high-speed analog circuits, RX and TX.
GND	C4, D3, D4, E3, E4, E6, E7 F3, F4, F5, F6, F7, G3, G4, G5, G6, G7	1, 14, 21, 25, 33, 46	Ground	Digital logic ground. Provides a ground for the logic circuits and digital I/O buffers.
GNDPLL	N/A	64	Ground	PLL ground. Provides a ground for the PLL circuitry. Tied to GNDA in the GQE package.

† For cross reference to TLK2201 RCP package only.
‡ P/D = pulldown
§ P/U = pullup

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 V to 3 V
Input voltage, V_I, (TTL) . . . . . −0.5 V to 4 V
DC input voltage (I/O) . . . . . −0.3 V to 3 V
Voltage range at any terminal . . . . . −0.3 V to V_{CC} +0.3 V
Storage temperature, T_{stg} . . . . . −65°C to 150°C
Electrostatic discharge . . . . . HBM:2 kV, CDM: 1 kV
Characterized free-air operating temperature range . . . . . 0°C to 70°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

DISSIPATION RATING TABLE‡

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
GQE	37.8	4.56	3.3 W

‡ This data was taken using 2 oz. trace and copper pad that is soldered directly to a JEDEC standard
‡ 4-layer, 3-in. x 3-in. PCB.

thermal characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board-mounted, no air flow, high conductivity Texas Instruments recommended test board, chip soldered or greased to thermal land		21.47		°C/W
		Board-mounted, no air flow, high conductivity Texas Instruments recommended test board with thermal land but no solder or grease thermal connection to thermal land		42.20		
		Board-mounted, no air flow, JEDEC test board		75.83		
$R_{\theta JC}$	Junction-to-case-thermal resistance	Board-mounted, no air flow, high conductivity Texas Instruments recommended test board, chip soldered or greased to thermal land		0.38		°C/W
		Board-mounted, no air flow, high conductivity Texas Instruments recommended test board with thermal land but no solder or grease thermal connection to thermal land		0.38		
		Board-mounted, no air flow, JEDEC test board		7.8		

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}, $V_{DD(A)}$			2.3	2.5	2.7	V
Total supply current I_{DD}, $I_{DD(A)}$	Frequency = 1.25 Gbps,	PRBS pattern		80		mA
	Frequency = 1.6 Gbps,	Worst case pattern†			111	
Total power dissipation P_D	Frequency = 1.25 Gbps,	PRBS pattern		190		mW
	Frequency = 1.6 Gbps,	Worst case pattern†			310	
Total shutdown current I_{DD}, $I_{DD(A)}$	Enable = 0,	$V_{DD(A)}$, V_{DD} = 2.7 V			50	µA
Startup lock time, PLL	V_{DD}, $V_{DD(A)}$ = 2.5 V, EN↑ to PLL acquire				500	µs
Operating free-air temperature, T_A			0		70	°C

† Worst case pattern is a pattern that creates a maximum transition density on the serial transceiver.

reference clock (REFCLK) timing requirements over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	Minimum data rate	TYP−0.01%	100	TYP−0.01%	MHz
Frequency	Maximum data rate	TYP−0.01%	160	TYP−0.01%	MHz
Accuracy		−100		100	ppm
Duty cycle		40%	50%	60%	
Jitter	Random plus deterministic			40	ps

TTL electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 µA	2.1	2.3		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	GND	0.25	0.5	V
V_{IH}	High-level input voltage		1.7		3.6	V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	Input high current	V_{DD} = 2.3 V, V_{IN} = 2 V			40	µA
I_{IL}	Input low current	V_{DD} = 2.3 V, V_{IN} = 0.4 V	−40			µA
C_{IN}					4	pf

transmitter/receiver characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Vod = |TxD−TxN|		Rt = 50 Ω	600	850	1100	mV
			Rt = 75 Ω	800	1050	1200	
$V_{(cm)}$	Transmit common mode voltage range		Rt = 50 Ω	1000	1250	1400	mV
			Rt = 75 Ω	1000	1250	1400	
	Receiver Input voltage requirement, Vid = |RxP − RxN|			200		1600	mV
	Receiver common mode voltage range, (RxP + RxN)/2			1000	1250	2250	mV
$I_{lkg(R)}$	Receiver input leakage current			−350		350	µA
C_I	Receiver input capacitance					2	pF
$t_{(TJ)}$	Serial data total jitter (peak-to-peak)		Differential output jitter, Random + deterministic, PRBS pattern, R_ω = 125 MHz			0.24	UI
$t_{(DJ)}$	Serial data deterministic jitter (peak-to-peak)		Differential output jitter, PRBS pattern, R_ω = 125 MHz			0.12	UI
t_r, t_f	Differential signal rise, fall time (20% to 80%)		R_L = 50 Ω, C_L = 5 pF, See Figure 7 and Figure 8	100		250	ps
	Serial data jitter tolerance minimum required eye opening, (per IEEE-802.3 specification)		Differential input jitter, random + determinisitc, PRBS pattern at zero crossing	0.25			UI
	Receiver data acquisition lock time from powerup					500	µs
	Data relock time from loss of synchronization					1024	Bit times
$t_{d(Tx\ latency)}$	Tx latency	TBI modes	See Figure 1	19		20	UI
		DDR mode		29		30	
$t_{d(Rx\ latency)}$	Rx latency	TBI modes (see Figure 6)	1 Gpbs	22		27	UI
			1.25 Gpbs	23		28	
			1.6 Gpbs	25		31	
		DDR mode	1 Gpbs	27		32	UI
			1.25 Gpbs	28		33	
			1.375 Gpbs	30		34	

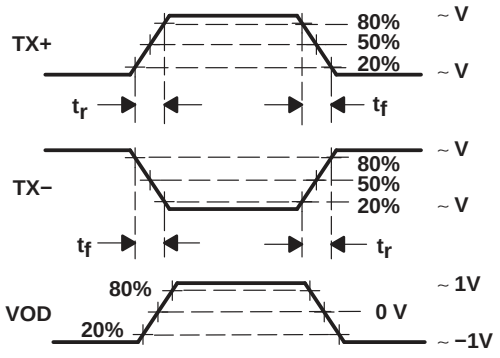


Figure 7. Differential and Common-Mode Output Voltage Definitions

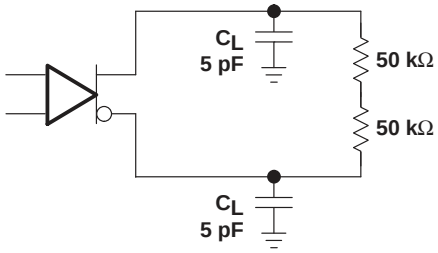


Figure 8. Transmitter Test Setup

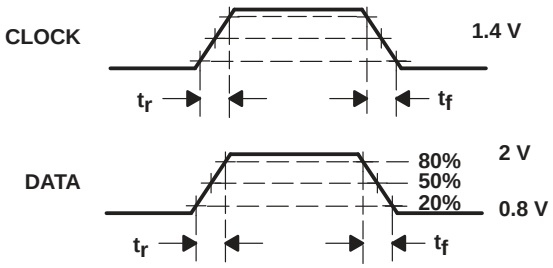


Figure 9. TTL Data I/O Valid Levels for AC Measurement

LVTTL output switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(BRC)}$	Clock rise time	80% to 20% output voltage, C = 5 pF (see Figure 9)	0.3		1.5	ns
$t_{f(RBC)}$	Clock fall time		0.3		1.5	
t_r	Data rise time		0.3		1.5	ns
t_f	Data fall time		0.3		1.5	
$t_{su(D1)}$	Data setup time (RD0..RD9), Data valid prior to RBC0 rising	TBI normal mode, (see Figure 3)	2.5			ns
$t_{h(D1)}$	Data hold time (RD0..RD9), Data valid after RBC0 rising	TBI normal mode, (see Figure 3)	2			ns
$t_{su(D2)}$	Data setup time (RD0..RD4)	DDR mode, R_ω = 125 MHz, (see Figure 4)	2			ns
$t_{h(D2)}$	Data hold time (RD0..RD4)	DDR mode, R_ω = 125 MHz, (see Figure 4)	0.8			ns
$t_{su(D3)}$	Data setup time (RD0..RD9)	TBI half-rate mode, R_ω = 125 MHz, (see Figure 2)	2.5			ns
$t_{h(D3)}$	Data hold time (RD0..RD9)	TBI half-rate mode, R_ω = 125 MHz, (see Figure 2)	1.5			ns

transmitter timing requirements over recommended operating conditions (unless otherwise noted)

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{su(D4)}$	Data setup time (TD0..TD9)	TBI modes	1.6			ns
$t_{h(D4)}$	Data hold time (TD0..TD9)		0.8			
$t_{su(D5)}$	Data setup time (TD0..TD9)	DDR modes	0.7			ns
$t_{h(D5)}$	Data hold time (TD0..TD9)		0.5			
t_r, t_f	TD[0,9] Data rise and fall time	See Figure 9			2	ns

APPLICATION INFORMATION

8B/10B transmission code

The PCS maps GMII signals into 10-bit code groups and vice versa, using an 8b/10b block coding scheme. The PCS uses the transmission code to improve the transmission characteristics of information to be transferred across the link. The encoding defined by the transmission code ensures that sufficient transitions are present in the PHY bit stream to make clock recovery possible in the receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. The 8b/10b transmission code specified for use has a high transition density, is run length limited, and is dc-balanced. The transition density of the 8b/10b symbols range from 3 to 8 transitions per symbol. The definition of the 8b/10b transmission code is specified in IEEE 802.3 Gigabit Ethernet and ANSI X3.230-1994 (FC−PH), clause 11.

8b/10b transmission code uses letter notation describing the bits of an unencoded information octet. The bit notation of ABCDEFGH for an unencoded information octet is used in the description of the 8b/10b transmission code-groups, where A is the LSB. Each valid code group has been given a name using the following convention: /Dx.y/ for the 256 valid data code-groups and /Kx.y/ for the special control code-groups, where y is the decimal value of bits EDCBA and x is the decimal value of bits HGF (noted as K<HGF.EDCBA>). Thus, an octet value of FE representing a code-group value of K30.7 is represented in bit notation as 111 11110.

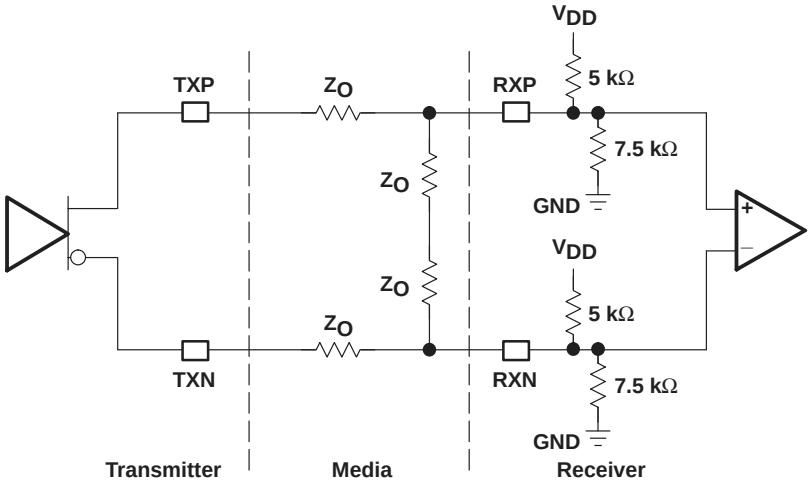


Figure 10. High-Speed I/O Directly-Coupled Mode

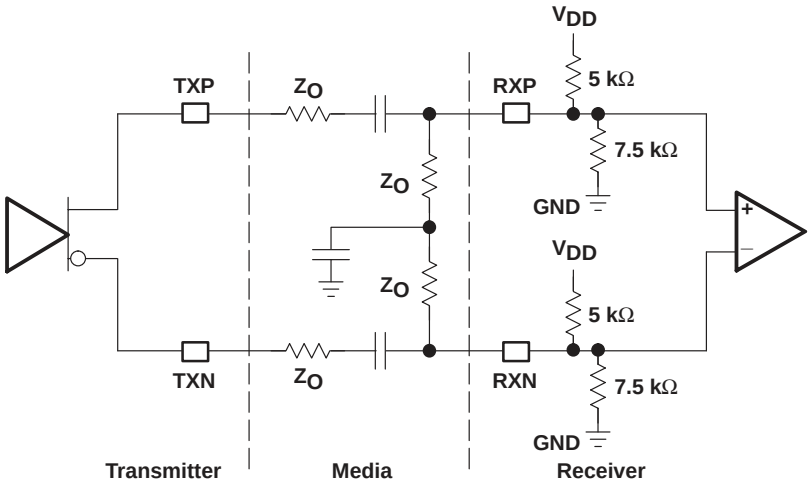


Figure 11. High-Speed I/O AC-Coupled Mode

APPLICATION INFORMATION

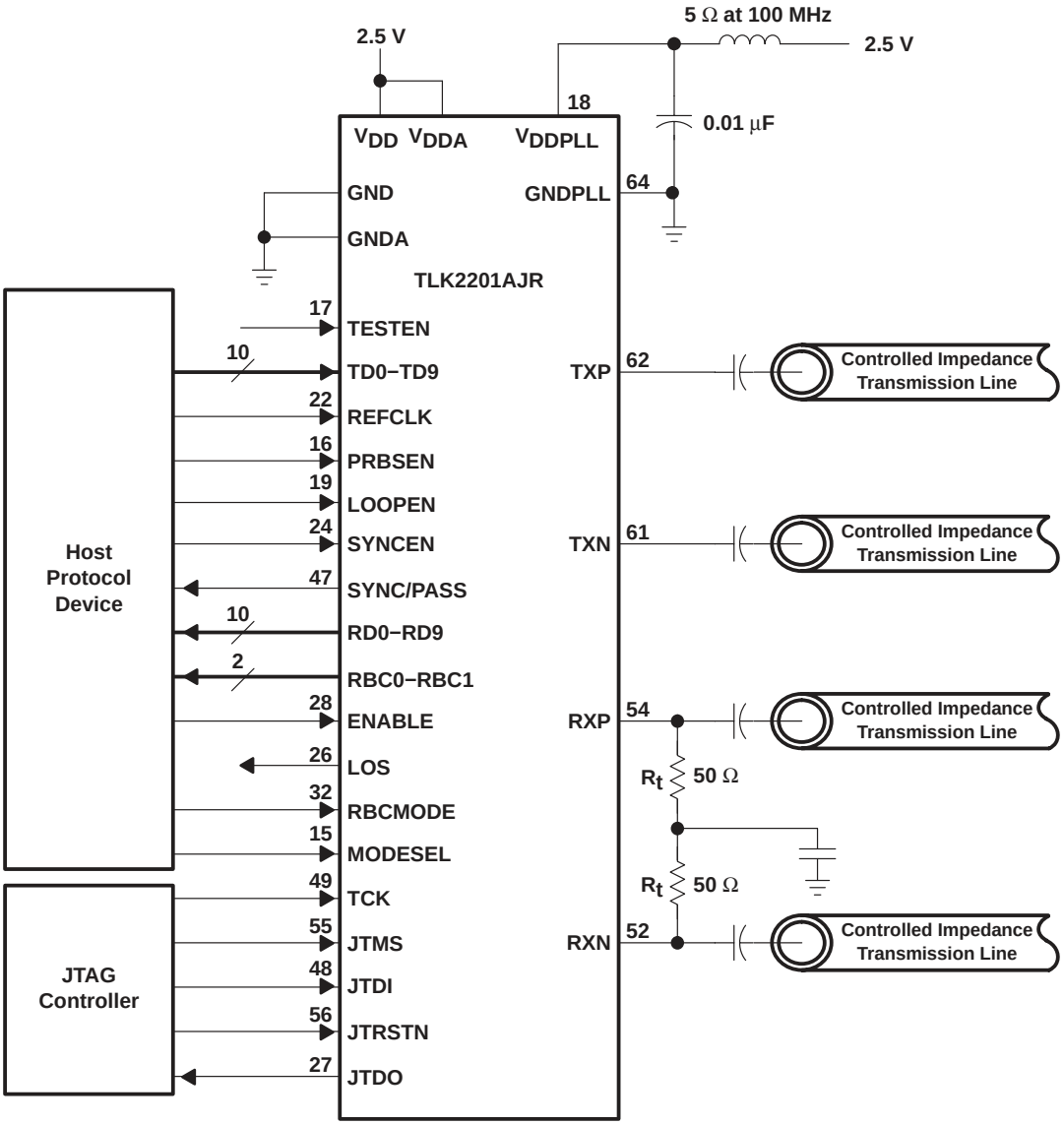


Figure 12. Typical Application Circuit (AC mode)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLK2201AJRGQE	LIFEBUY	BGA MICROSTAR JUNIOR	GQE	80	360	TBD	SNPB	Level-2A-235C-4 WKS	0 to 70	TLK2201A	
TLK2201AJRZQE	LIFEBUY	BGA MICROSTAR JUNIOR	ZQE	80	360	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 70	TLK2201A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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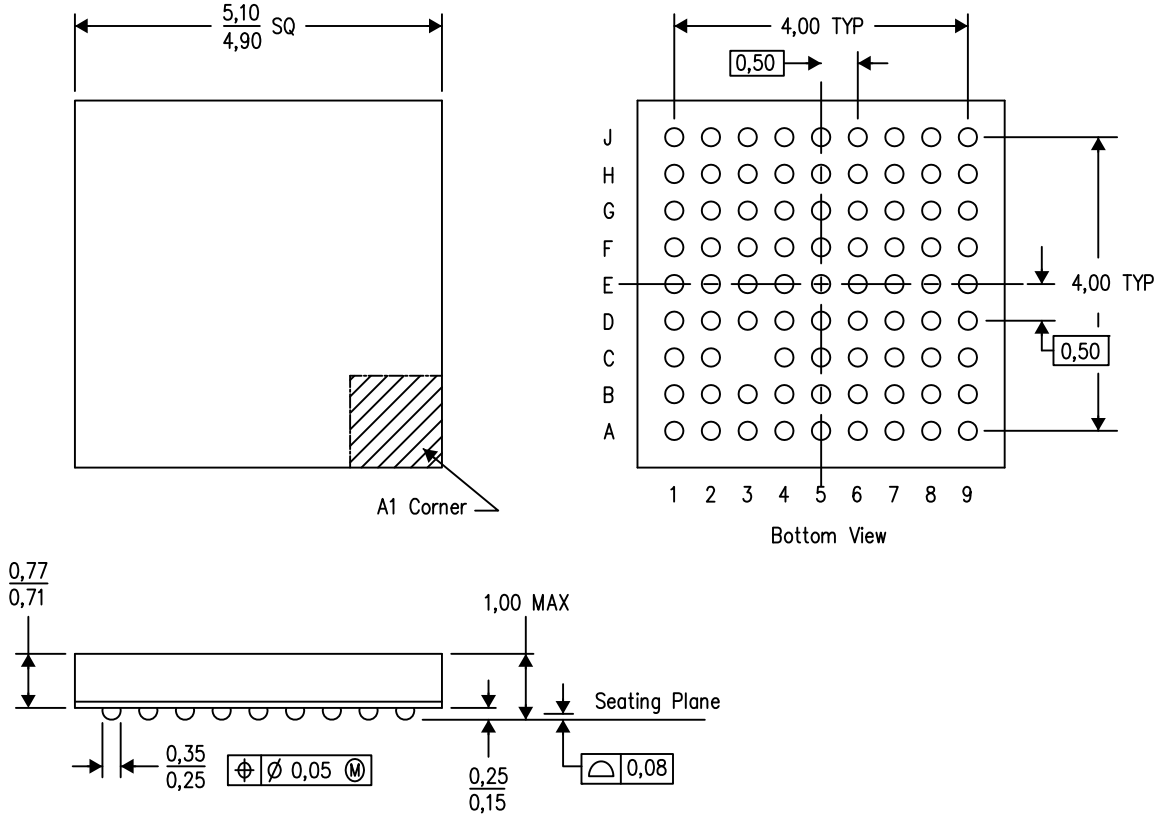
ZQE (S–PBGA–N80) PLASTIC BALL GRID ARRAY



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a Pb–free solder ball design.

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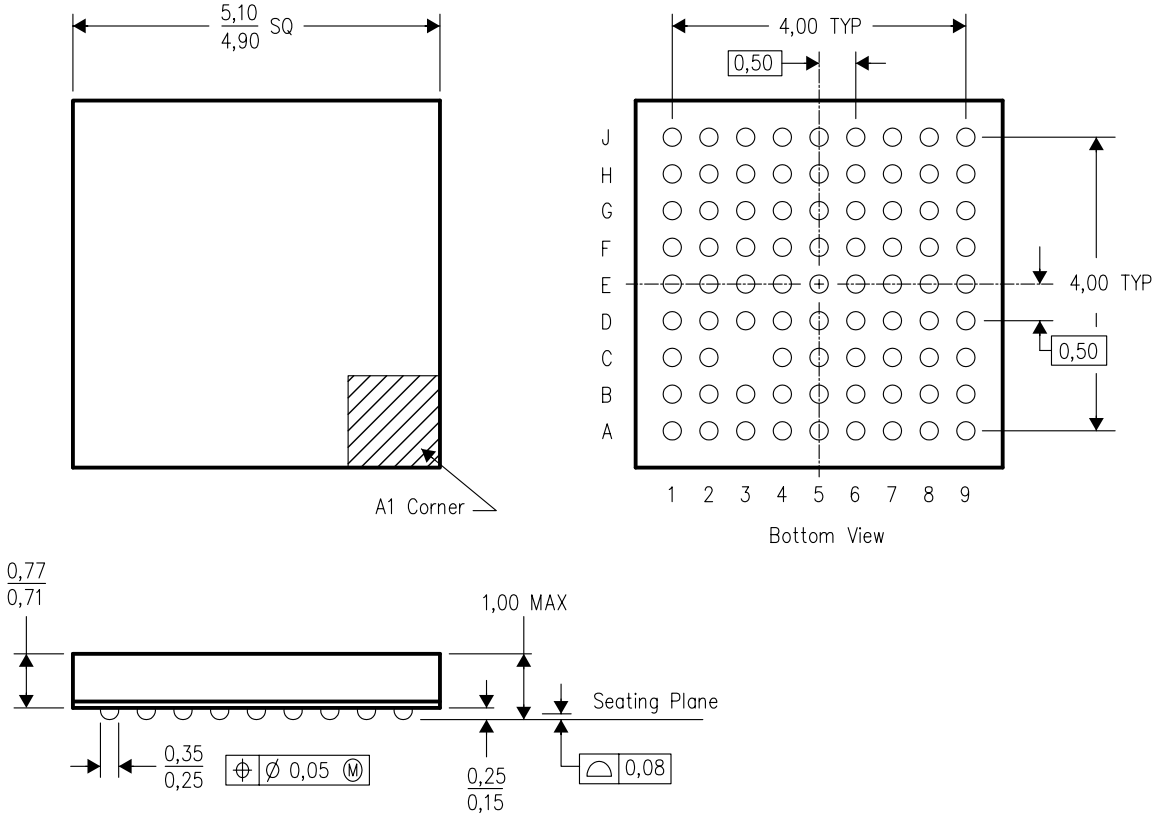
GQE (S–PBGA–N80) PLASTIC BALL GRID ARRAY



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B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225

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