ispMACH® 4000ZE Evaluation Board

User's Guide

February 2009
Revision: EB35_01.2

Introduction

The ispMACH 4000ZE Evaluation Board is a convenient platform for evaluation, testing and development with the Lattice ispMACH 4000ZE CPLD. The board features an ispMACH 4064ZE or ispMACH 4256ZE CPLD in a space-saving 144-ball csBGA package.

A variety of interfaces are provided for device programming, logical input, output/display, and I/O connection. A USB microcontroller and Lattice MachXO™ device implement the logic required for easy programming of the ultra low-power ispMACH 4000ZE CPLD.

A USB connection provides ample power for operation of the ispMACH 4000ZE and all other components on the board. On-board regulators provide the voltages necessary for all components.

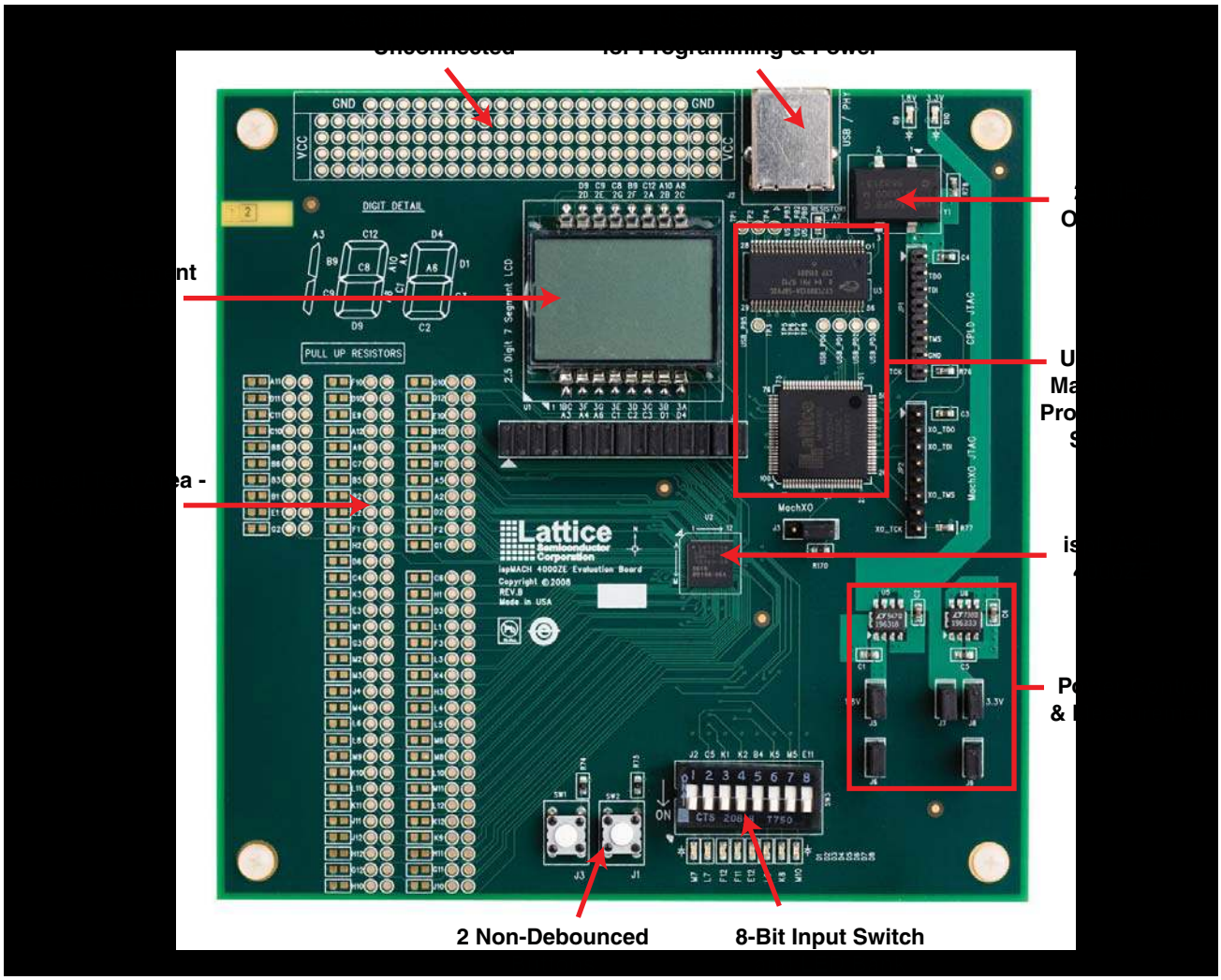
Key Features

- 7-segment LCD
- 8 LEDs
- 8-bit DIP switch
- 2 non-debounced input buttons
- General prototype area
- General test point area
- 24 MHz oscillator
- Jumpers between regulators for power measurement

Also included with this board:

- USB cable for programming

Figure 1. ispMACH 4000ZE Evaluation Board



Additional Resources

Additional resources for this board can be downloaded from the Lattice website at www.latticesemi.com/boards. Navigate to the appropriate evaluation board to find updated documentation, software, sample designs, demos and more. We will continue to add resources to this web page. If you wish to be notified when additional resources are available, click the "Subscribe to Page Update" icon at the top-right side of the screen.

Functional Description

ispMACH 4000ZE CPLD

At the heart of the board is the ispMACH 4000ZE device in a 144-ball csBGA package. Boards are available with either a ispMACH 4064ZE or ispMACH 4256ZE populated CPLD. Table 1 is a summary of all the I/O locations on the device and their connections.

Table 1. ispMACH 4000ZE I/O Locations and Connections

Functional Area	Board Connection	ispMACH 4064ZE		ispMACH 4256ZE		Ball Number	Bank Number
		Function	Pin Name	Function	Pin Name		
7 Segment Display	7SEG_01	I/O	A7	I/O	B8	A3	0
	7SEG_02	I/O	A4	I/O	B2	A4	0
	7SEG_03	I/O	A2	I/O	A6	A6	0
	7SEG_04	I/O	A10	I/O	C4	C1	0
	7SEG_05	I/O	A9	I/O	C6	C2	0
	7SEG_06	I/O	A8	I/O	C8	C3	0
	7SEG_07	I/O	A11	I/O	C2	D1	0
	7SEG_08	I/O	A14	I/O	D4	D4	0
	7SEG_09	I/O	D2	I/O	P6	A8	1
	7SEG_10	I/O	D4	I/O	O0	A10	1
	7SEG_11	I/O	D8	I/O	N8	C12	1
	7SEG_12	I/O	D6	I/O	O4	B9	1
	7SEG_13	I/O	D3	I/O	P8	C8	1
	7SEG_14	I/O	D5	I/O	O2	C9	1
	7SEG_15	I/O	D7	I/O	O6	D9	1
8-bit Input Switch	SW1	I/O	B9	I/O	F6	J2	0
	SW2	I/O	A6	I/O	B6	C5	0
	SW3	I/O	B8	I/O	F8	K1	0
	SW4	Input Only	I	I/O	F10	K2	0
	SW5	I/O	A5	I/O	B4	B4	0
	SW6	I/O	B3	I/O	H8	K5	0
	SW7	I/O	B1	I/O	H4	M5	0
	SW8	I/O	D13	I/O	M4	E11	1
8-bit LED	LED1	I/O	C1	I/O	I4	M7	1
	LED2	I/O	C2	I/O	I6	L7	1
	LED3	I/O	D15	I/O	M0	F12	1
	LED4	I/O	D14	I/O	M2	F11	1
	LED5	I/O	D12	I/O	M6	E12	1
	LED6	I/O	C5	I/O	J4	L9	1
	LED7	I/O	C6	I/O	J6	K8	1
	LED8	I/O	C7	I/O	J8	M10	1
Clock Input	CPLD_CLK	CLK0/I	CLK0/I	CLK0/I	CLK0/I	A7	0
Device Programming	JTAG - JP2	TDI	TDI	TDI	TDI	A1	-
	JTAG - JP2	TDO	TDO	TDO	TDO	B11	-
	JTAG - JP2	TCK	TCK	TCK	TCK	L2	-
	JTAG - JP2	TMS	TMS	TMS	TMS	M12	-
Non-Debounced Push-Button	Button 1	I/O	B11	I/O	F2	J1	0
	Button 2	I/O	B10	I/O	F4	J3	0

Table 1. ispMACH 4000ZE I/O Locations and Connections (Continued)

Functional Area	Board Connection	ispMACH 4064ZE		ispMACH 4256ZE		Ball Number	Bank Number
		Function	Pin Name	Function	Pin Name		
Test Points	TP01	Not Connected	-	I/O	C12	B2	0
	TP02	Not Connected	-	I/O	C10	B1	0
	TP03	Not Connected	-	I/O	D14	D2	0
	TP04	Not Connected	-	I/O	D12	D3	0
	TP05	Not Connected	-	I/O	D10	E1	0
	TP06	I/O	A12	I/O	D8	E2	0
	TP07	I/O	A13	I/O	D6	F2	0
	TP08	I/O	A15	I/O	D2	F1	0
	TP09	Input Only	I	I/O	D0	F3	0
	TP10	I/O	B15	I/O	E0	G1	0
	TP11	I/O	B14	I/O	E2	E3	0
	TP12	I/O	B13	I/O	E4	G2	0
	TP13	I/O	B12	I/O	E6	G3	0
	TP14	Not Connected	-	E8	E8	H1	0
	TP15	Not Connected	-	E10	E10	H3	0
	TP16	Not Connected	-	E12	E12	H2	0
	TP17	Not Connected	-	I/O	F12	L1	0
	TP18	Not Connected	-	I/O	G14	M1	0
	TP19	Not Connected	-	I/O	G12	K3	0
	TP20	Not Connected	-	I/O	G10	M2	0
	TP21	Input Only	I	I/O	G8	L3	0
	TP22	I/O	B7	I/O	G6	J4	0
	TP23	I/O	B6	I/O	G4	K4	0
	TP24	I/O	B5	I/O	G2	M3	0
	TP25	I/O	B4	I/O	G0	L4	0
	TP26	Not Connected	-	I/O	H12	M4	0
	TP27	Not Connected	-	H10	H10	L5	0
	TP28	CLK1/I	CLK1/I	CLK1/I	CLK1/I	L6	0
	TP29	A0/GOE0	A0/GOE0	A2/GOE0	A2/GOE0	D6	0
	TP30	I/O	A1	I/O	A4	B6	0
	TP31	I/O	A3	I/O	A8	C6	0
	TP32	Not Connected	-	I/O	A10	B5	0
	TP33	Not Connected	-	I/O	A12	A5	0
	TP34	Not Connected	-	I/O	B10	C4	0
	TP35	Not Connected	-	I/O	B12	B3	0
	TP36	Not Connected	-	I/O	B14	A2	0
	TP37	CLK2/I	CLK2/I	CLK2/I	CLK2/I	M6	1
	TP38	Not Connected	-	I/O	I10	L8	1
	TP39	Not Connected	-	I/O	I12	M8	1
	TP40	I/O	C4	I/O	J2	M9	1
	TP41	Not Connected	-	I/O	J10	L10	1
	TP42	Not Connected	-	I/O	J12	K9	1
	TP43	Not Connected	-	I/O	J14	M11	1

Table 1. ispMACH 4000ZE I/O Locations and Connections (Continued)

Functional Area	Board Connection	ispMACH 4064ZE		ispMACH 4256ZE		Ball Number	Bank Number
		Function	Pin Name	Function	Pin Name		
Test Points (Cont.)	TP44	Not Connected	-	I/O	K12	L12	1
	TP45	Not Connected	-	I/O	K10	L11	1
	TP46	I/O	C8	I/O	K8	K10	1
	TP47	I/O	C9	I/O	K6	K12	1
	TP48	I/O	C10	I/O	K4	J10	1
	TP49	I/O	C11	I/O	K2	K11	1
	TP50	Not Connected	-	I/O	L14	J12	1
	TP51	Not Connected	-	I/O	L12	J11	1
	TP52	Not Connected	-	I/O	L10	H10	1
	TP53	I/O	C12	I/O	L8	H12	1
	TP54	I/O	C13	I/O	L6	G11	1
	TP55	I/O	C14	I/O	L4	H11	1
	TP56	I/O	C15	I/O	L2	G12	1
	TP57	Input Only	I	I/O	L0	G10	1
	TP58	Not Connected	-	I/O	M8	D10	1
	TP59	Not Connected	-	I/O	M12	D12	1
	TP60	Not Connected	-	I/O	M10	F10	1
	TP61	I/O	D11	I/O	N2	E10	1
	TP62	I/O	D10	I/O	N4	D11	1
	TP63	I/O	D9	I/O	N6	E9	1
	TP64	Input Only	I	I/O	O8	A11	1
	TP65	Input Only	I	I/O	N10	C11	1
	TP66	Not Connected	-	I/O	N12	B12	1
	TP67	Not Connected	-	I/O	O14	A12	1
	TP68	Not Connected	-	I/O	O12	C10	1
	TP69	Not Connected	-	I/O	O10	B10	1
	TP70	Not Connected	-	I/O	P12	A9	1
	TP71	Not Connected	-	I/O	P10	B8	1
	TP72	D0/GOE1	D0/GOE1	P2/GOE1	P2/GOE1	B7	1
	TP73	CLK3/I	CLK3/I	CLK3/I	CLK3/I	C7	1
Unconnected Pins	Not Connected	I/O	D1	I/O	P4	D7	1
	Not Connected	I/O	B2	I/O	H6	J6	0
	Not Connected	I/O	C3	I/O	I8	J7	1
	Not Connected	I/O	B0	I/O	H2	K6	0
	Not Connected	I/O	C0	I/O	I2	K7	1

2 Buttons (Non-Debounced)

Two non-debounced buttons are provided at SW1 and SW2. These are inputs to the ispMACH 4000ZE, on ball locations J1 and J3 respectively. When the buttons are in the default (unpressed) state, they supply a logic 1 to the ispMACH 4000ZE device. When depressed, they provide a logical 0.

8-Bit DIP Switch

An 8-bit input DIP switch is provided for convenient user input at location SW3. Refer to Table 1 for the connection listing. When the switches are in the down position (switched toward the bottom of the board), they provide a logical 0 input to the ispMACH 4000ZE. When switched in the up position, they provide a logical 1.

Please note that the "ON" label on the silkscreen on the PCB may not correspond with the "ON" arrow label on the component itself. Naturally, the definition of "ON" may depend on the application.

8 LEDs

8 LEDs are provided near the bottom of the board for output indication. Refer to Table 1 for the connection listing. LEDs are lit when a logical 0 is applied.

General Test Area - Connected

At the left of the board, a general test area is provided. These test points are connected to the ispMACH 4000ZE device at the ball locations indicated on the board silkscreen. Pull-up resistors can be populated on the top of the board, and pull-down resistors can be populated on the bottom of the board. Note that not all of the test points are connected to the ispMACH 4000ZE device. For the smaller ispMACH 4000ZE device, some pins are no-connects. See Table 1 for a summary of these connections.

General Prototype Area - Unconnected

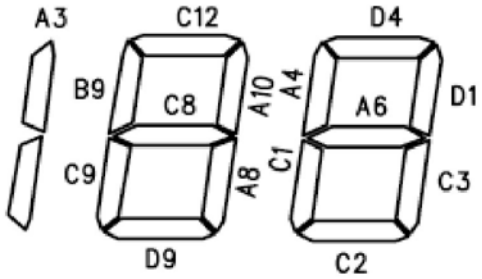
At the top of the board, a generic prototype area is provided. These are throughholes unconnected to the device. VCC and GND pin areas are also provided for convenience. The VCC areas are connected to 3.3V.

7-Segment LCD Display in 188 Configuration

The 7-segment LCD display is connected as indicated in Figure 2. Connections to the display are as indicated in Figure 2, board silkscreen, and Table 1. Application of a logical 0 at 0V will cause the corresponding segment of the display to be illuminated in black.

A bank of jumpers at J1 is provided to completely remove the 7-segment display from the board circuit. This can be useful for obtaining accurate power measurements of the ispMACH 4000ZE device. Additionally, these jumper locations provide generic access to the ispMACH 4000ZE I/O.

Figure 2. 7-Segment LCD Display



24 MHz Oscillator and Clocking

The 24 MHz oscillator near the top of the board is required for operation of the USB interface. However, it is also possible to use this oscillator as a clock input for the ispMACH 4000ZE. It is connected to ball location A7 as indicated in Table 1.

The ispMACH 4000ZE also features a user-programmable internal oscillator. For more details on this feature, see the ispMACH 4000ZE Family Data Sheet.

The ispMACH 4000ZE device can also be driven by an external clock source provided by the user.

Programming

Programming for the ispMACH 4000ZE device is controlled using the ispVM® System software, available for download from the Lattice website at www.latticesemi.com/ispvm.

Refer to the ispVM System software for help regarding operation of this software.

The ispMACH 4000ZE Evaluation Board is equipped with a built-in USB-based programming circuit. This consists of a USB microcontroller, a MachXO programmable device, and a USB connector. The MachXO is pre-programmed to act as the interface between the USB microcontroller and ispMACH 4000ZE device. When the board is connected to a PC via the inlcuded USB cable, it is recognized by the ispVM System software as a "USB Download Cable". The ispMACH 4000ZE can then be scanned and programmed using the ispVM System software.

Alternatively, the ispMACH 4000ZE device can be programmed with a Lattice ispDOWNLOAD® Cable (available separately), via the JTAG port at JP1. Refer to the board silkscreen for the correct connections for the ispDOWNLOAD cable. Remember that the board is powered via the USB connection, so even if you are programming the ispMACH 4000ZE via an ispDOWNLOAD Cable, the USB plug must be connected.

Note: If you are programming via an ispDOWNLOAD Cable, a jumper must be applied at J3 to disable the MachXO device and prevent a programming conflict situation.

For more information on the ispDOWNLOAD Cable, see the Lattice website at www.latticesemi.com/hardware.

The MachXO device can also be programmed via JTAG port JP2. However, it is not recommended to reprogram this device, as you will risk disabling the USB programming capability. JP2 is primarily used during manufacturing and initial setup of the board.

Power and Power Measurement

The board is powered via a 5V USB connection. On-board regulators are included on the board to provide 1.8V and 3.3V required by the components on the board. See Figure 3 for a block diagram of the default jumper settings and locations in relation to the ispMACH 4000ZE, on-board regulators and other components.

Jumpers J8 and J7 are positioned in-series with the power to the ispMACH 4000ZE. To measure the power consumed by the ispMACH 4000ZE I/O, remove J8 and J7 and apply an ammeter across either of them. This is a 3.3V rail, so multiply current measured by 3.3V to get wattage. To measure power consumed by the ispMACH 4000ZE device core, remove J5 and apply an ammeter across it. This is a 1.8V rail, so multiply current by 1.8V to get wattage.

See Figure 4 for a diagram of these measurements.

For more the most accurate Icc power measurements, remove jumpers J6 and J9 to disable everything on board except the ispMACH 4000ZE device and the I/Os.

Figure 3. Default Jumper Settings and Locations

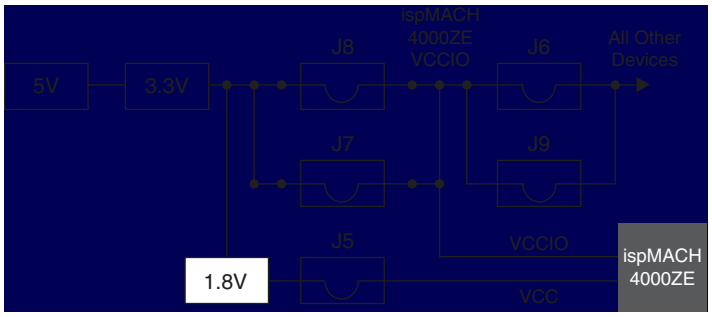
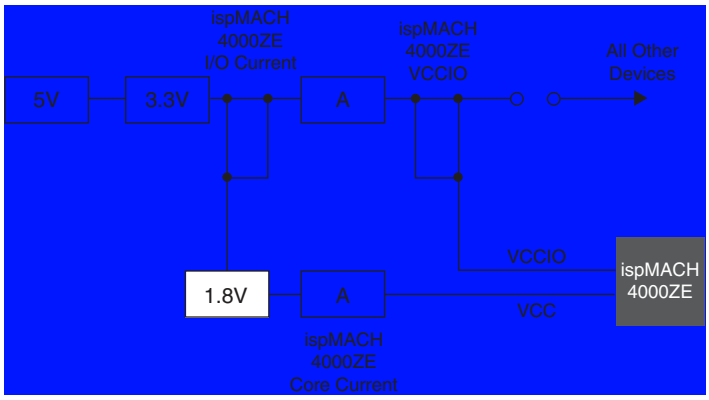


Figure 4. Power Measurement



Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
ispMACH 4064ZE Evaluation Board	LC4064ZE-EVN	
ispMACH 4256ZE Evaluation Board	LC4256ZE-EVN	

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
May 2008	01.0	Initial release.
May 2008	01.1	Updated board photo.
February 2009	01.2	Updated Power and Power Measurement text section.

Appendix A. Schematic

Figure 5. ispMACH 4000ZE

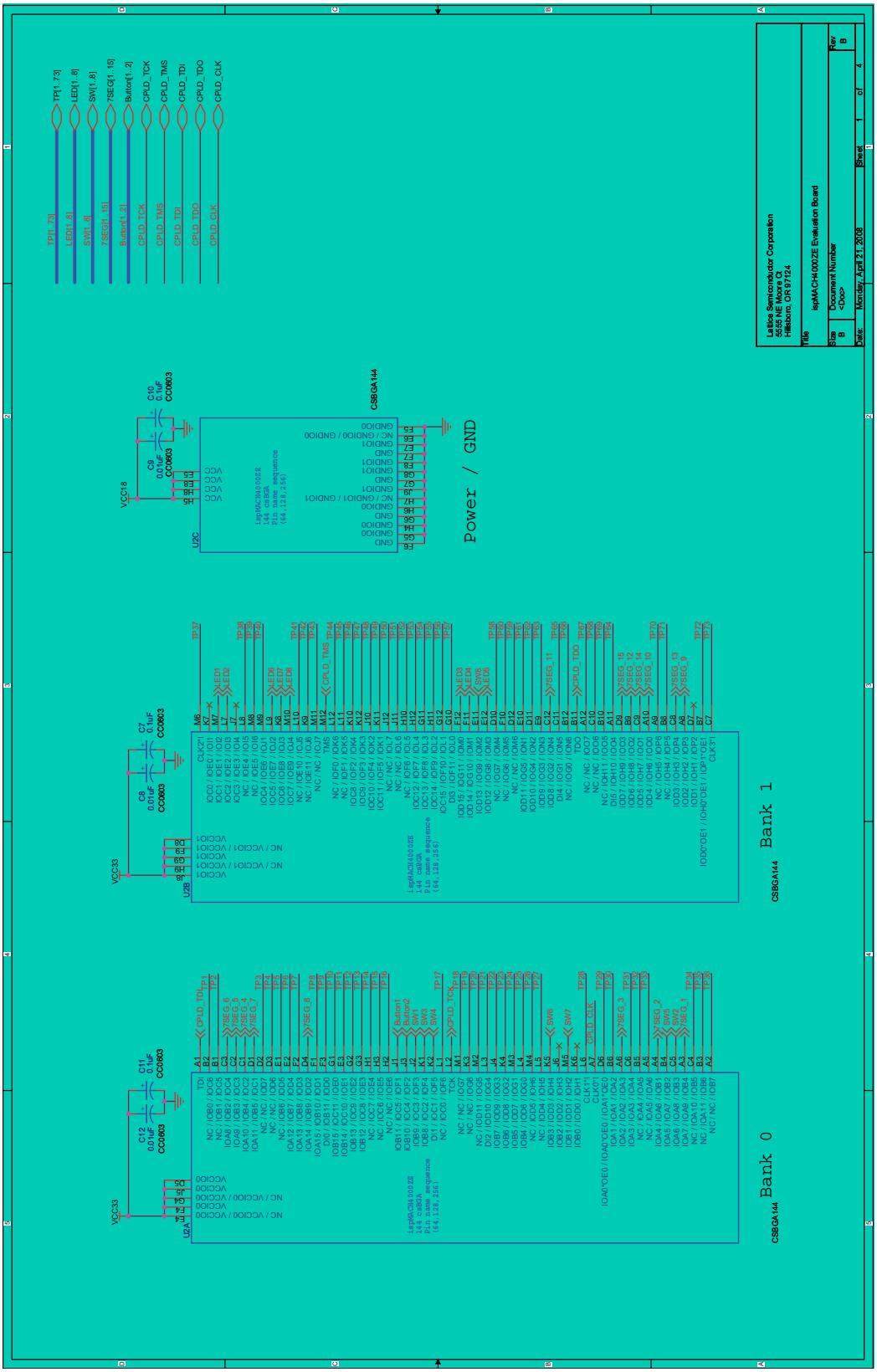


Figure 6. User I/O

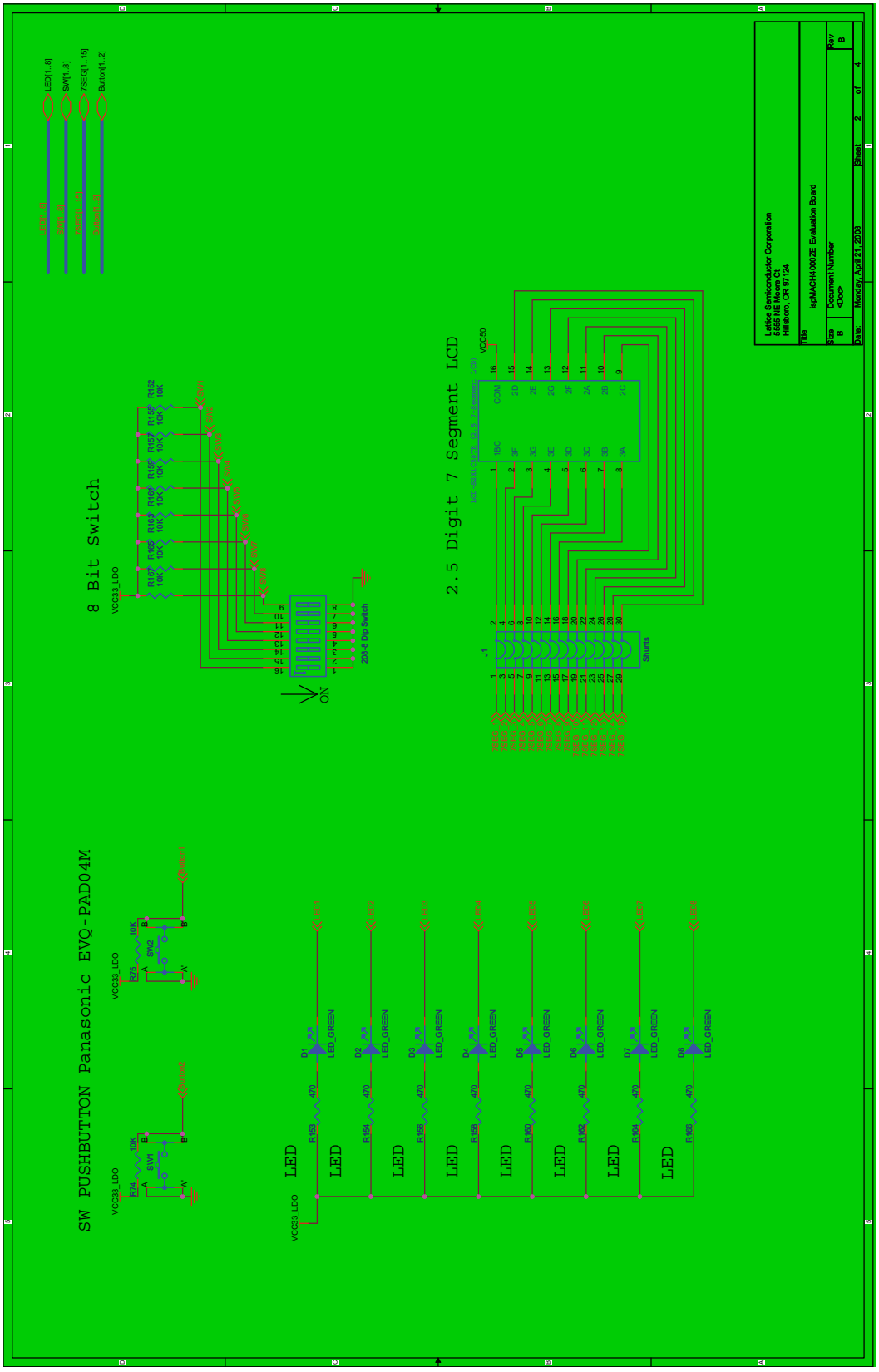


Figure 7. Test Points and Prototype Area

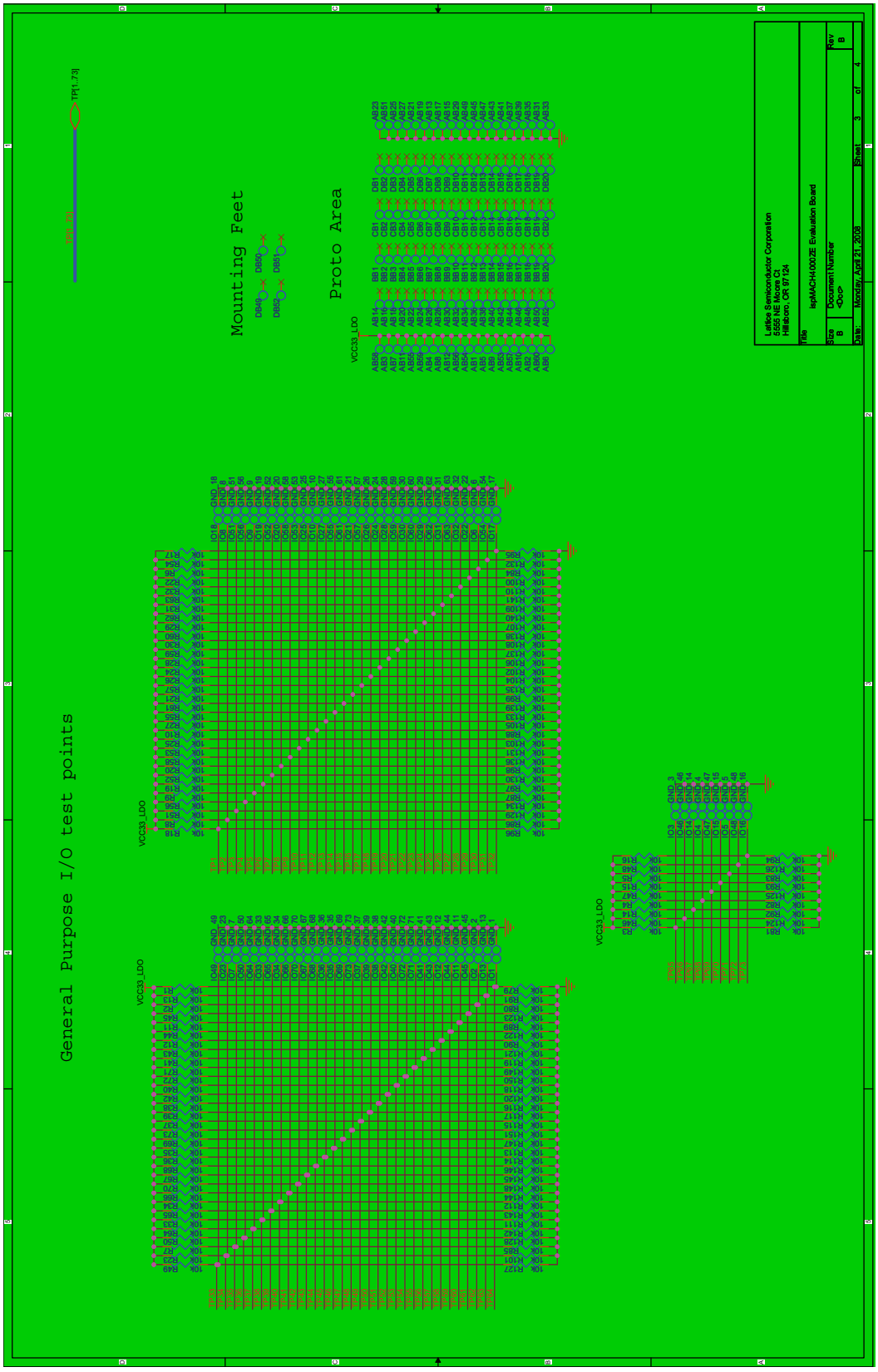


Figure 8. Programming and Power