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Evaluating the AD9081, AD9082, AD9986, or AD9988 Mixed Signal, Front-End RF Transceiver

FEATURES

- Fully functional evaluation boards for the AD9081, AD9082, AD9986, AD9988, AD9207, AD9209, or AD9177
- PC software for control with analysis, control, evaluate (ACE) software
- On-board clocking provided by the HMC7044 manages device and FPGA clocking
- Option to switch to external direct clocking

EVALUATION KIT CONTENTS

- AD9081-FMCA-EBZ, AD9082-FMCA-EBZ, AD9986-FMCB-EBZ, or AD9988-FMCB-EBZ evaluation boards
- Subminiature push on female (SMP-F) to Subminiature Version A female (SMA-F) cables (for only the AD908x-FMCA-EBZ boards)
- MicroSD cards
  - AD-FMC-SDCARD
  - ADS9V2-UZSD-MXFE

ADDITIONAL HARDWARE NEEDED

- ADS9-V2EBZ FPGA-based data capture board
- Signal generator for analog input
- Spectrum analyzer (to measure DAC output)
- SMA cable
- SMA female to female adapter (optional)
- Ethernet to USB adapter (optional)
- PC with USB port and Ethernet port
- Windows 7 or newer operating system

SOFTWARE NEEDED

- Analysis, control, evaluate (ACE) software
- DPGDownloaderLite software (included in ACE installation)
- WinSCP (or similar Telnet software)

DOCUMENTS NEEDED

- AD9081, AD9082, AD9986, AD9988, AD9207, AD9209, or AD9177 data sheet
- ADS9-V2EBZ user guide
- ACE software documentation
- Serial Control Interface Standard (Rev 1.0)
- AN-835, *Understanding High Speed ADC Testing and Evaluation*

GENERAL DESCRIPTION

This user guide describes the AD9081-FMCA-EBZ, AD9082-FMCA-EBZ, AD9986-FMCB-EBZ, and AD9988-FMCB-EBZ evaluation boards, which provide all of the support circuitry required to operate the AD9081, AD9082, AD9986, AD9988, AD9207, AD9209, or AD9177 in their various modes and configurations. The application software used to interface with the devices is also described. These evaluation boards connect to the Analog Devices, Inc., ADS9-V2EBZ for evaluation with the ACE software.

These evaluation boards can also interface to commercially available field-programmable gate array (FPGA) development boards from Xilinx® or Intel®. Information on how to use these platforms to evaluate the AD9081 or the AD9082 is available in the Using the AD-FMC-SDCARD section.

The ACE software allows the user to set up the MxFE® in various modes and to capture analog-to-digital converter (ADC) data for analysis. The DPGDownloaderLite software (included in ACE installation) generates and transmits vectors to the digital-to-analog converters (DACs), which can then be sent to a spectrum analyzer for further analysis.

For additional information, see the AD9081, AD9082, AD9986, AD9988, AD9207, AD9209, or AD9177 data sheets and the UG-1578, the device user guide, which must be consulted in conjunction with this user guide when using the evaluation boards.

TABLE OF CONTENTS

REVISION HISTORY

6/2021—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

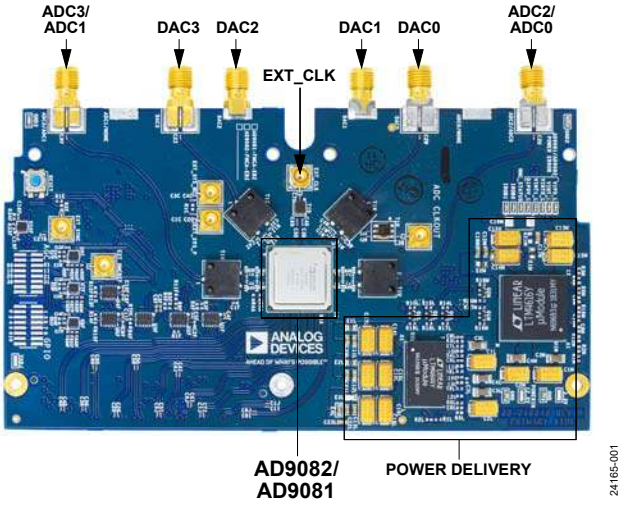

Figure 1. AD9082-FMCA-EBZ/AD9081-FMCA-EBZ Top Image

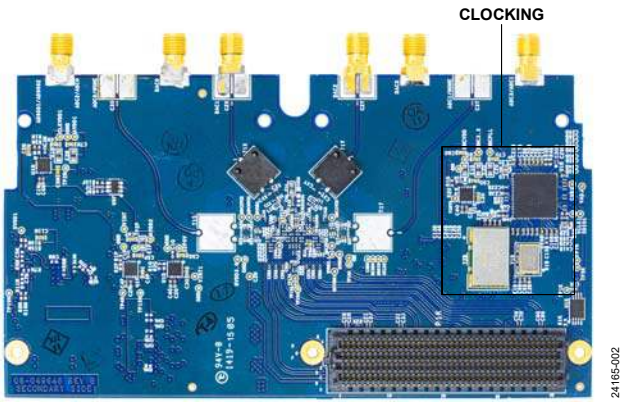

Figure 2. AD9082-FMCA-EBZ/AD9081-FMCA-EBZ Bottom Image

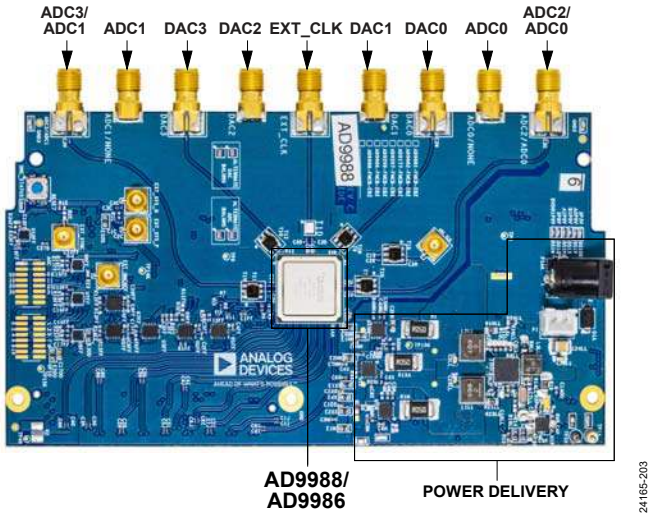

Figure 3. AD9988-FMCB-EBZ/AD9986-FMCB-EBZ Top Image

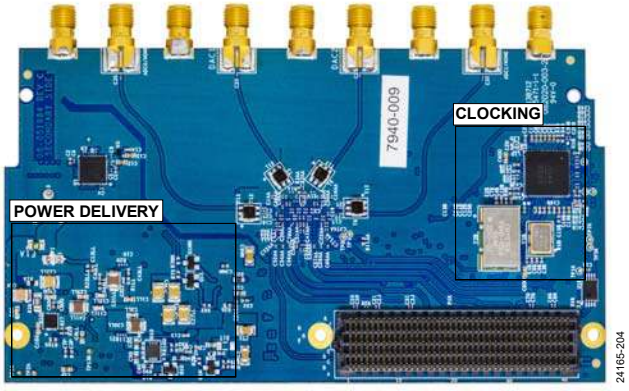

Figure 4. AD9988-FMCB-EBZ/AD9986-FMCB-EBZ Bottom Image

EVALUATION BOARD OVERVIEW

BOARD MODELS

The different board models are all listed in Table 1.

Certain early revisions of the evaluation boards shipped with a 122.88 MHz on-board crystal oscillator. The ACE plugin is designed to detect the evaluation board and make it function appropriately.

EVALUATION BOARD CONNECTION OVERVIEW

Figure 5 shows the basic hardware setup required to evaluate the AD9081, AD9082, AD9986, or AD9988. Note that the AD9082-FMCA-EBZ is shown in Figure 5 as an example. This setup uses the on-board clock to manage the clocks for the AD9082 as well as the FPGA for proper functioning of the transceivers.

Table 1. MxFE™ Evaluation Board Hardware Summary

Evaluation Board Model Number	Devices Supported[1]	Power Delivery	Analog Front-End Balun	Clock Input Network	On-Board Crystal Oscillator (MHz)
AD9081-FMCA-EBZ	AD9081/AD9209/AD9177	Via a FPGA mezzanine card (FMC) using the µModule and a low dropout (LDO) regulator	BALH-0009SMG	SMP + BAL-0416	100
AD9082-FMCA-EBZ	AD9082/AD9207	Via a FMC connector using the µModule and a LDO regulator	BALH-0009SMG	SMP + BAL-0416	100
AD9986-FMCB-EBZ	AD9986	An external 12 V using the ADP5056 and a LDO regulator	TCM1-83X/ LDB184G6	SMA + NCR2-123+	122.88
AD9988-FMCB-EBZ	AD9988	An external 12 V using the ADP5056 and a LDO regulator	TCM1-83X/ LDB184G6	SMA + NCR2-123+	122.88

[1] The AD9207, AD9209, and AD9177 do not have individual evaluation boards. The ACE plugin has specific modes that can be used within the AD9081-FMCA-EBZ for either the AD9209 or AD9177 and within the AD9082-FMCA-EBZ for the AD9207.

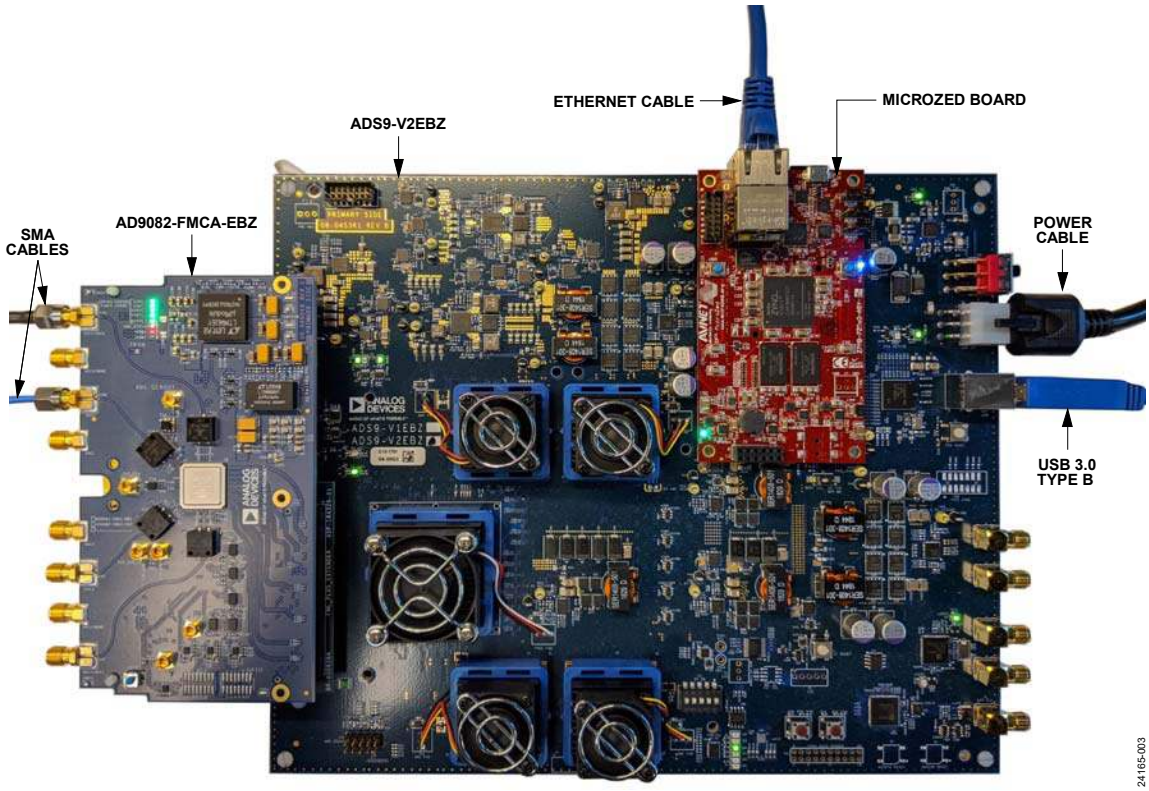

Figure 5. Bench Setup for the Evaluation of the AD9081, AD9082, AD9986, or AD9988

INSTALLATION OF HEAT SINK WITH INTEGRATED FAN

A heat sink (with integrated fan) is shipped with each evaluation board for active cooling of the IC. Note that the power consumption of the IC is dependent on its operation mode with some configurations consuming up to 13 W, where the IC die temperature can approach or exceed its maximum specified operating range of 120°C. Therefore, it is recommended to install the heat sink shown in Figure 6 through Figure 8 before the evaluation process begins.

The heat sink installation steps are as follows:

1. Remove the blue frame clip that is attached to assembly by lifting the metal tab free from this frame clip by using a small tweezer or a metal pick (see Figure 6). This frame clip is not essential for attachment of the heat sink to the IC (while noting that the AD998x-FMCB-EBZ variant does accept this frame clip due to passive components within its keep out region).
2. Remove the thin plastic tape to expose the adhesive surface (see Figure 7).
3. Carefully position and center the heat sink on top of the IC package such that it also remains clear of the RF baluns (see Figure 8).
4. Once positioned correctly, press down on the top side of the heat sink for 10 seconds to secure it to the IC package (see Figure 8).
5. Connect the power supply cable (see Figure 8).

Once power is applied to the evaluation board, the fan starts spinning. In the unlikely event that the fan does not spin, the two screws used to secure the fan to the heat sink may be too tight, which has resulted in the fan blades not spinning freely. Note that loosening the screws often releases the fan blade allowing it to spin freely.

Additional information on the Advanced Thermal Solutions fanSink™ product can be found on the website of the company.

Figure 6. Heat Sink Installation Step 1

Figure 7. Heat Sink Installation Step 2

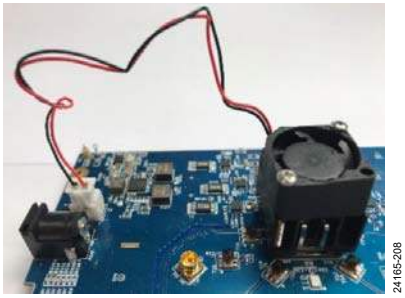

Figure 8. Heat Sink Installation Step 3 and Step 5

EVALUATION BOARD SOFTWARE

ACE AND DPGDownloaderLite

Download and run the ACE installer from the ACE web page at www.analog.com/ace. Check all options under the **High Speed DAC Components** section of this webpage to install DPGDownloaderLite, which replaces the legacy DPGDownloader (see Figure 9).

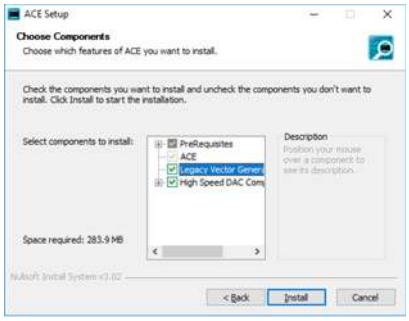

Figure 9. ACE Installation Including DPGDownloaderLite

After the ACE software is installed, the user must install the plugin for the specific evaluation board being used. There are two options for installing the plugin from ACE and from the web.

Plugin Installation from ACE

Installing plugins can be performed using the **Plug-in Marketplace** feature in the ACE software as described in this section. Plugins can be downloaded from the ACE software page by searching for the relevant device number within the ACE software.

To install a plugin from ACE, take the following steps:

1. From the **Start** menu, click **All Programs** > **Analog Devices** > **ACE** to open the main ACE software window.
2. In the left pane, click **Plug-in Manager**. The **Manage Plug-ins** window opens (see Figure 10).

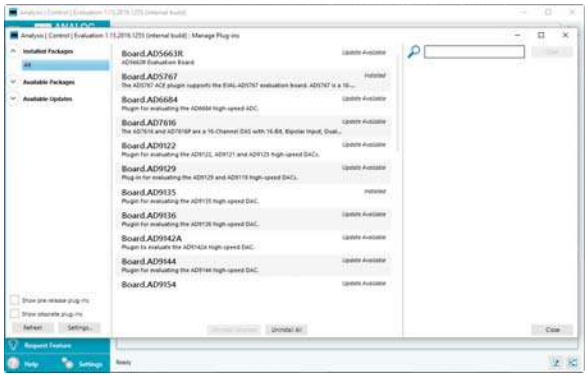

*Figure 10. ACE **Manage Plug-ins** Window*

3. Click the **Available Packages** dropdown menu on the left side of the software window.
4. Enter the device model number (AD9081, AD9082, AD9986, or AD9988) in the search bar on the right side of the window to search for the device that is intended for evaluation and find the appropriate board plugin.
5. Select the required plugin that supports the AD9081, AD9082, AD9986, or AD9988, and click **Install Selected**.
6. Click **Close**.

Plugin Installation from the Web

To install the plugin from the web, take the following steps:

1. Ensure that the ACE software is installed.
2. From the ACE software page on the Analog Devices, Inc., website (www.analog.com/ace), navigate to the **ACE Evaluation Board Plug-ins** section and search for the device to evaluate (see Figure 11).
3. Click the appropriate board plugin (see Figure 11). The board plugin automatically downloads to the PC. When the download is complete, locate the downloaded file. Note that if the browser used for the plugin download is Internet Explorer, the file extension of the plugin file may be **.zip**. If the extension is **.zip**, right-click the file and rename the file extension to **.acezip**.
4. Double-click the **.acezip** file to automatically install the plugin.
5. The plugin installation process opens the ACE software. Then, close ACE after the plugin installation completes.

*Figure 11. **ACE Evaluation Board Plug-ins** Web Installation*

INTRODUCTION TO THE AD9081, AD9082, AD9986, OR AD9988 PLUGIN

The AD9081, AD9082, AD9986, or AD9988 plugin allows the user to evaluate the AD9081, AD9082, AD9986, or AD9988 chip via the AD9081-FMCA-EBZ, AD9082-FMCA-EBZ, AD9986-FMCB-EBZ, or AD9988-FMCB-EBZ evaluation board. First, ensure that the evaluation board is connected with all of the proper hardware (see Figure 5). Next, ensure that the ADS9-V2EBZ is powered on before opening the ACE software. When the user opens the ACE software, the plugin corresponding to the evaluation board chosen appears in the **Attached Hardware** section (see Figure 12).

Board View

Double-clicking the evaluation board icon in the **Attached Hardware** section in the ACE software opens the board view corresponding to the connected evaluation board. In the example shown in Figure 12, the board used is the AD9082-FMCA-EBZ. (Note that the Ax portion of the AD9082-FMCA-EBZ board name delineates the software version.) The same steps can be used for other boards as well.

The board view tab enables the user to quickly set up the AD9081, AD9082, AD9986, or AD9988. Figure 13 shows the **QUICK CONFIGURATION** pane within the **AD9082-FMCA-EBZ** board view.

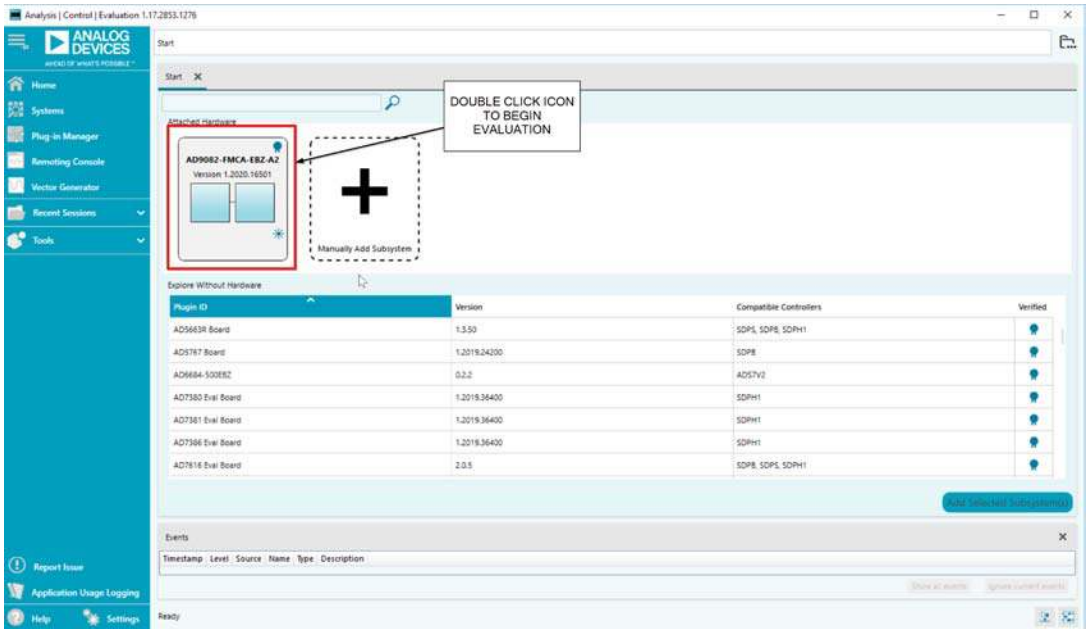

*Figure 12. ACE Initial Window Showing the **Attached Hardware** Section*

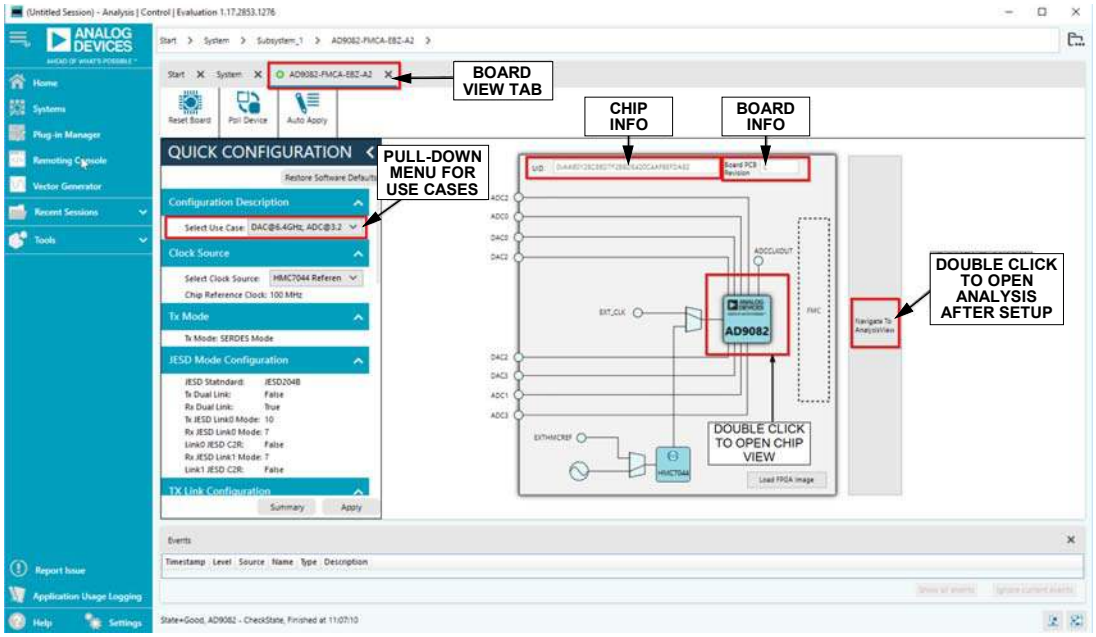

*Figure 13. **AD9082-FMCA-EBZ-A2** Board View Tab Details*

Chip View

Double-clicking the **AD9081**, **AD9082**, **AD9986**, or **AD9988** icon in the board view opens the chip view. The chip view enables the user to customize the AD9081, AD9082, AD9986, or AD9988 beyond the functions available in the board view. Use the **QUICK CONFIGURATION** pane in the chip view if using a direct external clock. Figure 14 shows the details of the chip view for the **AD9082** as an example.

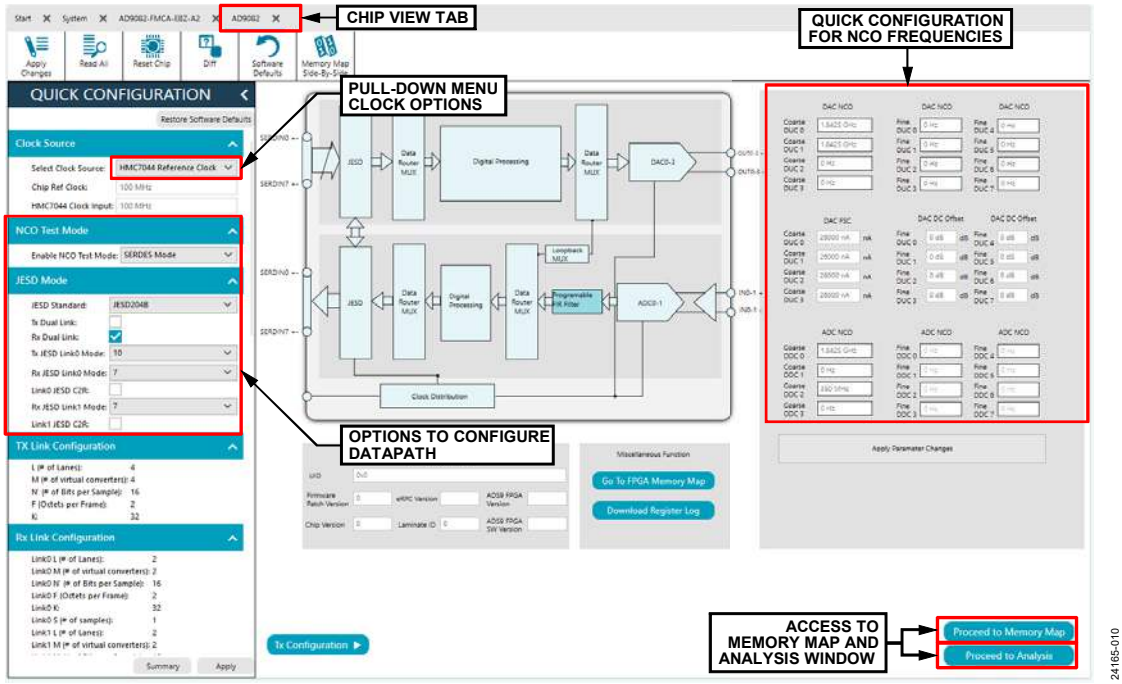

*Figure 14. **AD9082** Chip View Tab Detail*

SETTING UP THE MicroZed CONNECTION

Before performing the evaluation of the AD9081, AD9082, AD9986, or AD9988, the Ethernet interface to the MicroZed™ board must be set up by configuring the network interface between the PC and the MicroZed board.

MicroSD CARD FOR THE MicroZed BOARD

To ensure proper connection between the microSD card and the MicroZed board, take the following steps:

1. Locate the microSD card (HSX) from the contents of ADS9-V2EBZ packaging.
2. Connect the microSD card to the MicroZed board (face the contacts of the microSD card up). See Figure 15 for additional details.

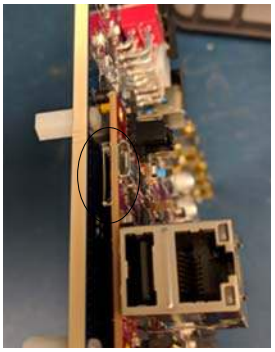

Figure 15. MicroSD Card Slot in MicroZed Board

3. As a precaution, ensure that the MicroZed board is seated properly on the ADS9-V2EBZ (see Figure 5). Only a visual inspection is needed.

MODE JUMPER CONNECTIONS FOR THE MicroZed BOARD

Ensure that the mode jumpers on the MicroZed board are connected as shown in Figure 16.

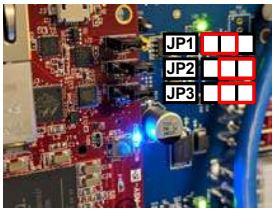

Figure 16. Mode Jumper Connections for MicroZed Board

The boot mode jumpers (JP1 to JP3) shown in Figure 16 allow the MicroZed board to boot the image from the microSD card.

CONFIGURE THE NETWORK INTERFACE TO THE MicroZed BOARD

To configure the network interface to the MicroZed board, take the following steps:

1. Ensure that the connections to ADS9-V2EBZ are as shown in Figure 5. It is not necessary to connect the AD9082-FMCA-EBZ (or the AD9081-FMCA-EBZ, AD9986-FMCB-EBZ, or AD9988-FMCB-EBZ) evaluation board.
2. One end of the Ethernet cable can be connected directly to the PC Ethernet port or to a USB to Ethernet adapter, with the other end connected to the MicroZed board.
3. Power on the ADS9-V2EBZ board. Allow up to 10 sec for the MicroZed board to boot up.
4. Open the local area connection settings. On Windows® 7: **Start Menu > Control Panel > Network and Sharing Center > Change adapter settings**. On Windows 10: **Start Menu > Settings > Network & Internet > Change adapter options**.
5. If the **Local Area Connection** icon does not appear in the **Network Connections** window, unplug the Ethernet connection from the MicroZed board and then reconnect it.
6. Double-click the **Local Area Connection** icon that appears (Figure 17 shows **Local Area Connection 3** as an example).
7. Click **Properties**.
8. Select **Internet Protocol Version 4 (TCP/IPv4)**.
9. Click **Properties**.
10. Enter **192.168.0.2** in the **IP address** field.
11. Ensure the **Subnet mask** field shows **255.255.255.0**.
12. Click **OK**.

CHECKING THE CONNECTION TO THE MicroZed BOARD

To check the connection to the MicroZED board, take the following steps:

1. Power cycle the ADS9-V2EBZ. Wait about 10 sec for the MicroZed to boot up.
2. Open a Telnet software, such as WinSCP or Tera Term.
3. Initiate a secure shell (SSH) connection to 192.168.0.10, which is the IP address to the embedded remote procedure call (eRPC) server in the MicroZed board.
4. Login with username: **root** and password: **analog**.
5. When the login is complete, the contents of the root folder display in the Telnet software, which confirms the Ethernet connection.

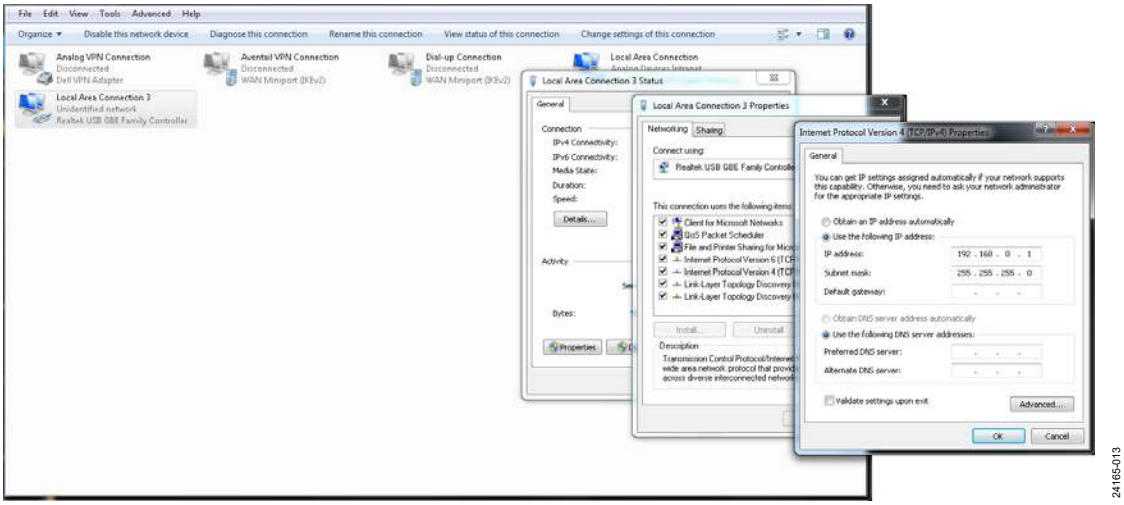

Figure 17. Internet Protocol Settings

EVALUATION BOARD HARDWARE SETUP

DETERMINE THE CLOCK SOURCE

Determine whether the AD9081-FMCA-EBZ, AD9082-FMCA-EBZ, AD9986-FMCB-EBZ, or AD9988-FMCB-EBZ is set to the external clock or on-board HMC7044 clock by checking the C3D, C4D, C5D, and C6D capacitors on the evaluation board chosen. By default, the HMC7044 clock is enabled (C3D and C5D are placed on the evaluation board, and C4D and C6D are do not insert (DNI)). If using a direct external clock, remove the C3D and C5D capacitors and place the C4D and C6D capacitors on the evaluation board. The capacitors are 0.1 µF, size 0201 (imperial) or size 0603 (metric). For additional details, see Figure 18 and Figure 19.

DEFAULT CLOCKING SCHEME FOR AD9081-FMCA-EBZ, AD9082-FMCA-EBZ, AD9986-FMCB-EBZ, OR AD9988-FMCB-EBZ

The default clocking scheme for these evaluation boards uses the on-chip phase-locked loop (PLL) within the AD9081, AD9082, AD9986, or AD9988. The HMC7044 provides the reference input to the chip. The evaluation board provides all the necessary clocks for conducting a quick evaluation of the device, including the auxiliary clocks needed by the FPGA in the ADS9-V2EBZ board to set up the JESD204B or JESD204C link. The clocking scheme is shown in Figure 20. As shown in Table 1, the reference frequencies used by the two boards (AD908x-FMCA-EBZ or AD998x-FMCB-EBZ) are different. Therefore, each board only supports the integer multiples of the crystal oscillator that are on the evaluation board. The plugin only supports the integer multiples of the crystal oscillator that are installed on the evaluation board. If a different clock frequency is required for evaluation, the user must modify the evaluation board to accept an external clock by following the instructions previously listed. This modification also necessitates an additional clock source for the ADS9-V2EBZ. Refer to Figure 30 for additional details on the instrument setup.

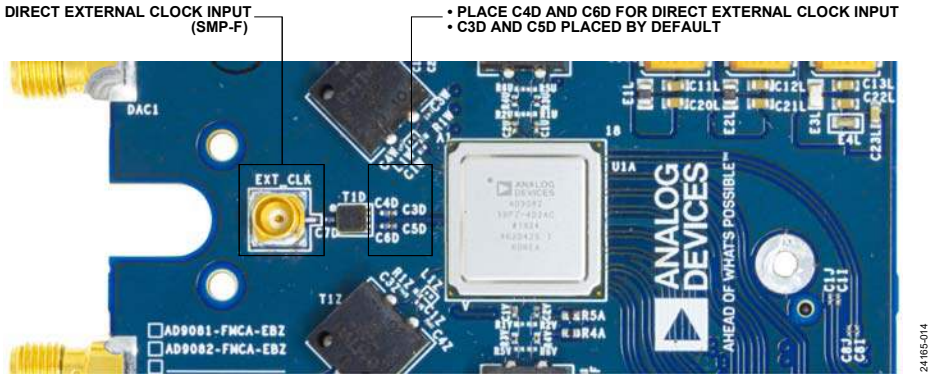

Figure 18. Capacitor Position for Direct External vs. On-Board HMC7044 Clocking (Showing the AD908x-FMCA-EBZ)

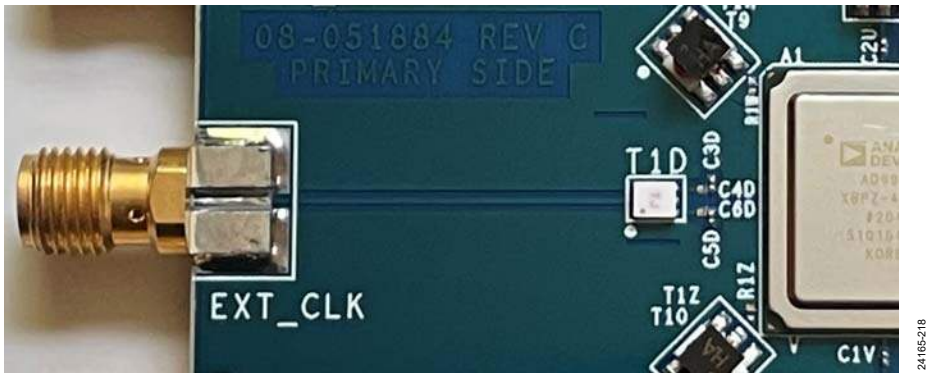

Figure 19. Capacitor Position for Direct External vs. On-Board HMC7044 Clocking (Showing the AD998x-FMCB-EBZ Evaluation Board)

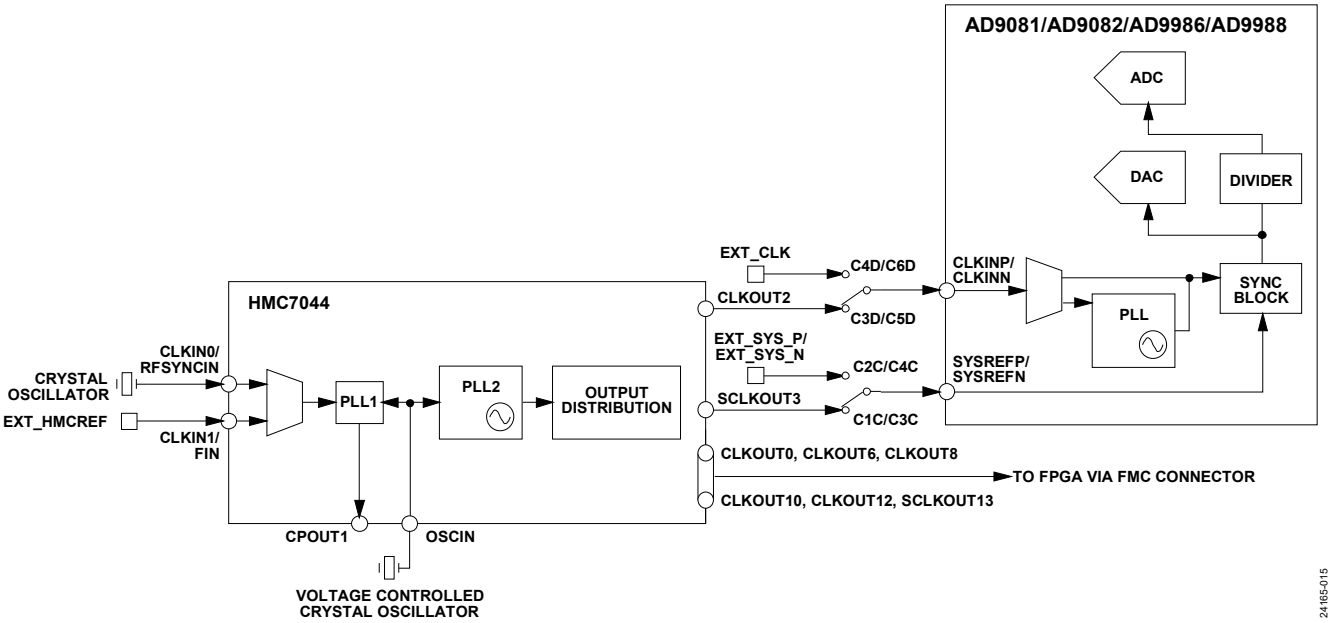

Figure 20. Default Clocking Scheme Used for the AD9081, AD9082, AD9986, or AD9988 Evaluation Board

SET UP THE INSTRUMENTATION

To use on-board clocking, the user must only provide an analog input signal using a signal generator. To analyze DAC outputs, a spectrum analyzer is needed.

The following are recommended instruments and connectors:

- Signal generator: a low phase noise signal generator, such as the Rohde & Schwarz SMA (100A or 100B) or Keysight UXG/EXG series. Note that the performance listed in the product data sheet is from the Rohde & Schwarz SMA100B with the B-711 option.
- Spectrum analyzer: Keysight PXA/UXA or Rohde & Schwarz FSW/FSWP.
- Cables: use a shielded, RG-58, 50 Ω coaxial cable.

Ensure that the 10 MHz references are shared between the instruments.

Analog Devices recommends the coaxial, 48.0 in. (1.2 m or 4.0 ft), RG316 DS, SMA to SMA, male to male cable assembly from Cinch Connectivity Solutions Johnson, Part Number 415-0033-048 for the setup.

Set Up the Spectrum Analyzer

Analog Devices recommends the following configuration for the spectrum analyzer:

- Start frequency = 50 MHz (or 0 MHz)
- Stop frequency = 5 GHz
- Resolution bandwidth = 30 kHz
- Use an average or rms detector setting and set the input attenuation to 6 dB or as desired

These settings can be changed to satisfy the particular use case.

It is recommended to have all the instruments share a common reference. Usually, this common reference is achieved by connecting the 10 MHz reference output from one instrument to the reference input of the next, and so on.

USING THE AD9081, AD9082, AD9986, OR AD9988 BOARD VIEW

The board view allows the user to quickly set up the AD9081, AD9082, AD9986, or AD9988 to a predetermined use case for evaluation. The board view uses the on-board clocking solution to manage the clocks to the AD9081, AD9082, AD9986, or AD9988, as well as the FPGA. For more details on the clock setup, refer to Figure 20. Figure 21 shows the hardware connection needed when using the board view with the AD9082-FMCA-EBZ board as an example.

USE CASES

The use cases in Table 2, Table 3, Table 4, and Table 5 are supported for JESD204B and JESD204C modes for the AD9081-FMCA-EBZ, AD9082-FMCA-EBZ, AD9986-FMCB-EBZ, or AD9988-FMCB-EBZ. Tx means transmit data path, and Rx means receive data path.

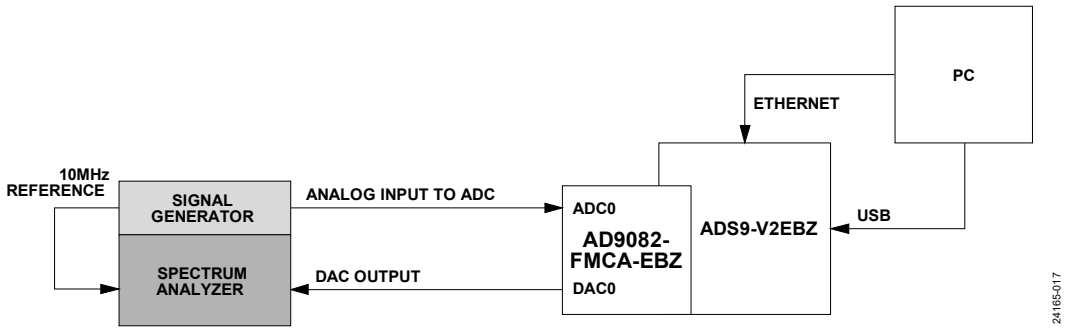

Figure 21. Hardware Setup for Using the Board Wizard (Note the 10 MHz Reference Connection)

In Table 2, N/A means not applicable.

Table 2. Use Cases for AD9081-FMCA-EBZ Board View (Uses 100 MHz On-Board Crystal Oscillator, All Single Link)

Description	Clock (GHz)		JESD204x Mode[1]		Tx Interpolation		Rx Decimation		Tx Data Rate (MSPS)	No. of Tx Channels	Rx Data Rate (MSPS)	No. of Rx Channels	Link Line Rate (Gbps/lane)	JESD204x Protocol[2]
	Tx	Rx	Tx	Rx	Coarse	Fine	Coarse	Fine						
12 GSPS DAC, 1.5 GSPS I/Q, 4 GSPS ADC, Full Bandwidth	12	4	15C	27C	8	1	1	1	1500	4	4000	4	24.75	C
12 GSPS DAC, 1.5 GSPS I/Q, 3 GSPS ADC, Full Bandwidth	12	3	15C	18C	8	1	1	1	1500	4	3000	4	24.75	C
6 GSPS DAC, 1.5 GSPS I/Q, 3 GSPS ADC, Full Bandwidth	6	3	15C	18C	4	1	1	1	1500	4	3000	4	24.75	C
12 GSPS DAC, 4 GSPS ADC, 250 MSPS I/Q	12	4	9B	10B	8	6	4	4	250	4	250	4	10	B
Dual Band Setup, 12 GSPS DAC, 3 GSPS ADC, 375 MSPS I/Q	12	3	16B	17B	8	4	2	4	375	4	375	4	15	B

Description	Clock (GHz)		JESD204x Mode[1]		Tx Interpolation		Rx Decimation		Tx Data Rate (MSPS)	No. of Tx Channels	Rx Data Rate (MSPS)	No. of Rx Channels	Link Line Rate (Gbps/lane)	JESD204x Protocol[2]
	Tx	Rx	Tx	Rx	Coarse	Fine	Coarse	Fine						
AD9209 Full Bandwidth	N/A	4	N/A	27C	N/A	N/A	1	1	BYP	BYP	4000	4	24.75	C
AD9177 1.5 GSPS I/Q mode	12	N/A	15C	N/A	8	1	N/A	N/A	1500	4	N/A	N/A	24.75	C
NCO Test Mode	12	N/A	9B	N/A	8	6	N/A	N/A	N/A	4	N/A	N/A	N/A	N/A

[1] B means JESD204B, and C means JESD204C. Note that Rx mode applies to the ADC data path (or JESD204 Tx/JTx), and Tx mode applies to the DAC data path (or JESD204 Rx/JRx). For more information about the JESD204B or JESD204C modes, refer to the UG-1578, *System Development User Guide for the AD9081 and AD9082 Direct RF Sampling Transceivers*.
[2] B means JESD204B, and C means JESD204C.

In Table 3, N/A means not applicable.

Table 3. Use Cases for AD9988-FMCBA-EBZ Board View (Uses 122.88 MHz On-Board Crystal Oscillator, All Single Link)

Description	Clock (GHz)		JESD204x Mode[1]		Tx Interpolation		Rx Decimation		Tx Data Rate (MSPS)	No. of Tx Channels	Rx Data Rate (MSPS)	No. of Rx Channels	Link Line Rate (Gbps/lane)	JESD204x Protocol[2]
	Tx	Rx	Tx	Rx	Coarse	Fine	Coarse	Fine						
mmWave 5G, 4T4R single band, 983.04 MSPS I/Q	11.79648	2.94912	15C	16C	12	1	3	1	983.04	4	983.04	4	16.22016	C
mmWave 5G, 4T4R single band, 1474.56 MSPS I/Q	11.79648	2.94912	15C	16C	8	1	2	1	1474.56	4	1474.56	4	24.33024	C
11.79648 GSPS DAC, 2.94912 GSPS ADC, 245.76 MSPS I/Q	11.79648	2.94912	9B	10B	8	6	4	4	245.76	4	245.76	4	9.8304	B
Dual Band Setup, 5.89824 GSPS DAC, 2.94912 GSPS ADC, 368.64 MSPS I/Q	5.89824	2.94912	16B	17B	8	2	4	2	368.64	4	368.64	4	14.7456	B
NCO Test Mode	11.79648	N/A	9B	N/A	8	6	N/A	N/A	N/A	4	N/A	N/A	N/A	N/A

[1] B means JESD204B, and C means JESD204C. Note that Rx mode applies to the ADC data path (or JESD204 Tx/JTx), and Tx mode applies to the DAC data path (or JESD204 Rx/JRx). For more information about the JESD204B or JESD204C modes, refer to the UG-1578, *System Development User Guide for the AD9081 and AD9082 Direct RF Sampling Transceivers*.
[2] B means JESD204B, and C means JESD204C.

In Table 4, N/A means not applicable.

Table 4. Use Cases for AD9082-FMCA-EBZ Board View (Uses 100 MHz On-Board Crystal Oscillator, all single link)

Description	Clock (GHz)		JESD204x Mode[1]		Tx Interpolation		Rx Decimation		Tx Data Rate (MSPS)	No. of Tx Channels	Rx Data Rate (MSPS)	No. of Rx Channels	Link Line Rate (Gbps/lane)	JESD204x Protocol[2]
	Tx	Rx	Tx	Rx	Coarse	Fine	Coarse	Fine						
4D2A, 12 GSPS DAC, 1.5 GSPS I/Q, 6 GSPS ADC, Full Bandwidth	12	6	15C	19C	8	1	1	1	1500	4	6000	2	24.75	C
2D2A, 12 GSPS DAC, 1.5 GSPS I/Q, 6 GSPS ADC, Full Bandwidth	12	6	10C	19C	8	1	1	1	1500	2	6000	2	24.75	C
6 GSPS DAC, 1.5 GSPS I/Q, 6 GSPS ADC, Full Bandwidth	6	6	15C	19C	4	1	1	1	1500	4	6000	2	24.75	C
12 GSPS DAC, 4 GSPS ADC, 250 MSPS I/Q	12	3	9B	6B	8	6	4	6	250	4	250	2	10	B
Dual Band Setup, 6 GSPS DAC, 3 GSPS ADC, 375 MSPS I/Q	6	3	16B	10B	8	2	4	2	375	4	375	2	15	B
6 GSPS DAC, 6 GSPS ADC, 1000 MSPS I/Q	6	6	28C	22C	6	1	6	1	1000	4	1000	2	24.75	C
AD9207 Full Bandwidth	N/A	6	N/A	19C	N/A	N/A	1	1	N/A	N/A	6000	2	24.75	C
NCO Test Mode	12	N/A	9B	N/A	8	6	N/A	N/A	N/A	4	N/A	N/A	N/A	N/A

[1] B means JESD204B, and C means JESD204C. Note that Rx mode applies to the ADC data path (or JESD204 Tx/JTx), and Tx mode applies to the DAC data path (or JESD204 Rx/JRx). For more information about the JESD204B or JESD204C modes, refer to the UG-1578, *System Development User Guide for the AD9081 and AD9082 Direct RF Sampling Transceivers*.

[2] B means JESD204B, and C means JESD204C.

In Table 5, N/A means not applicable.

Table 5. Use Cases for AD9986-FMCBA-EBZ Board View (Uses 122.88 MHz On-Board Crystal Oscillator, All Single Link)

Description	Clock (GHz)		JESD204x Mode[1]		Tx Interpolation		Rx Decimation		Tx Data Rate (MSPS)	No. of Tx Channels	Rx Data Rate (MSPS)	No. of Rx Channels	Link Line Rate (Gbps/lane)	JESD204x Protocol[2]
	Tx	Rx	Tx	Rx	Coarse	Fine	Coarse	Fine						
mmWave 5G, 4T2O single band, 983.04 MSPS I/Q	11.79648	5.89824	15C	11C	12	1	6	1	983.04	4	983.04	2	16.22016	C
mmWave 5G, 4T2R single band, 1474.56 MSPS I/Q	11.79648	2.94912	15C	11C	8	1	2	1	1474.56	4	1474.56	2	24.33024	C
4T2O Rx Digital Predistortion (DPD)	11.79648	5.89824	9B	11B	8	6	2	6	245.76	4	491.52	2	9.8304	B
Dual Band Setup, 5.89824 GSPS DAC, 2.94912 GSPS ADC, 368.64 MSPS I/Q	5.89824	2.94912	16B	10B	8	2	4	2	368.64	4	368.64	2	14.7456	B
NCO Test Mode	11.79648	N/A	9B	N/A	8	6	N/A	N/A	N/A	4	N/A	N/A	N/A	N/A

[1] B means JESD204B, and C means JESD204C. Note that Rx mode applies to the ADC data path (or JESD204 Tx/JTx), and Tx mode applies to the DAC data path (or JESD204 Rx/JRx). For more information about the JESD204B or JESD204C modes, refer to the UG-1578, *System Development User Guide for the AD9081 and AD9082 Direct RF Sampling Transceivers*.

[2] B means JESD204B, and C means JESD204C.

SETTING UP THE AD9081, AD9082, AD9986, OR AD9988 IN FULL BANDWIDTH MODE

Set up the evaluation board as explained in the Evaluation Board Hardware Setup section. Open the board view. This section uses the evaluation board in its default configuration with the HMC7044 clock enabled (C3D and C5D are placed, and C4D and C6D are DNI). See Figure 18 and Figure 19 for additional details.

In the **QUICK CONFIGURATION** pane, select the **DAC@12.0GHz, ADC@6.0GHz, JESD204C (4D2A ADC Full Bandwidth)** from the **Select Use Case** pulldown menu (see Figure 22), and click **Apply**.

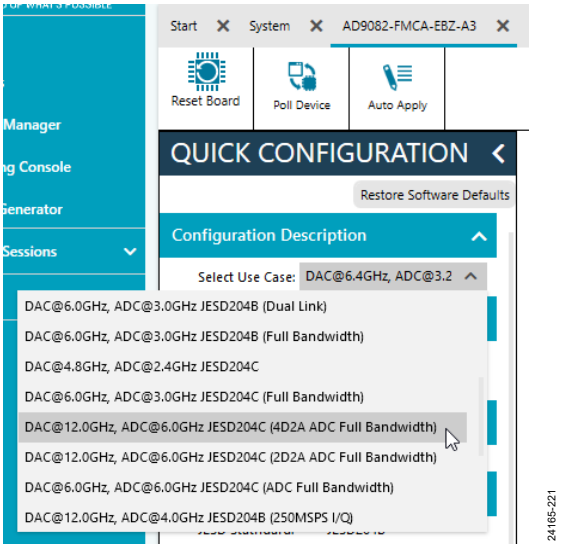

Figure 22. Selecting Full Bandwidth (JESD204C) Mode in the Board View

After clicking **Apply**, the **Quick Configuration Summary** pane displays. Double-click the **AD9081** or **AD9082** chip for further analysis. Figure 23 shows the **AD9082** chip as an example.

A block diagram that allows transmitter, receiver, and programmable filter configurations loads, as shown in Figure 24. Click **Proceed to Analysis**. In addition, see the ADC Analysis and DAC Output Setup section for additional details.

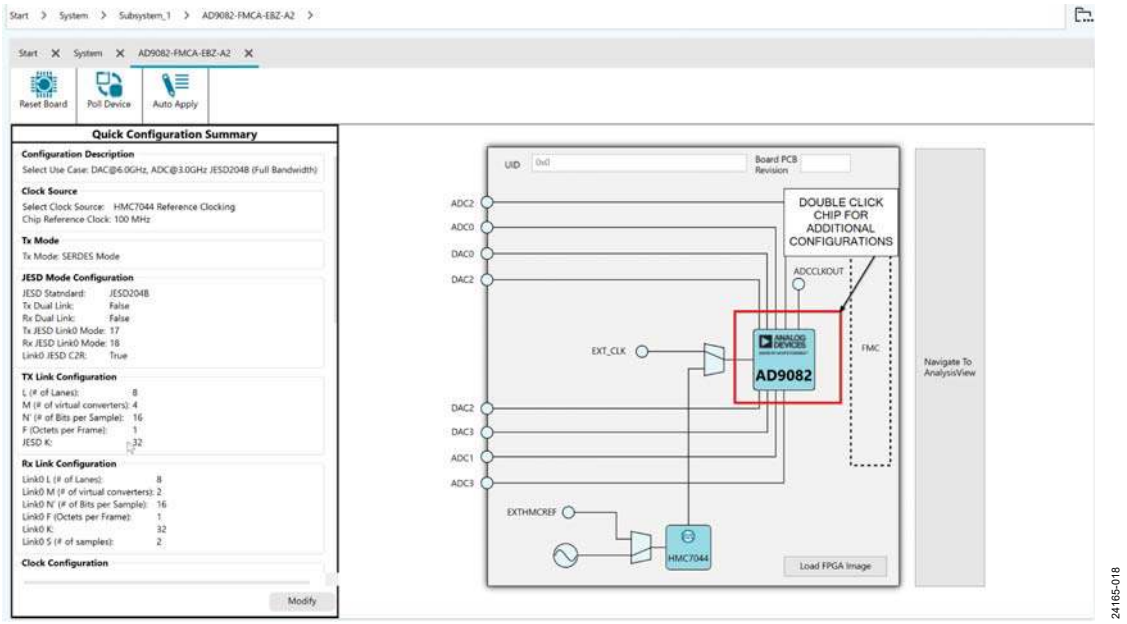

Figure 23. Navigating to Chip View for Additional Controls

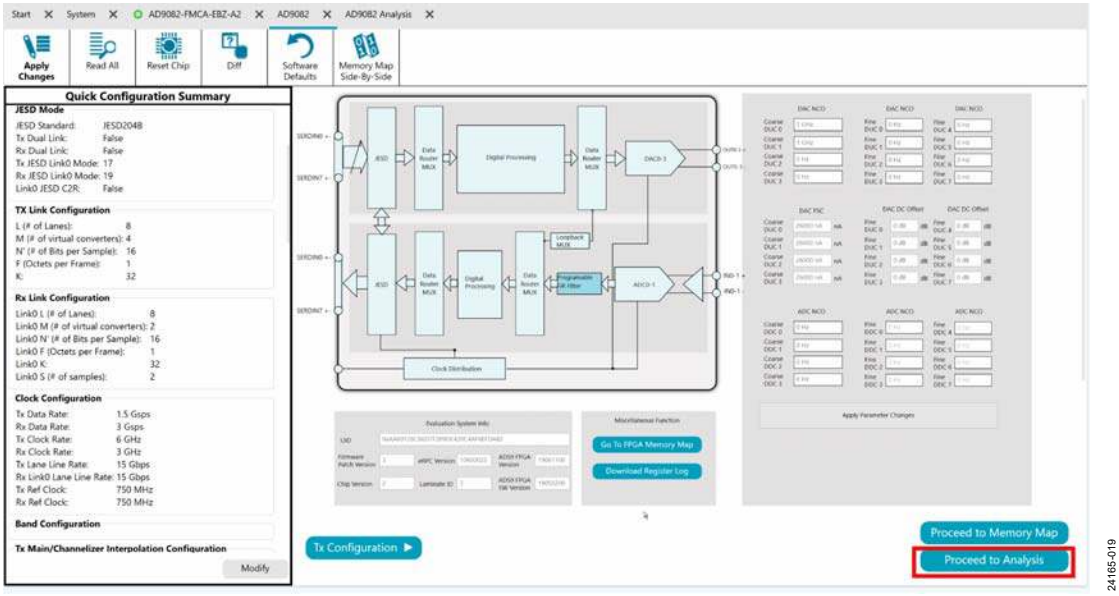

Figure 24. Additional Controls Including Analysis Features

ADC ANALYSIS AND DAC OUTPUT SETUP

This section explains how to use ACE for analysis of ADC data and DPGDownloaderLite (included in ACE installation) for sending waveforms out the DAC channels. Regardless of whether the board view or the chip view is used, the same procedure applies to using ACE and the DPGDownloaderLite software.

CAPTURE AND ANALYSIS OF ADC DATA

After setting up the AD9081, AD9082, AD9986, or AD9988 using the **QUICK CONFIGURATION** pane in the board view, open the ADC data analysis window by clicking the **Proceed to Analysis** button in the AD9081, AD9082, AD9986, or AD9988 chip view. Set up a signal generator with a single-tone sinusoid at 1.81 GHz and ~6.5 dBm output power. Supply this signal to the ADC0 input. Select the **Waveform** and **FFT** boxes on the left side of the pane, and then click **Run Once** to run the FFT analysis (see Figure 25). A graph displays, together with details of the analysis. For optimum ADC performance, ensure that the correct Nyquist zone is selected in the **QUICK CONFIGURATION** options.

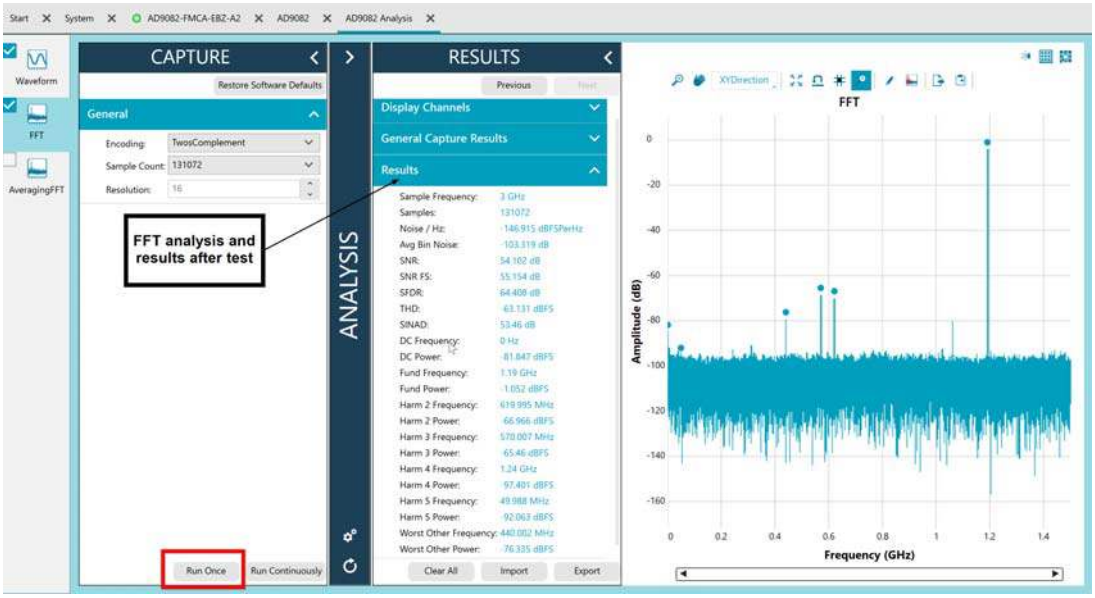

Figure 25. FFT Analysis Window Showing a 1.81 GHz Tone Sampled at 3 GSPS

DAC WAVEFORM GENERATION USING DPGDownloaderLITE SOFTWARE

To generate a waveform using the DPGDownloaderLite software, open DPGDownloaderLite (**Start** > **All Programs** > **Analog Devices** > **DPGDownloaderLite**) within the ACE software and ensure the evaluation board is displaying the product number matching the hardware used. Ensure **AD9081, AD9082**, **AD9986**, or **AD9988** is selected under **Eval Board** (**AD9082** is shown in Figure 26).

Next, select **Single Tone** from **Add Generated Waveform** (see Figure 26).

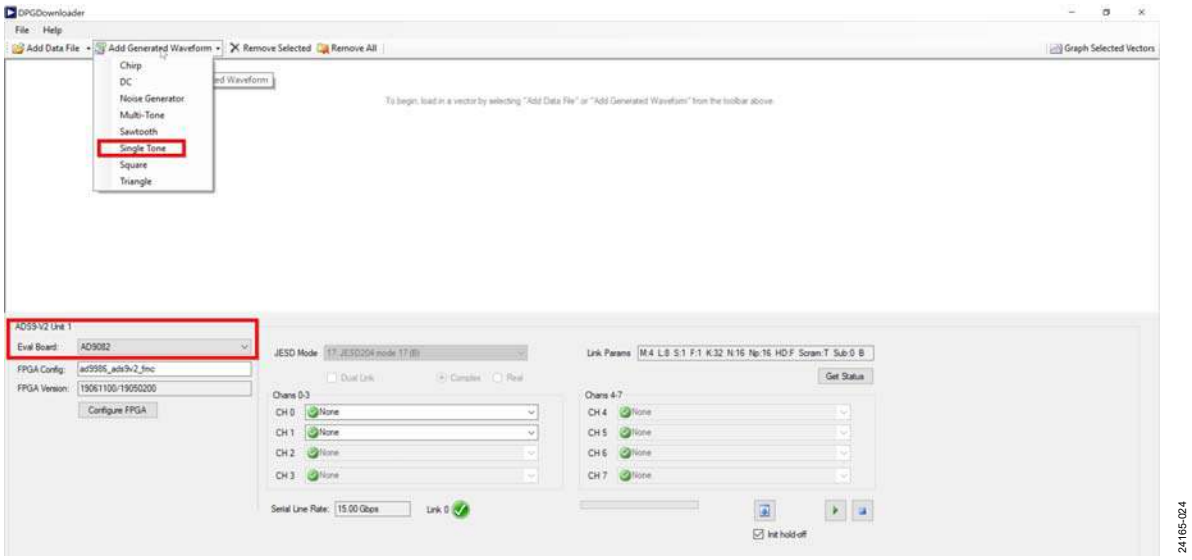

Figure 26. Single-Tone Generation

Then, in the DPGDownloaderLite software, follow these steps:

1. At the top of the window, enter or verify the following data values, as shown in Figure 28:
   a. **Data Rate**: this must match the selected **Tx Data Rate** field under the **Clock Configuration** section in ACE.
   b. **DAC Resolution**: 16 bits.
   c. **Record Length**: 16384.
   d. **Offset**: 0.
   e. **Desired Frequency**: 10.000 MHz.
   f. **Amplitude**: 0.0 dB.
   g. **Relative Phase**: 0.0°.
   h. **Unsigned Data**: cleared.
   i. **Allow even cycle count**: cleared.
   j. **Generate Complex Data (I & Q)**: selected.
2. Select the channels. In Figure 28, two channels are selected.
   a. **CH 0** dropdown box: **Single Tone - 10.025 MHz; 0.0 dB; 0.0°(C)**
   b. **CH 1** dropdown box: **Single Tone - 10.025 MHz; 0.0 dB; 0.0°(C)**.
3. Click the **Download** button.
4. Click **Play** to display the waveform on the spectrum analyzer.

Then, connect the DAC0 or DAC1 output to a spectrum analyzer. A 1.85 GHz single tone appears on the spectrum analyzer as shown in Figure 27.

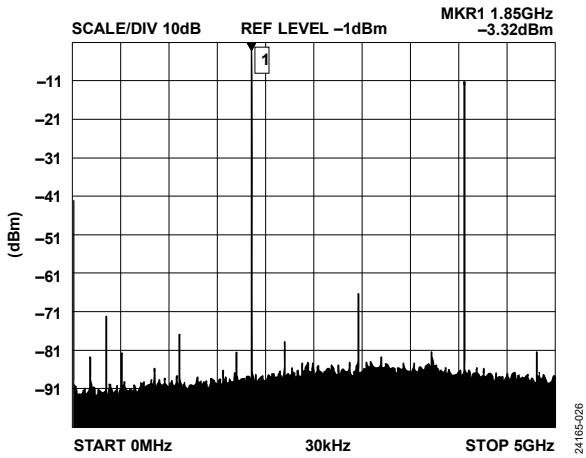

Figure 27. Spectrum Analyzer Plot Showing Single Tone at 1.85 GHz

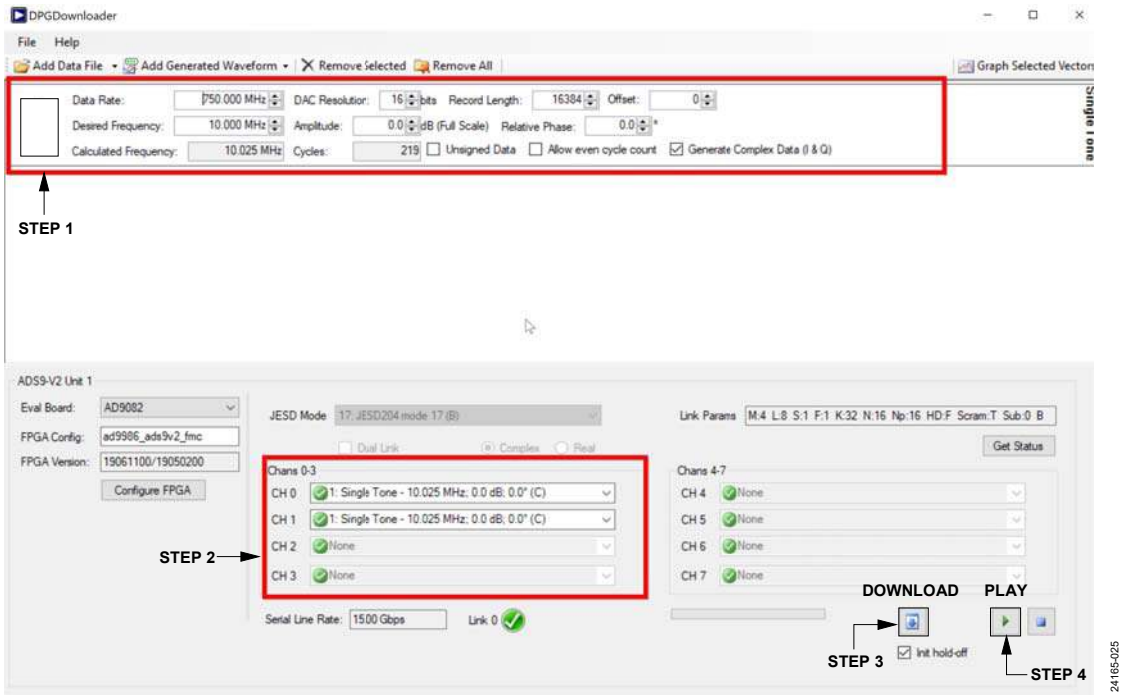

Figure 28. Downloading the Single-Tone Signal to the DAC

USING THE AD9081, AD9082, AD9986, OR AD9988 CHIP VIEW

The chip view enables the user to customize the AD9081, AD9082, AD9986, or AD9988 beyond the functions available in the board view. Use the chip view if using a direct external clock. The chip view provides a more customizable user interface (UI) that directs the user through the various aspects of the device setup. For optimal use of the chip view, provide a direct external clock to the AD9081-FMCA-EBZ, AD9082-FMCA-EBZ, AD9986-FMCB-EBZ, or AD9988-FMCB-EBZ. Refer to Figure 18 and Figure 19 for information on how to modify the board for a direct external clock. When using direct external clock mode, the user must provide the device clock as well as the FPGA reference clock.

SETTING UP THE AD9081 OR THE AD9082 IN FULL BANDWIDTH MODE WITH EXTERNAL CLOCKING

Take the steps that follow to set up the AD9081 or the AD9082 in full bandwidth mode. The AD9986 or the AD9988 does not offer full bandwidth mode. Refer to the UG-1578 to see what options are supported by the various devices.

1. Set up the evaluation board hardware and instrumentation as shown in Figure 30.
2. Set the clock signal generator to 6 GHz, with an amplitude set to 5 dBm. Provide this signal to J6 of the AD9081-FMCA-EBZ or the AD9082-FMCA-EBZ.
3. Set the reference clock signal generator to 750 MHz with an amplitude set to 5 dBm. Provide this signal to the J1 EXT CLK connector of the ADS9-V2EBZ.
4. Set the analog input signal generator to 1.81 GHz with an amplitude set to ~6.5 dBm. Turn the signal generator output off for this setup.
5. Open the chip view. In the **QUICK CONFIGURATION** pane, select the **External Direct Clocking (J6)** clock source, as shown in Figure 29.

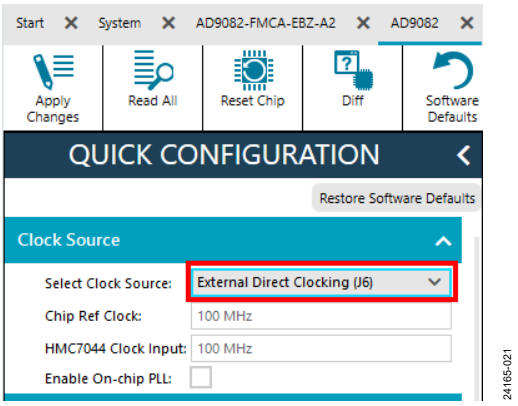

Figure 29. Selecting the Clock Source in Chip View

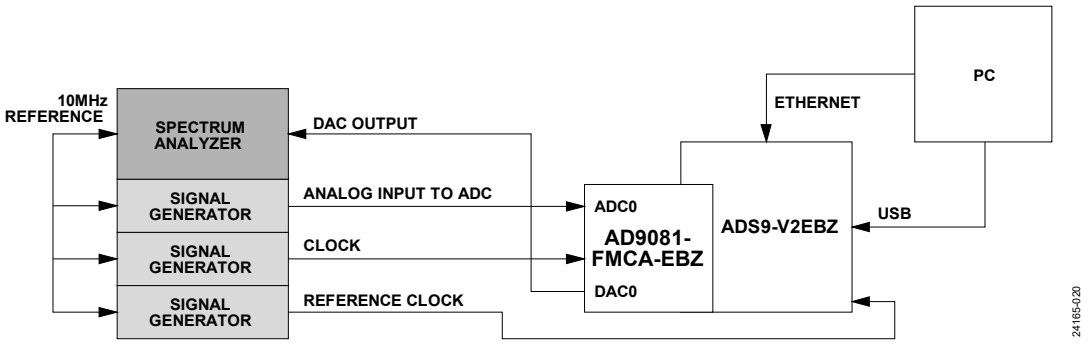

Figure 30. Hardware Setup for Using the Chip View (Note the 10 MHz Reference Connection)

6. Select the options for the other sections (**TX Link Configuration**, **Rx Link Configuration**, and **Clock Configuration**) in the **QUICK CONFIGURATION** pane as shown in Figure 31.
7. Click **Apply** to open the **Quick Configuration Summary** pane.
8. Click the **Proceed to Analysis** button for further analysis.

See the ADC Analysis and DAC Output Setup section and the Additional Use Cases and Customization section for more additional details.

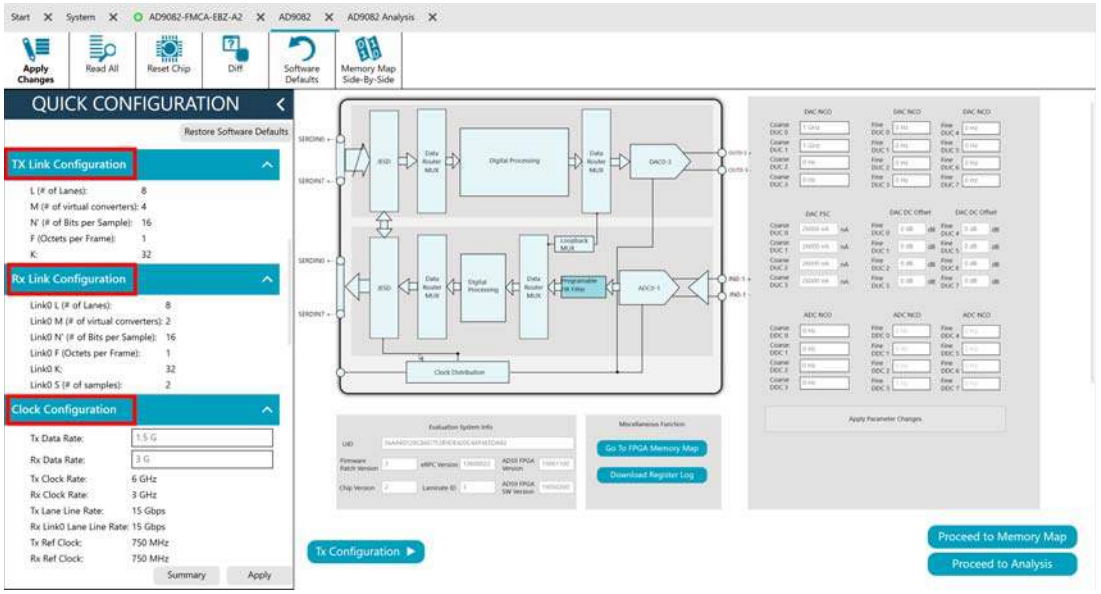

Figure 31. Configuring the AD9081 or AD9082 for Full Bandwidth Mode Using Chip View and the Direct External Clock

ADDITIONAL FEATURES

USING THE AD-FMC-SDCARD

This section explains how to use the supplied microSD card, AD-FMC-SDCARD, to evaluate the AD9081, AD9082, AD9986, or AD9988 using FPGA development boards from Intel or Xilinx.

The AD-FMC-SDCARD is a microSD Card and SD card adapter (to use the microSD card in an SD card slot), preformatted with an Analog Devices supported Linux image on it, which can be used for development and prototyping with the AD9081-FMCA-EBZ or the AD9082-FMCA-EBZ on Xilinx Zynq®, Zynq UltraScale+™, and Intel system on a chip (SoC) platforms. The AD-FMC-SDCARD uses a publicly facing hardware description language (HDL) and software reference design to enable the use of this hardware setup for algorithmic prototyping and development. For more information, visit wiki.analog.com/ad-fmc-sdcard. For questions about the contents on this card, ask on the Analog Devices EngineerZone at ez.analog.com/fpga for HDL questions or ez.analog.com/linux-software-drivers for software questions.

USING THE ADS9V2-UZSD-MXFE

This section explains how to use the supplied ADS9V2-UZSD-MXFE microSD card. Insert this microSD card in the slot as described in the MicroSD Card for the MicroZed Board section. This microSD card enables the user to evaluate the AD9081, AD9082, AD9986, or AD9988 using the available **TxFE/MxFE Eval App Extras**, which is an app on the ADS9V2-UZSD-MXFE microSD Card. More information is available in the documentation supplied with the application programming interface (API) framework. The API can be downloaded by going to www.analog.com/srf and submitting a request.

ADDITIONAL USE CASES AND CUSTOMIZATION

The ACE plugin for the AD9081, AD9082, AD9986, or AD9988 supports additional use cases and some level of customization. Because these are highly configurable devices, not all these modes are described in this user guide. Additional example use cases and features are described on the Analog Devices wiki site at wiki.analog.com/resources/eval/ad9082.

TROUBLESHOOTING TIPS

EVALUATION BOARD FUNCTIONING

If the evaluation board is not functioning properly, take the following steps:

1. Ensure that the evaluation board is properly seated in the FMC connector.
2. After ACE has programmed the FPGA, power is provided to the evaluation board for the AD908x-FMCA-EBZ board. For the AD998x-FMCA-EBZ version of the boards, power is provided externally through the 12 V connector. Ensure that the LEDs that denote power are all lit. See Figure 32.

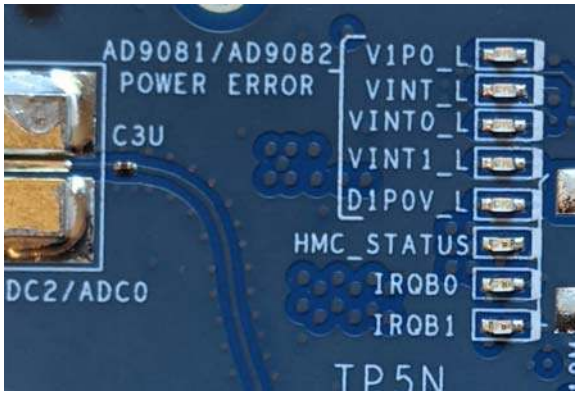

Figure 32. LEDs Denoting Power to the Various Rails on the Evaluation Board

3. Ensure that the eRPC server has made a successful connection to the evaluation board. If the chip information reads back a successful user identification (UID), this means that the connection is successful. Otherwise, the UID reads 0x0 (see Figure 13). If this is the case, power cycle the evaluation board and restart all software.

ACE SPEED ISSUES

If ACE is slow to capture data and setup the evaluation board, take the following steps:

1. Ensure that the USB connection between the ADS9-V2EBZ board and the PC is done through a USB 3.0 cable.
2. Connect the cable to a USB 3.0 supported port on the PC.
3. Restart all software and hardware.

DATA CAPTURED ISSUES AFTER SETUP

In some instances, users may be unable to capture data from the FPGA, which is characterized by no capture within the ACE software or as a configure channel failed error in the ACE software. In either case, only four of the six LEDs on the FPGA board are lit (see Figure 33).

Figure 33. LED Status on ADS9-V2EBZ Following an Unsuccessful Data Capture

If this happens, and the setup is using an external direct clock to the chip, ensure that the instrumentation is setup as shown in Figure 30. Ensure the correct clock and reference clock frequencies are set. Check the connections to the evaluation board to ensure that the connections are snug. If the problem persists, open the DPGDownloaderLite software (included with the ACE installation) and download a tone (see Figure 28). After this step, a successful data capture shows all the LEDs lit (see Figure 34).

Figure 34. LED Status on ADS9-V2EBZ Following a Successful Data Capture

HMC7044 CONFIGURATION ERROR

When operating using the on-board clocking and the on-chip PLL mode, the user can get a HMC7044 configuration error in the ACE software setup (see Figure 35). If this happens, ensure that the correct modes are selected to setup the chip. Not all modes listed in the UG-1578 are supported by the evaluation board hardware using the on-board HMC7044 clock and on-chip PLL mode. Note that the HMC7044 derives its reference from a 100 MHz crystal oscillator if using the AD908x-FMCA-EBZ version of the evaluation board or a 122.88 MHz crystal oscillator if using the AD998x-FMCB-EBZ version of the evaluation board.

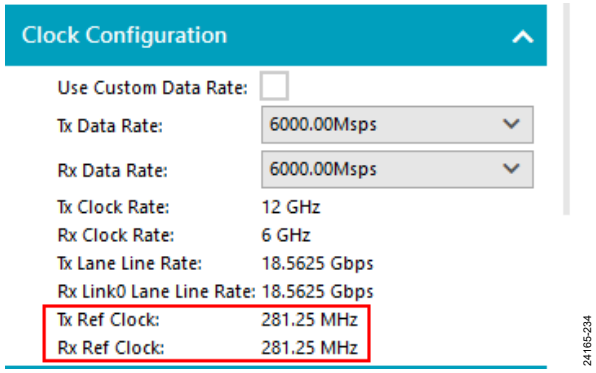

Figure 35. HMC7044 Configuration Error (Reference Clock Value Not Supported When Using a 100 MHz Crystal Oscillator)

If this use case is required, the best approach is to switch to using the direct external clock. This approach bypasses the HMC7044 setup, and the user is not limited to the setup options provided by the combination of the on-board crystal oscillator and the HMC7044 setup.