

DSP Pro Development Board

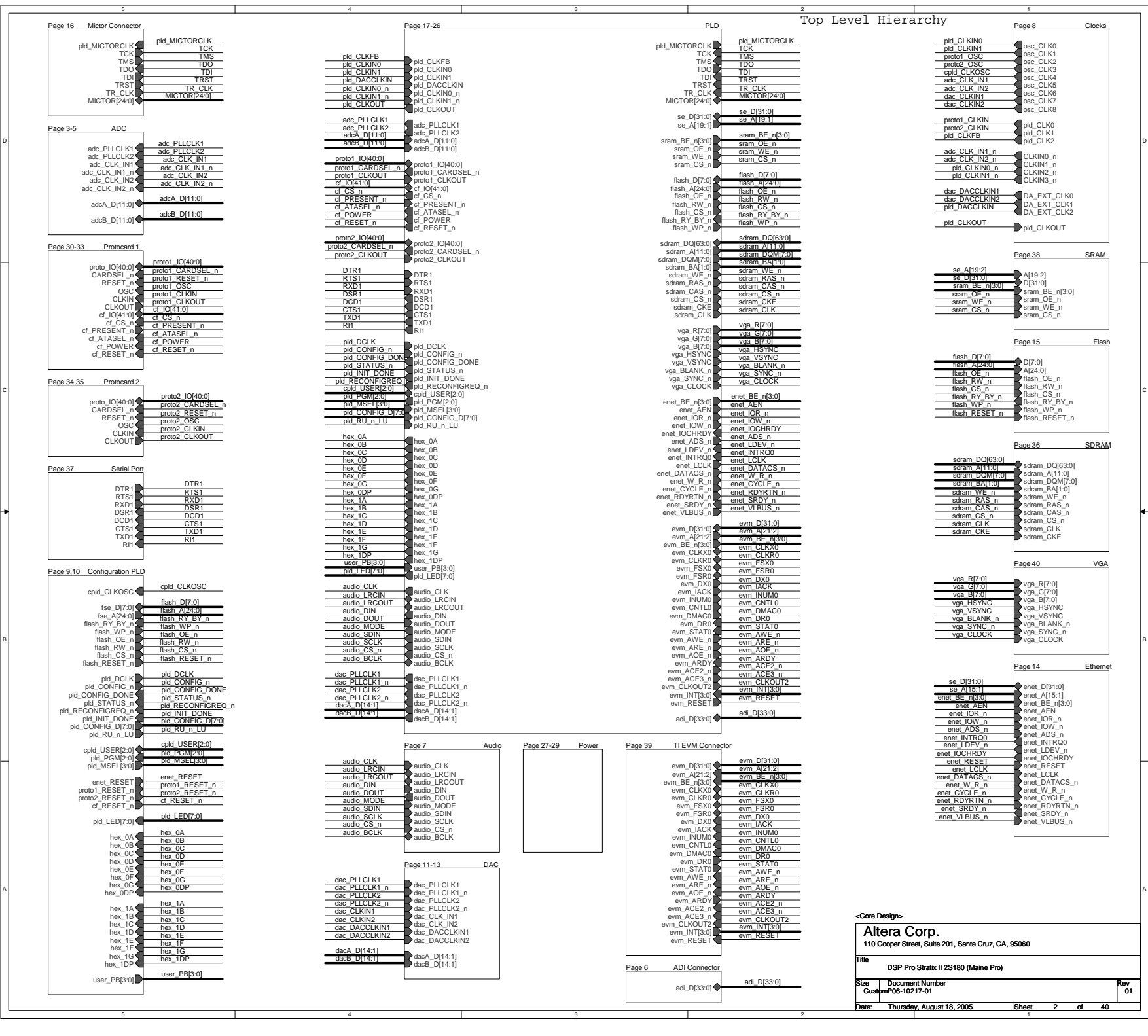
Stratix II 2S180 Edition

Rev 01

Revision History		
Date	Change Description	Rev
8/18/05	Created schematic and changed the component from the 2S60 on the DSP board to the 2S180 on this Pro version of the board	01

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Size A	Document Number P06-10217-01	Rev 01
Date:	Thursday, August 18, 2005	Sheet 1 of 40



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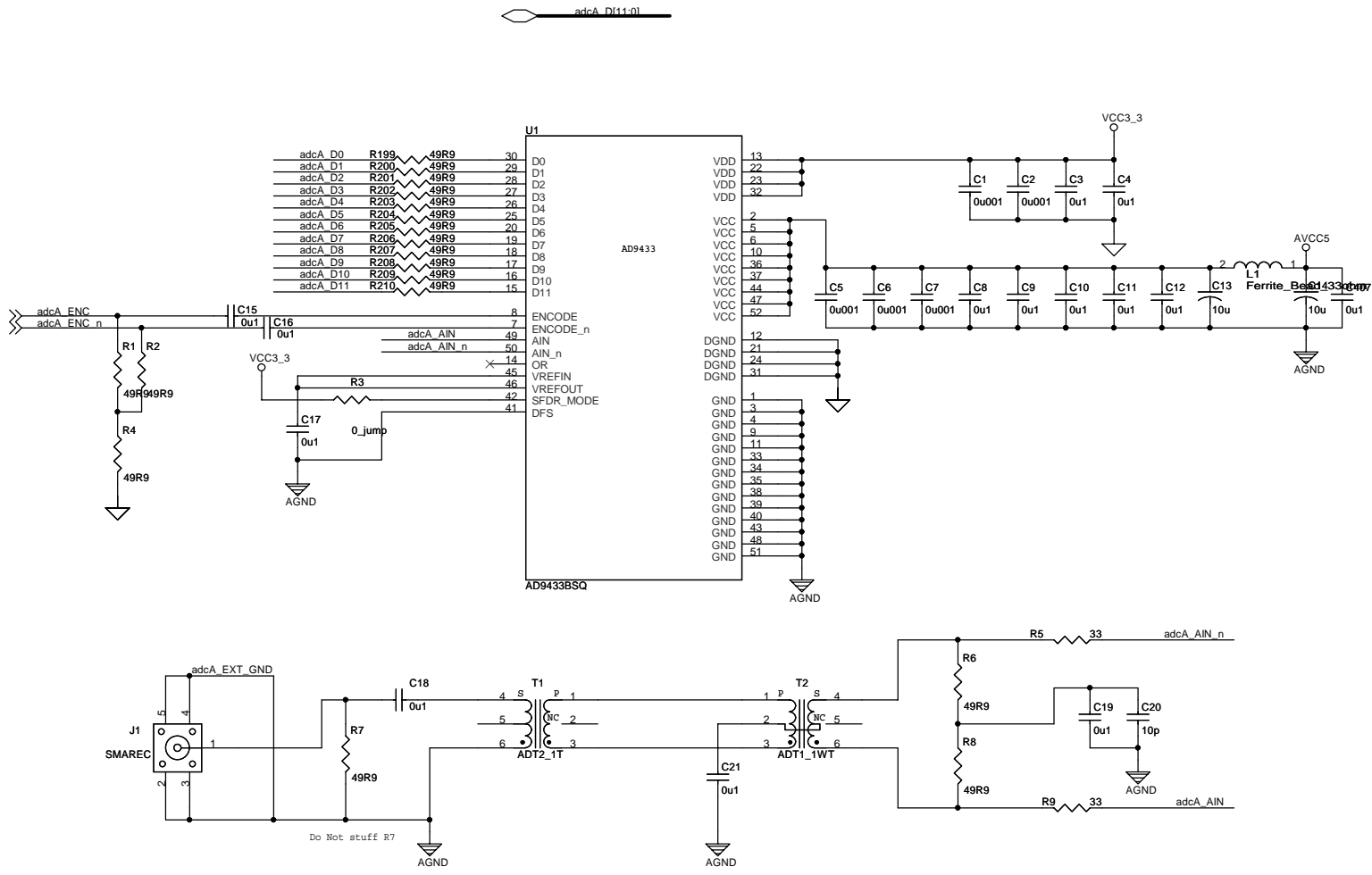
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Size: Document Number
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Date: Thursday, August 18, 2005

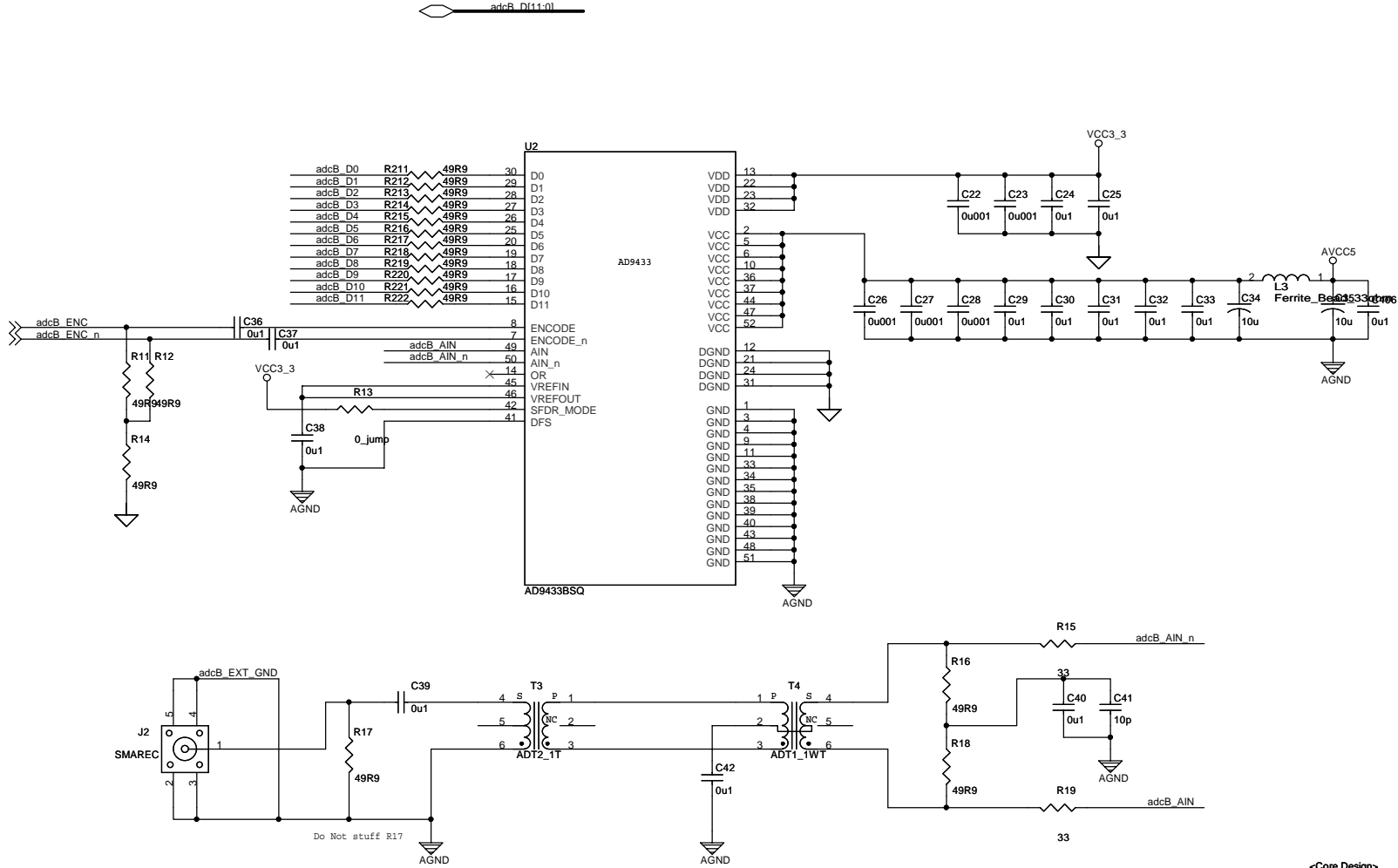
Sheet: 2 of 40

Rev: 01



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Title DSP Pro Stratix II 2S180 (Maine Pro)		
Size B	Document Number P06-10217-01	Rev 01
Date:	Thursday, August 18, 2005	Sheet 3 of 40

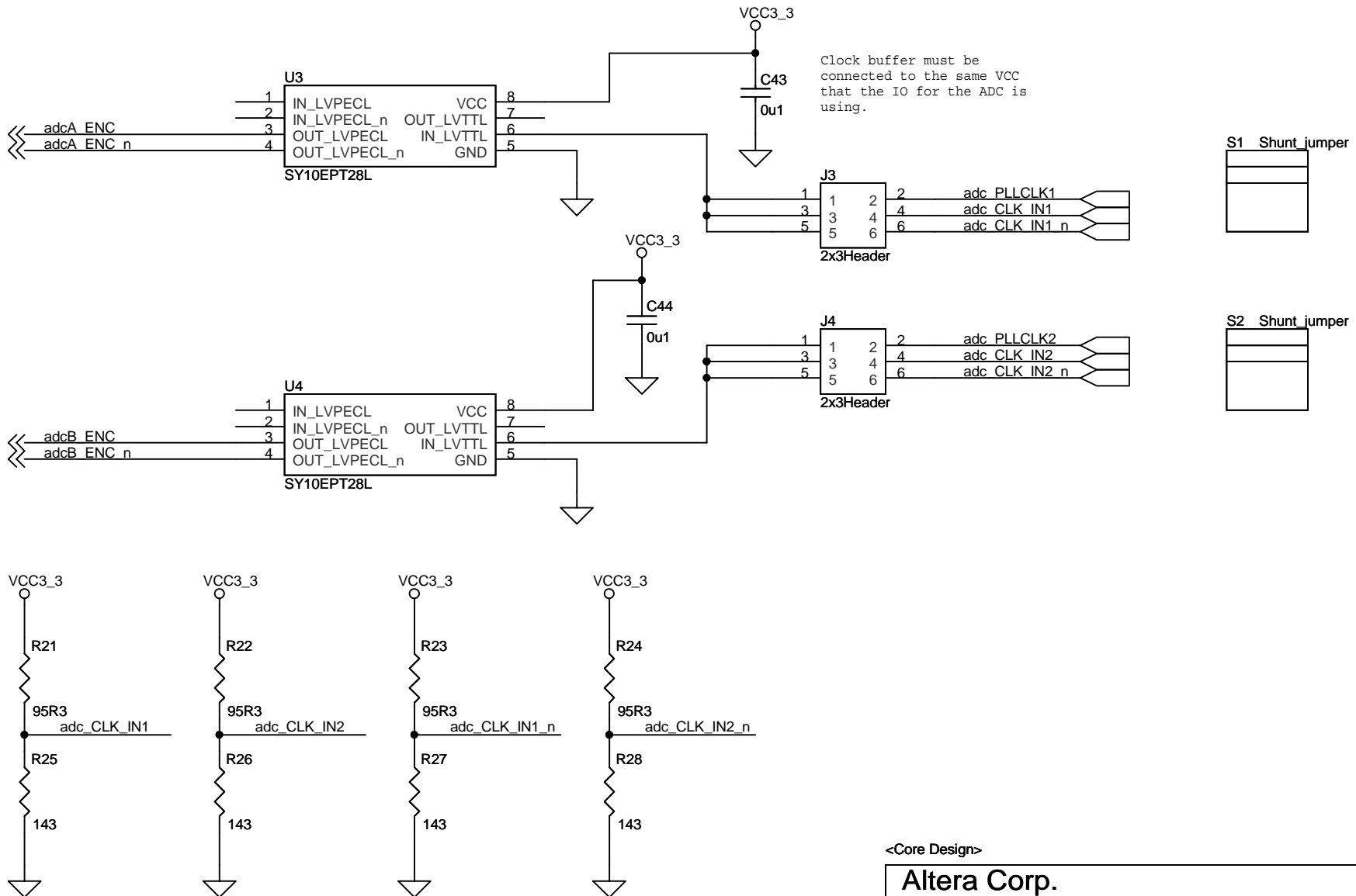


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Title		
DSP Pro Stratix II 2S180 (Maine Pro)		
Size	Document Number	Rev
B	P06-10217-01	01
Date:	Thursday, August 18, 2005	Sheet 4 of 40

ADC Clock Selection



Clock buffer must be connected to the same VCC that the IO for the ADC is using.

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Size

Document Number
P06-10217-01

Rev

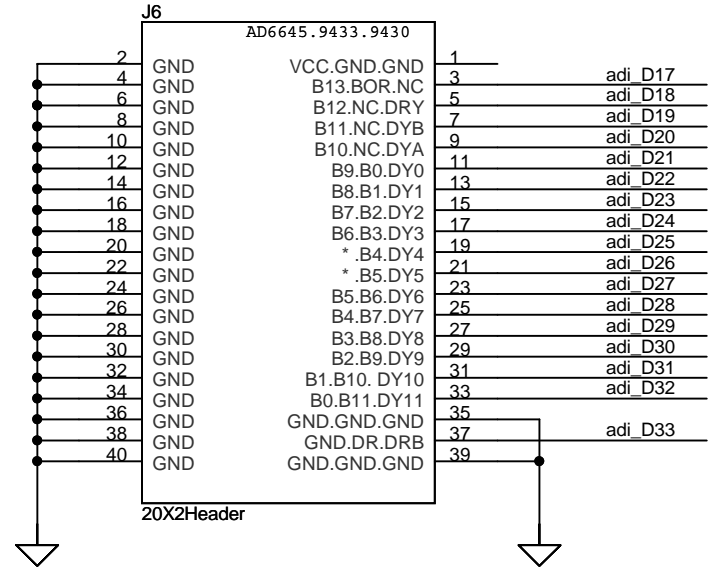
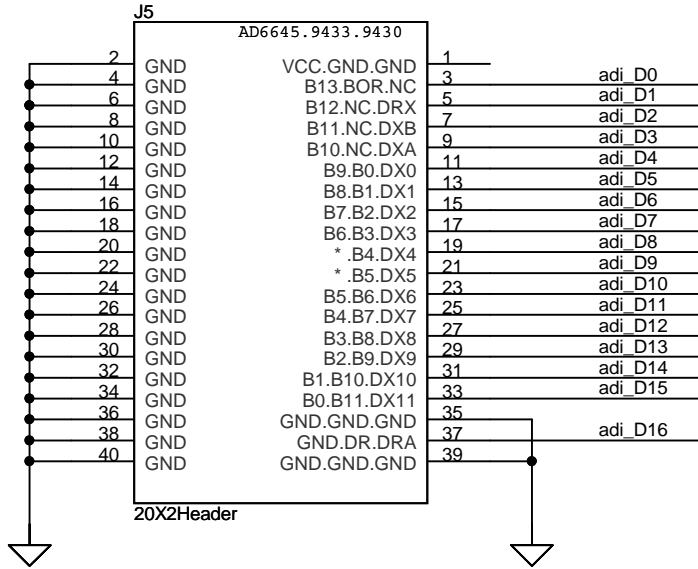
01

Date: Thursday, August 18, 2005

Sheet 5 of 40

ADI Connector

adi_D[33:0]



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Document Number

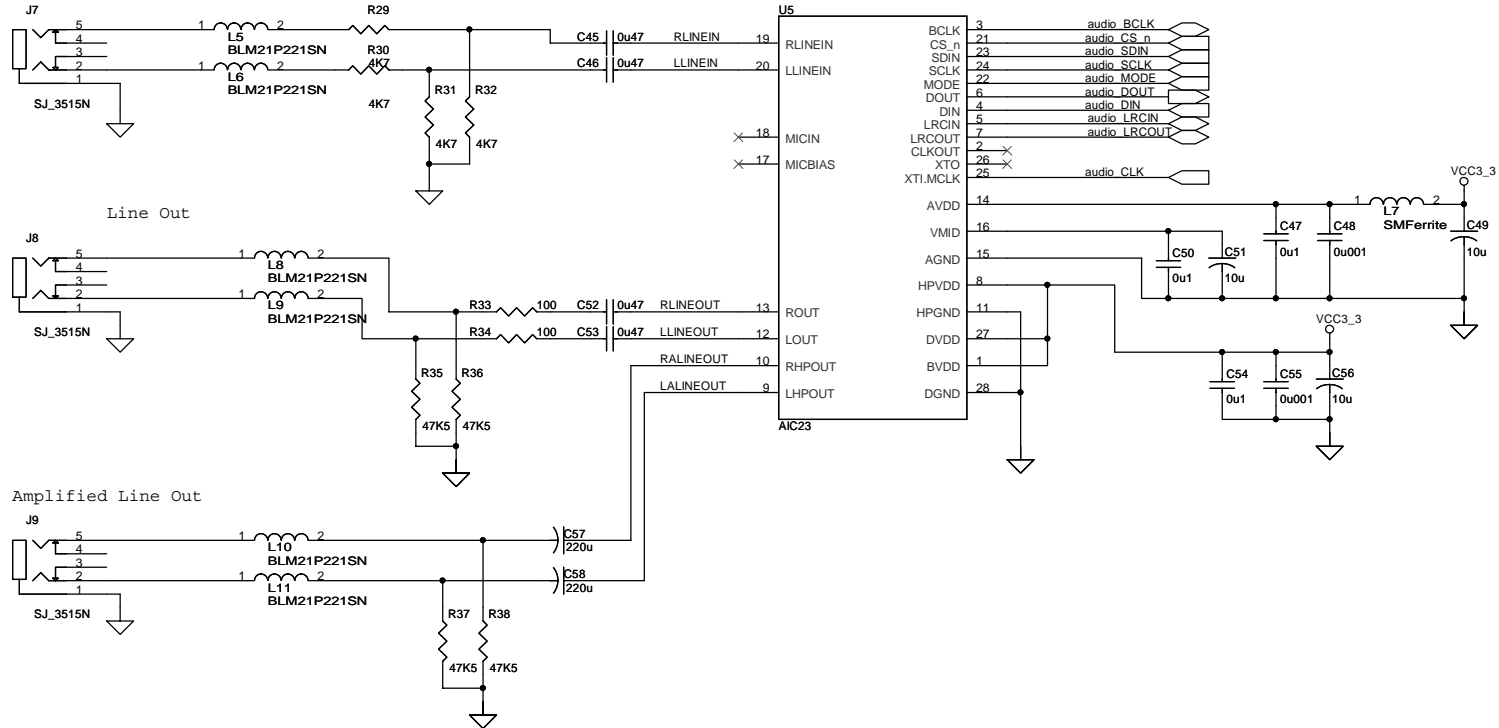
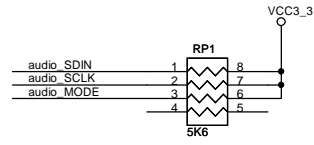
Rev

P06-10217-01

01

Date: Thursday, August 18, 2005

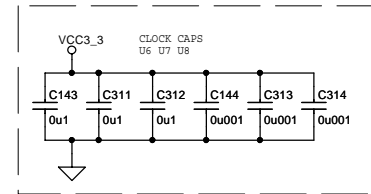
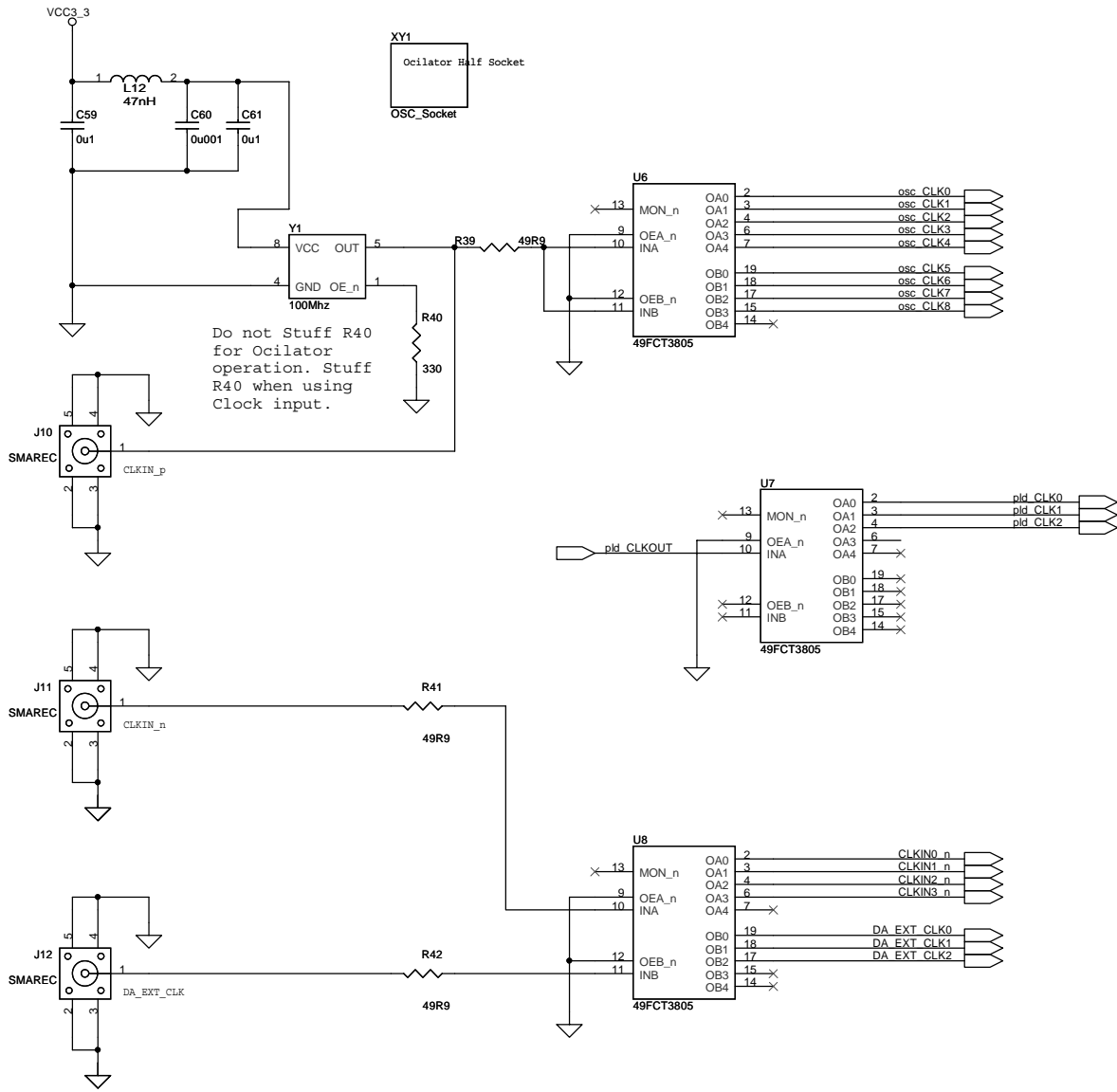
Sheet 6 of 40



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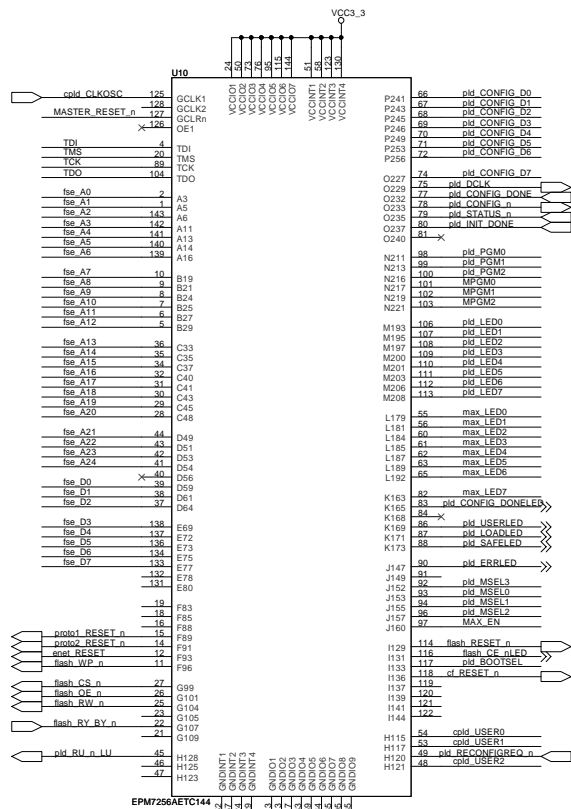
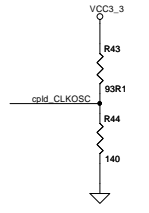
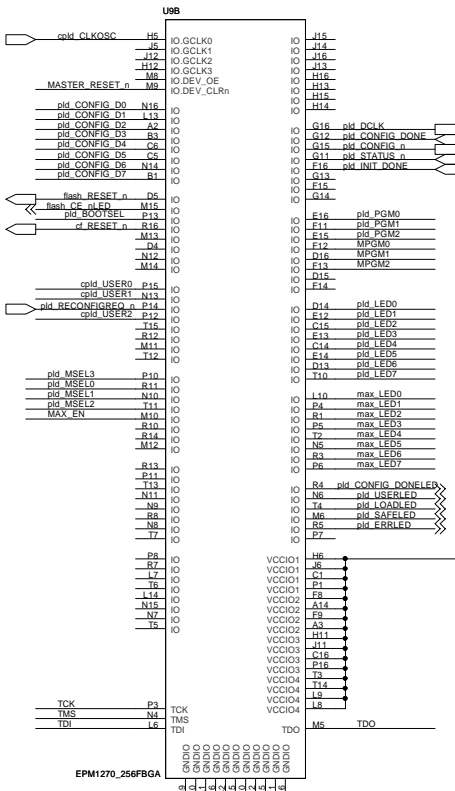
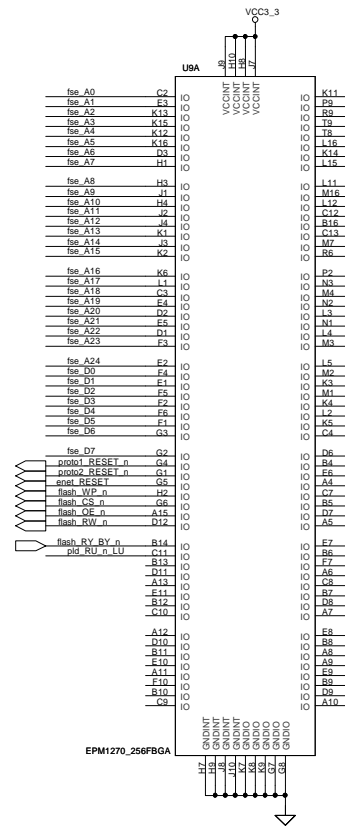
Title		
DSP Pro Stratix II 2S180 (Maine Pro)		
Size	Document Number	Rev
B	P06-10217-01	01
Date:	Thursday, August 18, 2005	Sheet 7 of 40



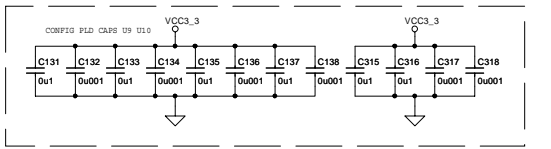
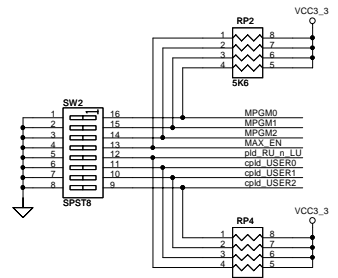
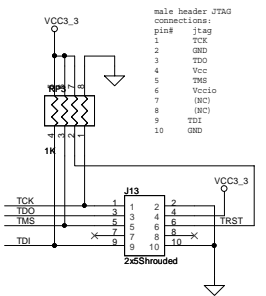
<Core Design>

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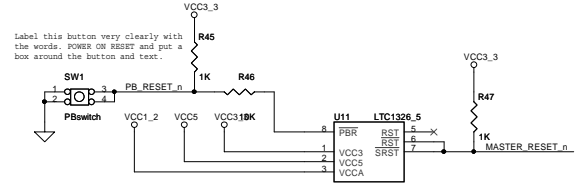
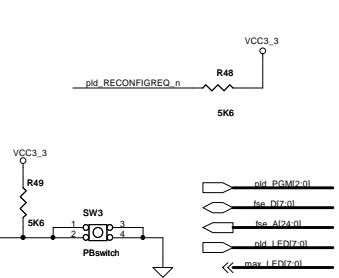
Title		
DSP Pro StratiX II 2S180 (Maine Pro)		
Size	Document Number	Rev
B	P06-10217-01	01
Date:	Thursday, August 18, 2005	Sheet 8 of 40



Configuration PLD

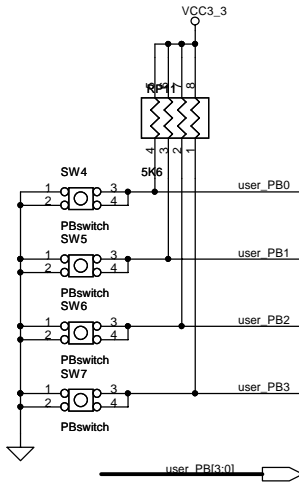
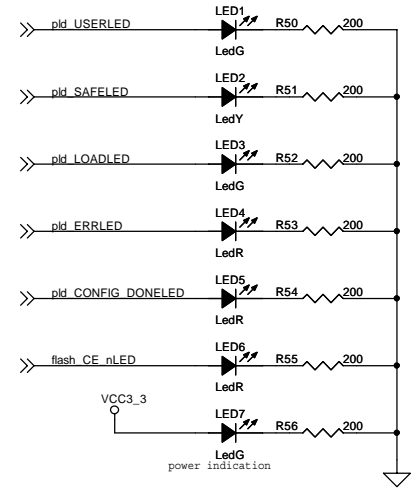
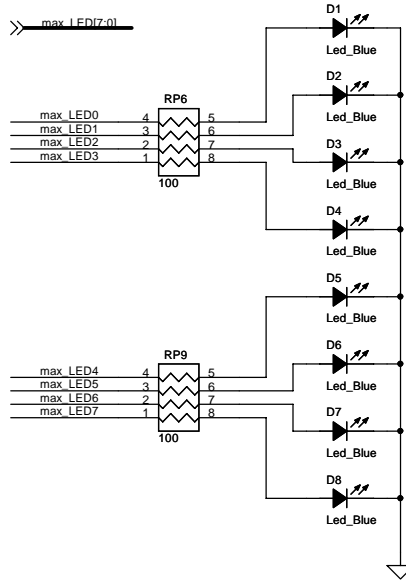
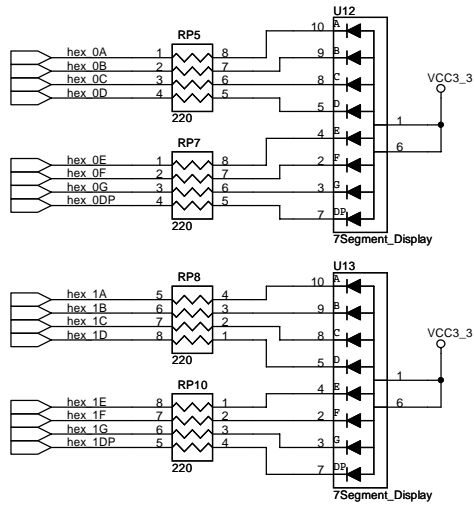


pld_BOOTSEL determines whether to force a boot from the default boot sector, or the user-programmed boot sector.



- ◊ pld_PGM2[0]
- ◊ fse_D17[0]
- ◊ fse_A17[0]
- ◊ pld_LED7[0]
- ◊ pld_USER12[0]
- ◊ pld_MSEL3[0]
- ◊ pld_CONFIG_D17[0]

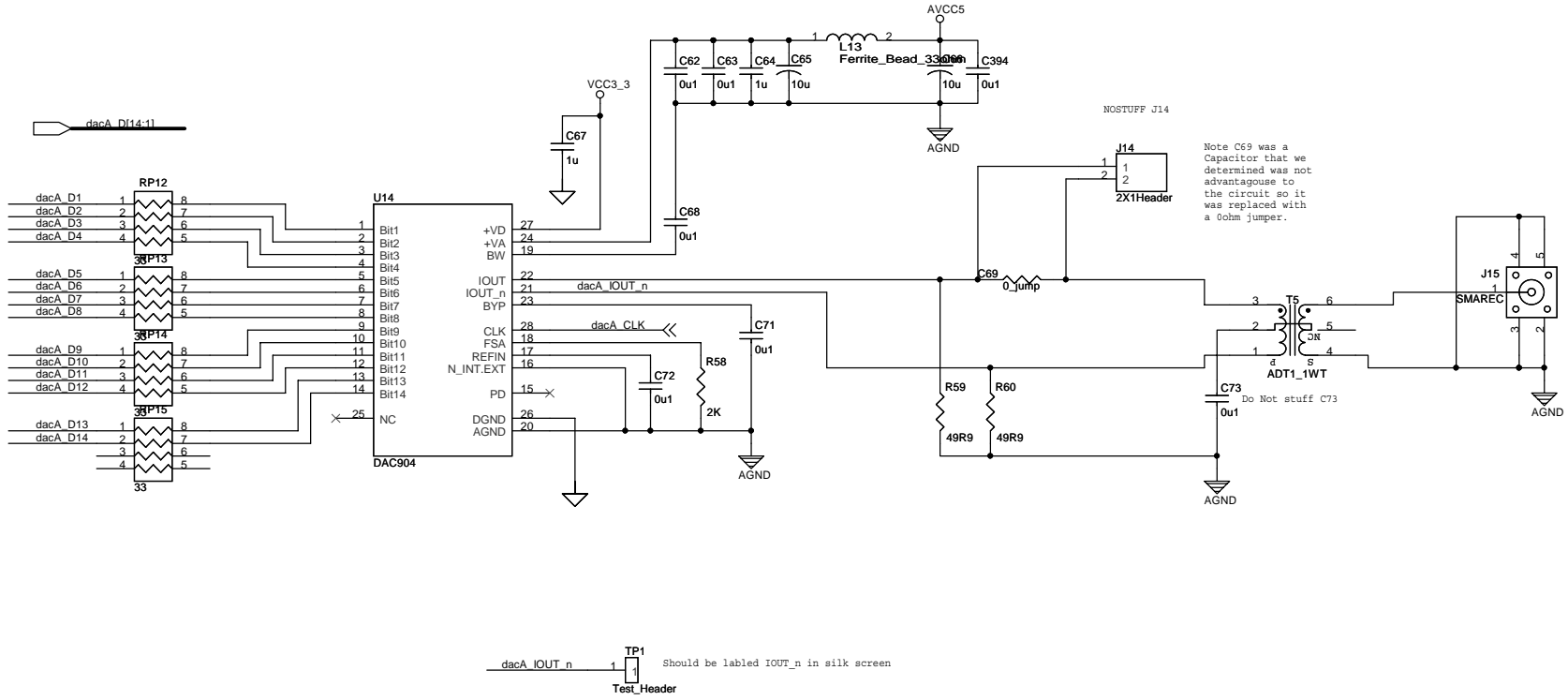
<Core Design>
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Title DSP Pro Stratix II ZS180 (Maine Pro)
Size Document Number P06-10217-01
Date: Thursday, August 18, 2005 **Sheet** 9 of 40 **Rev** 01



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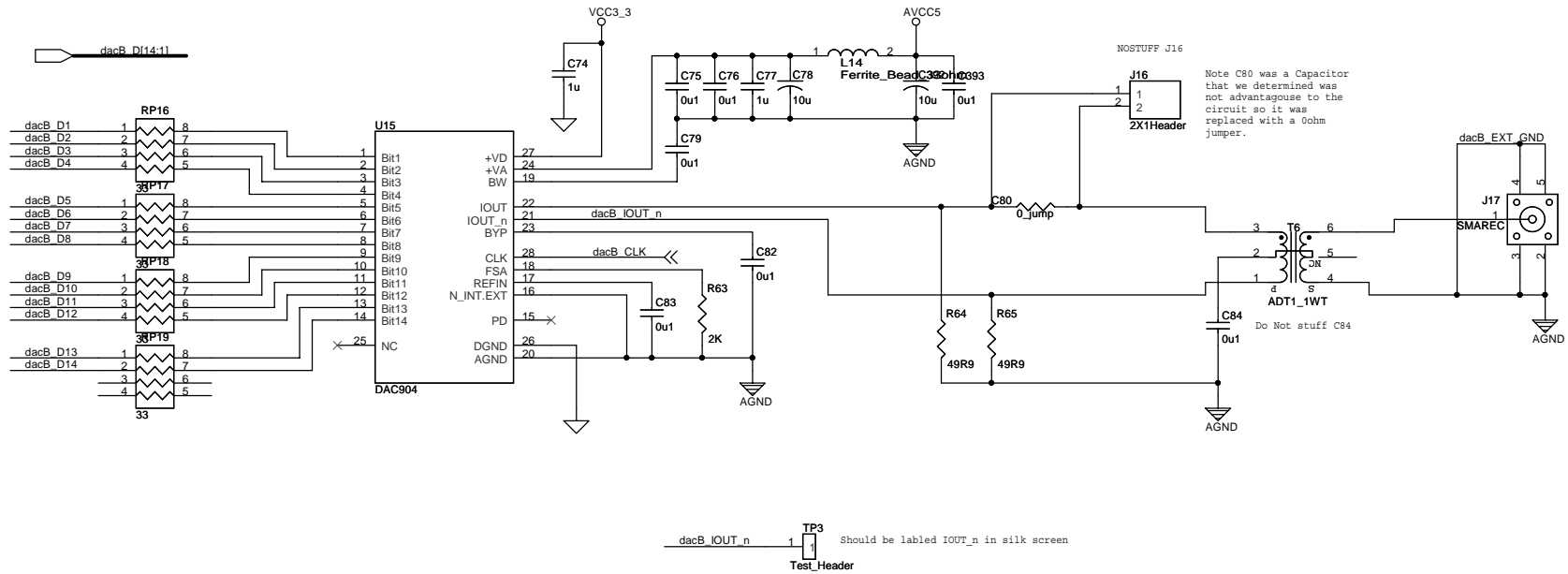
Title		
DSP Pro Stratix II 2S180 (Maine Pro)		
Size	Document Number	Rev
B	P06-10217-01	01
Date:	Thursday, August 18, 2005	Sheet 10 of 40



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Title		
DSP Pro Stratix II 2S180 (Maine Pro)		
Size	Document Number	Rev
B	P06-10217-01	01
Date:	Thursday, August 18, 2005	Sheet 11 of 40



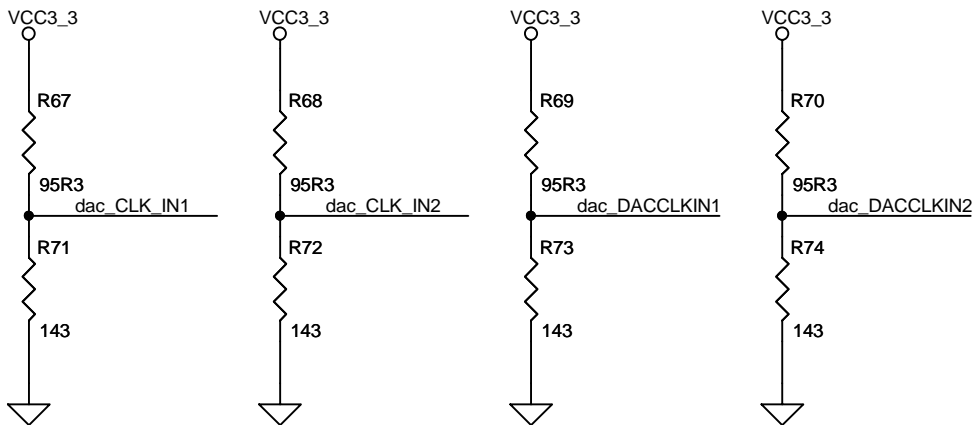
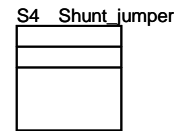
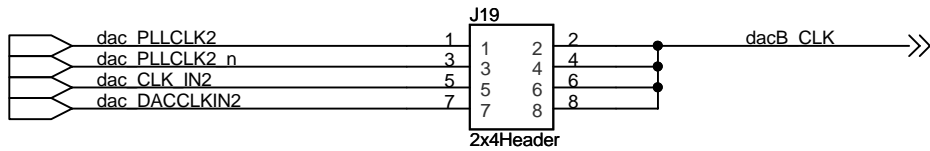
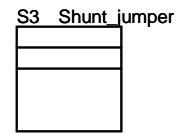
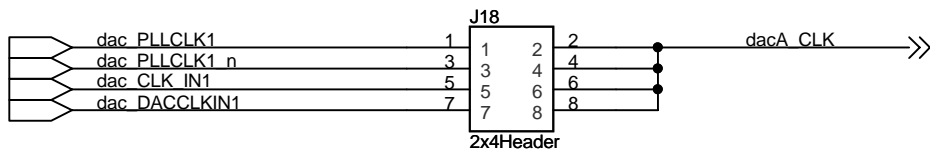
Note C80 was a Capacitor that we determined was not advantageous to the circuit so it was replaced with a 0ohm jumper.

Do Not stuff C84

TP3
Test_Header
Should be labeled IOUT_n in silk screen

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Title		
DSP Pro Stratix II 2S180 (Maine Pro)		
Size	Document Number	Rev
B	P06-10217-01	01
Date:	Thursday, August 18, 2005	Sheet 12 of 40

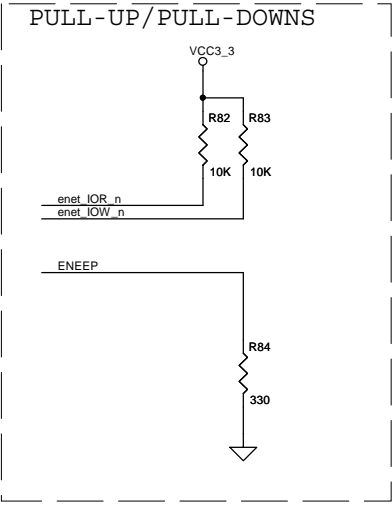
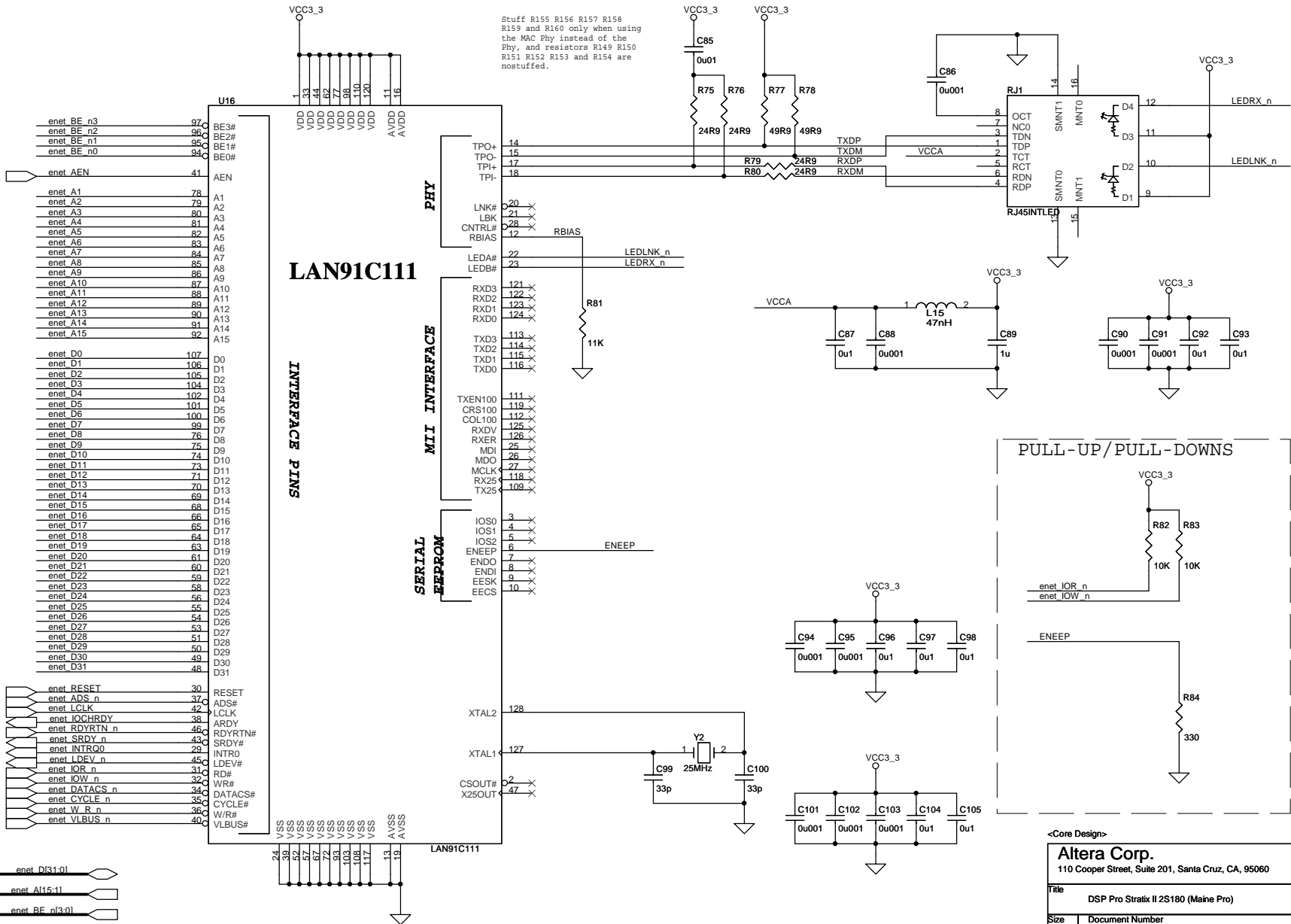
DAC Clock Jumper



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Title DSP Pro Stratix II 2S180 (Maine Pro)		
Size A	Document Number P06-10217-01	Rev 01
Date:	Thursday, August 18, 2005	Sheet 13 of 40

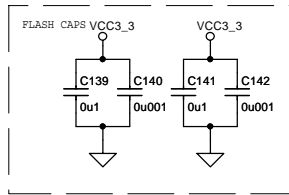
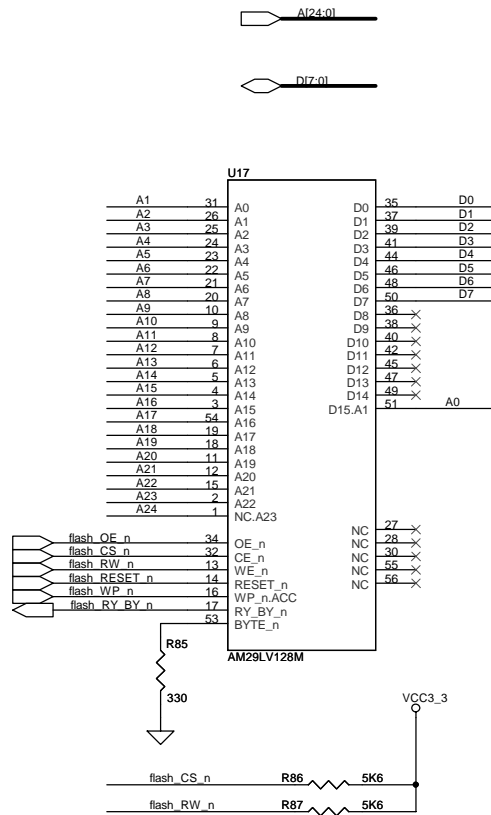
Stuff R155 R156 R157 R158 R159 and R160 only when using the MAC Phy instead of the Phy, and resistors R149 R150 R151 R152 R153 and R154 are not stuffed.



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Title		DSP Pro Stratix II 2S180 (Maine Pro)	
Size	Document Number	Rev	
B	P06-10217-01	01	
Date:	Thursday, August 18, 2005	Sheet	14 of 40



Flash chip is 16M x 8 for 16Mbytes of flash

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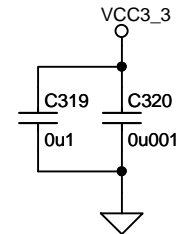
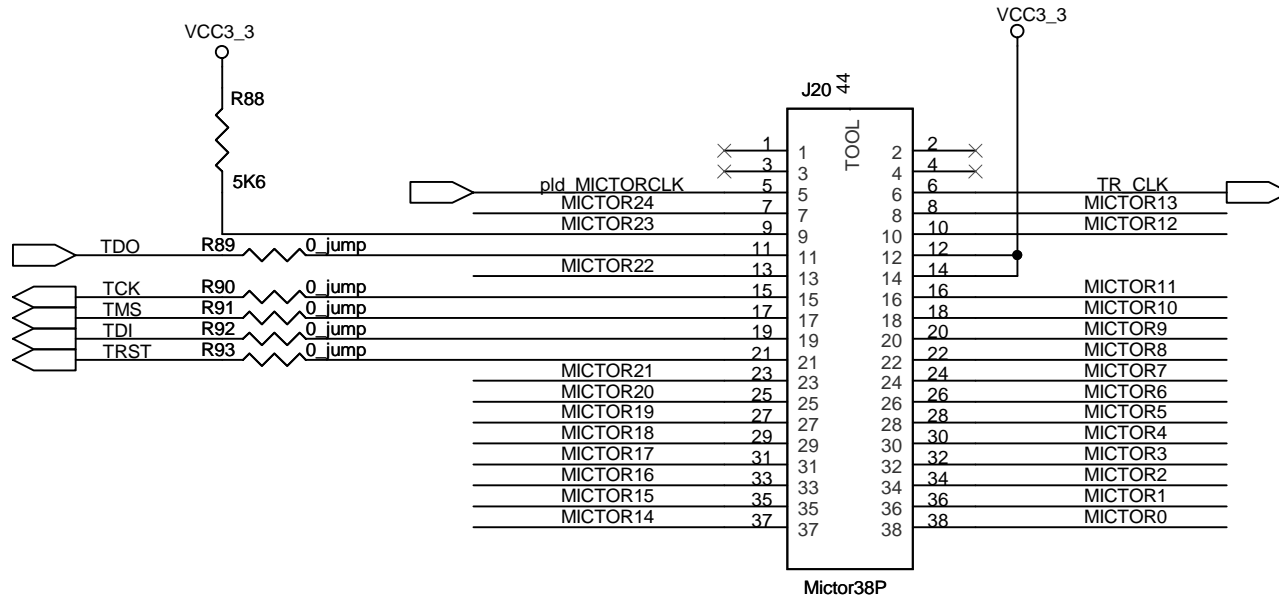
Title
DSP Pro Stratix II 2S180 (Maine Pro)

Size Document Number
CustomP06-10217-01

Rev
01

Date: Thursday, August 18, 2005 Sheet 15 of 40

Mictor Connector



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DSP Pro Stratix II 2S180 (Maine Pro)

Size

Document Number

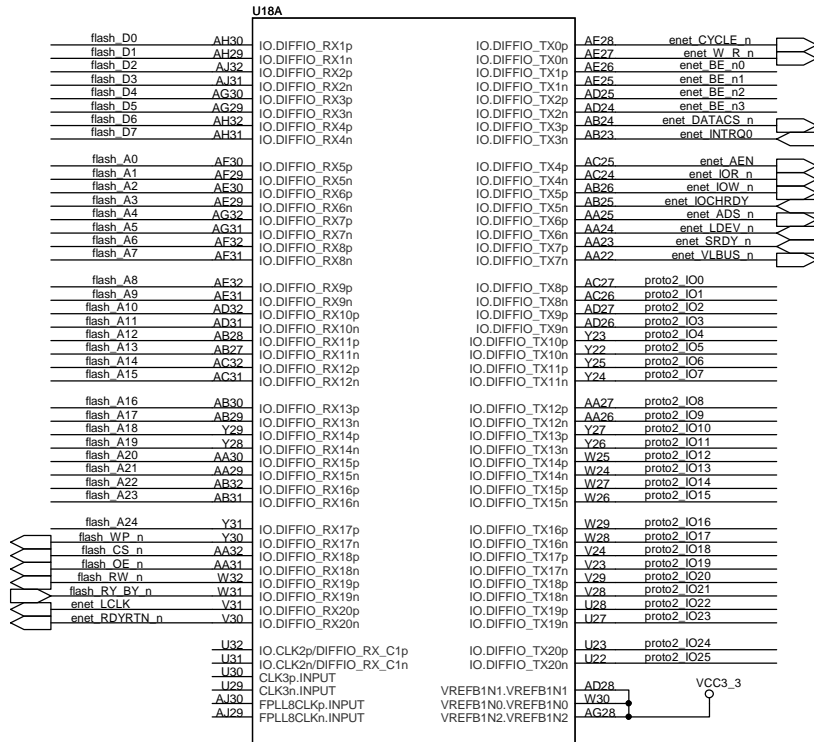
Rev

A P06-10217-01

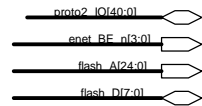
01

Date: Thursday, August 18, 2005

Sheet 16 of 40



EP2S180F1020C3



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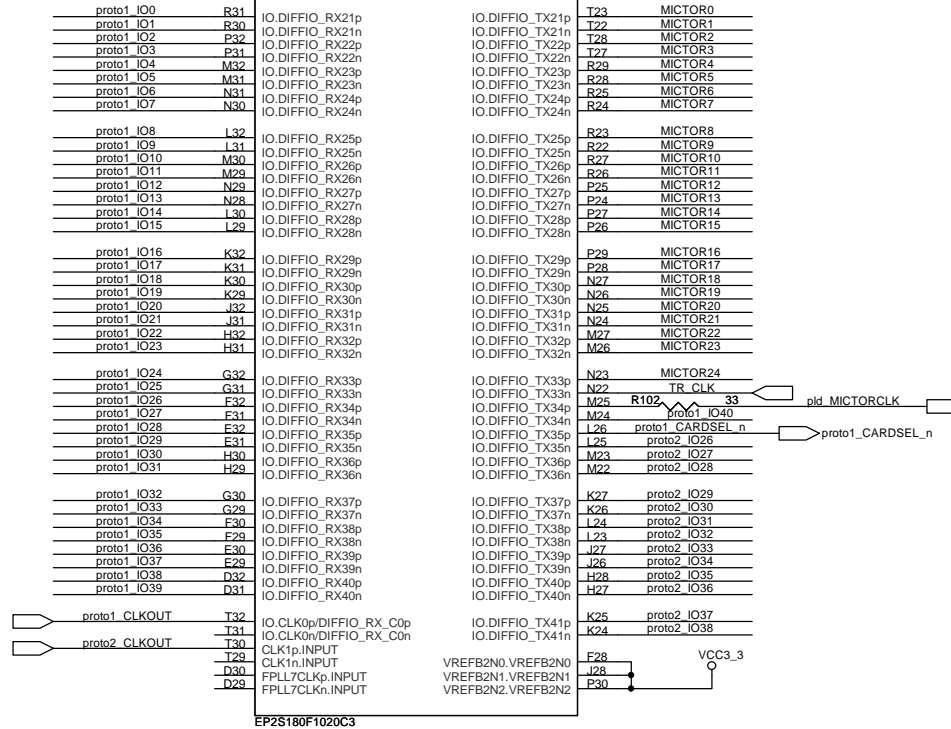
Title: DSP Pro Stratix II 2S180 (Maine Pro)

Size	Document Number	Rev
B	P06-10217-01	01

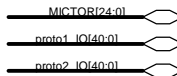
Date: Thursday, August 18, 2005 Sheet 17 of 40

PLD Bank 2

U18B



EP2S180F1020C3

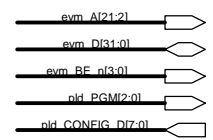
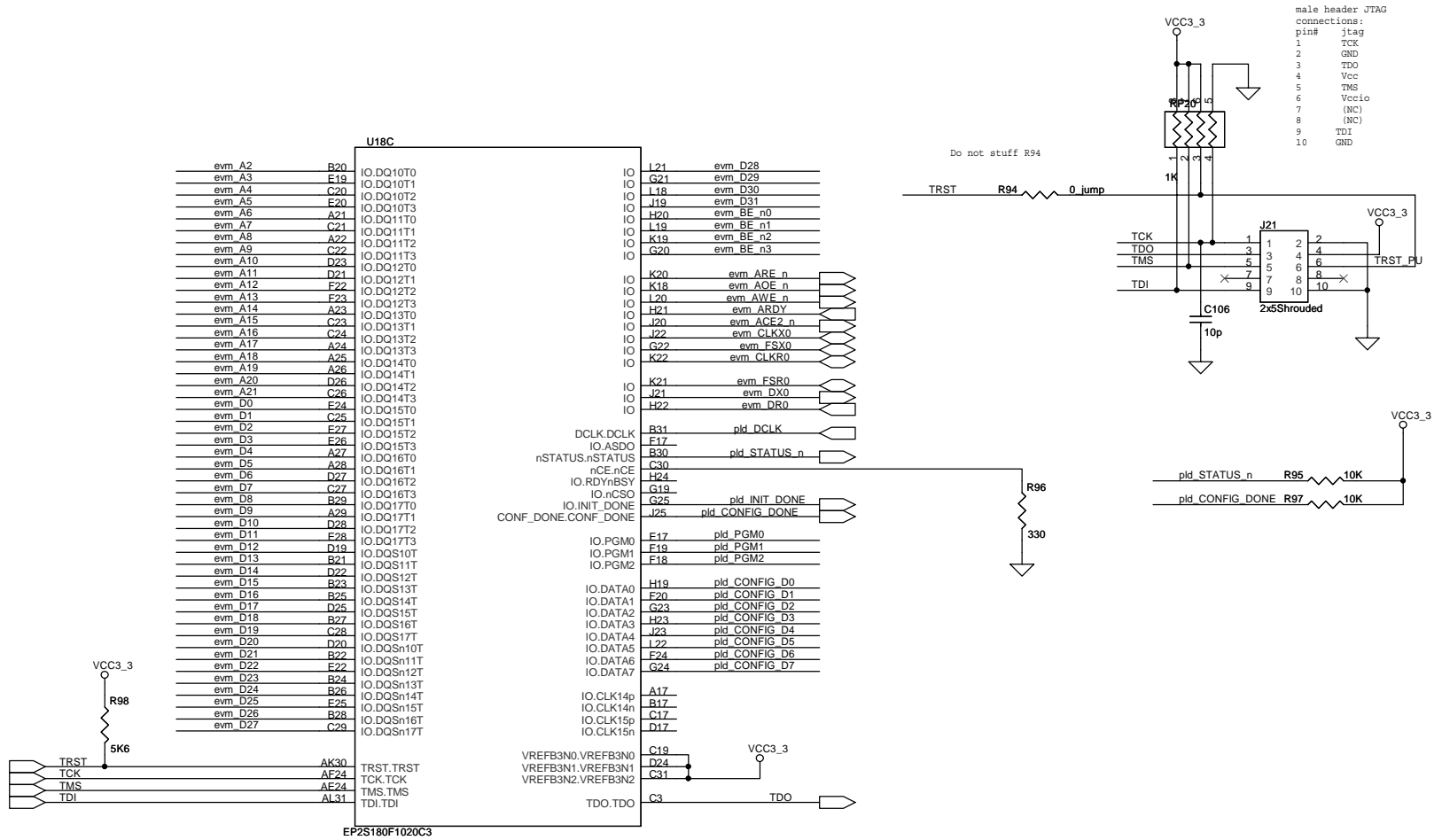


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Title		
DSP Pro Stratix II 2S180 (Maine Pro)		
Size	Document Number	Rev
B	P06-10217-01	01
Date:	Thursday, August 18, 2005	Sheet 18 of 40

PLD Bank 3



<Core Design>

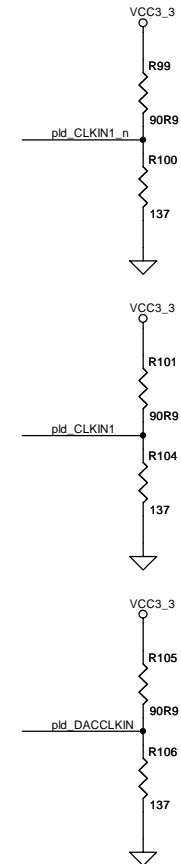
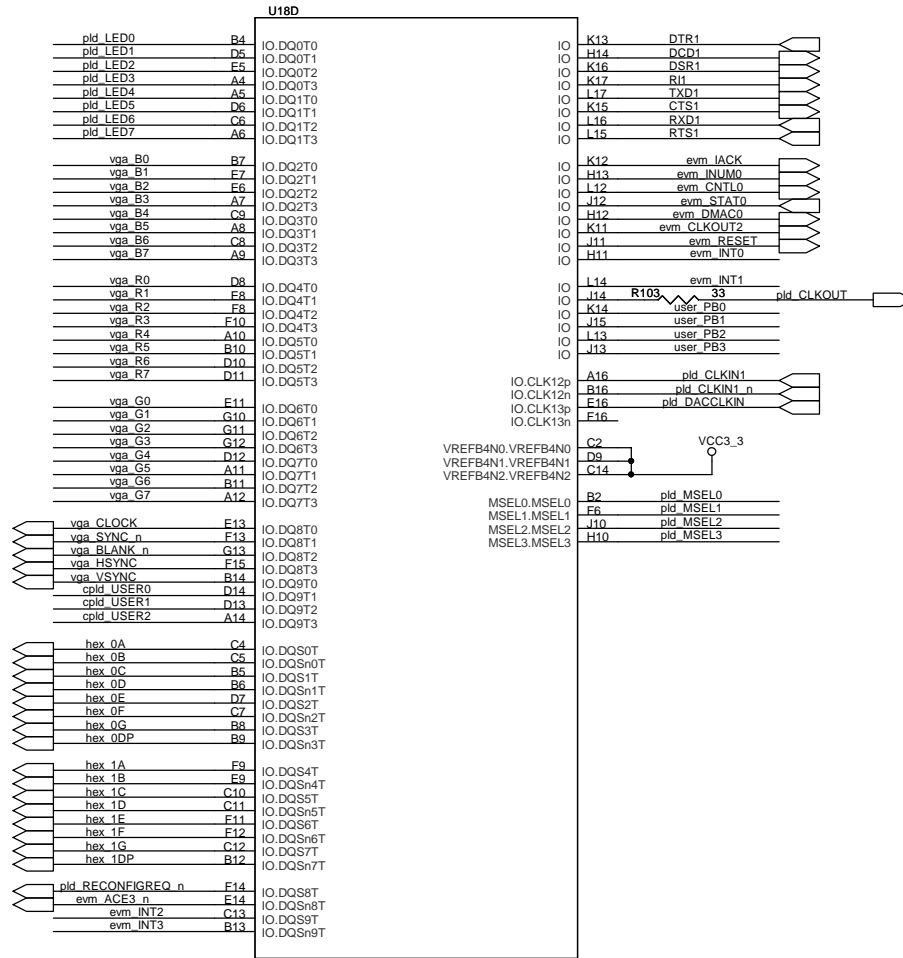
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Title: DSP Pro Stratix II 2S180 (Maine Pro)

Size B	Document Number P06-10217-01	Rev 01
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Date: Thursday, August 18, 2005 Sheet 19 of 40

PLD Bank 4



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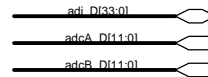
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Title		
DSP Pro Stratix II 2S180 (Maine Pro)		
Size	Document Number	Rev
B	P06-10217-01	01
Date:	Thursday, August 18, 2005	Sheet 20 of 40

U18E

adcA_D0	D1	IO.DIFFIO_RX43p	IO.DIFFIO_TX42p	J6	adi_D16
adcA_D1	D2	IO.DIFFIO_RX43n	IO.DIFFIO_TX42n	J7	adi_D17
adcA_D2	E3	IO.DIFFIO_RX44p	IO.DIFFIO_TX43p	J8	adi_D18
adcA_D3	E4	IO.DIFFIO_RX44n	IO.DIFFIO_TX43n	J9	adi_D19
adcA_D4	F1	IO.DIFFIO_RX45p	IO.DIFFIO_TX44p	K8	adi_D20
adcA_D5	F2	IO.DIFFIO_RX45n	IO.DIFFIO_TX44n	K9	adi_D21
adcA_D6	F3	IO.DIFFIO_RX46p	IO.DIFFIO_TX45p	L9	adi_D22
adcA_D7	F4	IO.DIFFIO_RX46n	IO.DIFFIO_TX45n	L10	adi_D23
adcA_D8	F1	IO.DIFFIO_RX47p	IO.DIFFIO_TX46p	L7	adi_D24
adcA_D9	F2	IO.DIFFIO_RX47n	IO.DIFFIO_TX46n	L8	adi_D25
adcA_D10	G3	IO.DIFFIO_RX48p	IO.DIFFIO_TX47p	K6	adi_D26
adcA_D11	G4	IO.DIFFIO_RX48n	IO.DIFFIO_TX47n	K7	adi_D27
adcB_D0	G1	IO.DIFFIO_RX49p	IO.DIFFIO_TX48p	L6	adi_D28
adcB_D1	G2	IO.DIFFIO_RX49n	IO.DIFFIO_TX48n	M10	adi_D30
adcB_D2	J3	IO.DIFFIO_RX50p	IO.DIFFIO_TX49p	M11	adi_D31
adcB_D3	J4	IO.DIFFIO_RX50n	IO.DIFFIO_TX49n		
adcB_D4	H1	IO.DIFFIO_RX51p	IO.DIFFIO_TX50p	M8	adi_D32
adcB_D5	H2	IO.DIFFIO_RX51n	IO.DIFFIO_TX50n	M9	adi_D33
adcB_D6	J1	IO.DIFFIO_RX52p	IO.DIFFIO_TX51p	M6	
adcB_D7	J2	IO.DIFFIO_RX52n	IO.DIFFIO_TX51n	M7	
adcB_D8	K3	IO.DIFFIO_RX53p	IO.DIFFIO_TX52p	N6	
adcB_D9	K4	IO.DIFFIO_RX53n	IO.DIFFIO_TX52n	N7	
adcB_D10	K1	IO.DIFFIO_RX54p	IO.DIFFIO_TX53p	N8	
adcB_D11	K2	IO.DIFFIO_RX54n	IO.DIFFIO_TX53n	N9	
adi_D0	L3	IO.DIFFIO_RX55p	IO.DIFFIO_TX54p	P8	
adi_D1	L4	IO.DIFFIO_RX55n	IO.DIFFIO_TX54n	P9	
adi_D2	N4	IO.DIFFIO_RX56p	IO.DIFFIO_TX55p	P6	
adi_D3	N5	IO.DIFFIO_RX56n	IO.DIFFIO_TX55n	P7	
adi_D4	M3	IO.DIFFIO_RX57p	IO.DIFFIO_TX56p	P4	
adi_D5	M4	IO.DIFFIO_RX57n	IO.DIFFIO_TX56n	P5	
adi_D6	L1	IO.DIFFIO_RX58p	IO.DIFFIO_TX57p	P10	
adi_D7	L2	IO.DIFFIO_RX58n	IO.DIFFIO_TX57n	P11	
adi_D8	N2	IO.DIFFIO_RX59p	IO.DIFFIO_TX58p	R6	
adi_D9	N3	IO.DIFFIO_RX59n	IO.DIFFIO_TX58n	R7	
adi_D10	M1	IO.DIFFIO_RX60p	IO.DIFFIO_TX59p	R4	
adi_D11	M2	IO.DIFFIO_RX60n	IO.DIFFIO_TX59n	R5	
adi_D12	R2	IO.DIFFIO_RX61p	IO.DIFFIO_TX60p	R10	
adi_D13	R3	IO.DIFFIO_RX61n	IO.DIFFIO_TX60n	R11	
adi_D14	P1	IO.DIFFIO_RX62p	IO.DIFFIO_TX61p	T5	
adi_D15	P2	IO.DIFFIO_RX62n	IO.DIFFIO_TX61n	T6	
T1		IO.CLK10p/DIFFIO_RX_C3p	IO.DIFFIO_TX62p	T10	fan_TACH
T2		IO.CLK10n/DIFFIO_RX_C3n	IO.DIFFIO_TX62n	T11	fan_EN_n
T3		CLK11p.INPUT		P3	VCC3_3
T4		CLK11n.INPUT		J5	
D3		FPLL10CLKp.INPUT		F5	
D4		FPLL10CLKn.INPUT			

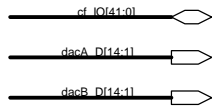
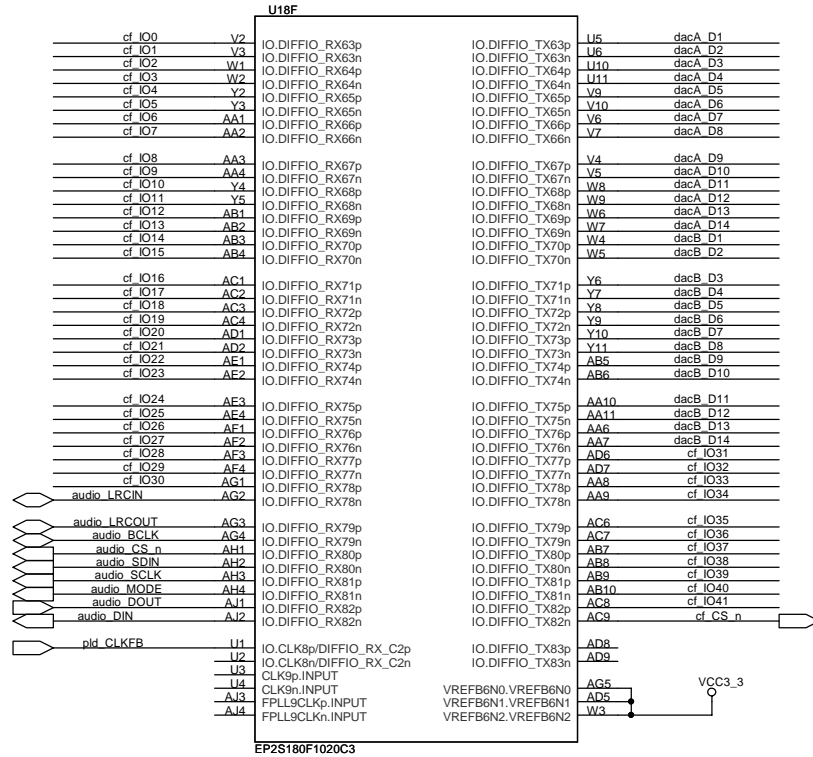
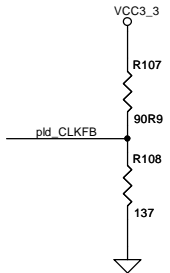
EP2S180F1020C3



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Title		
DSP Pro Stratix II 2S180 (Maine Pro)		
Size	Document Number	Rev
B	P06-10217-01	01
Date:	Thursday, August 18, 2005	Sheet 21 of 40



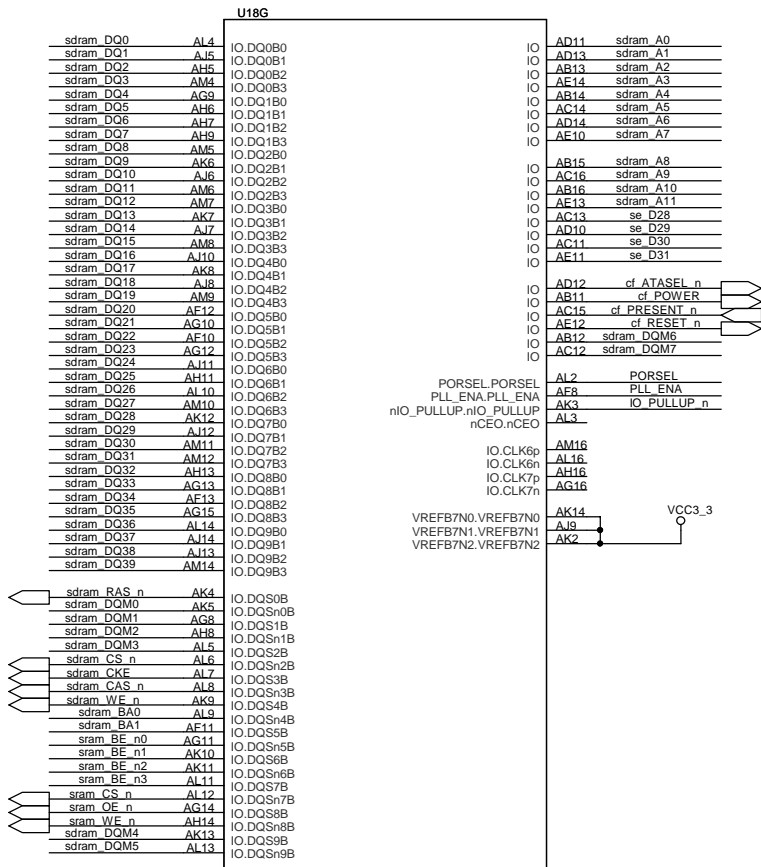
<Core Design>

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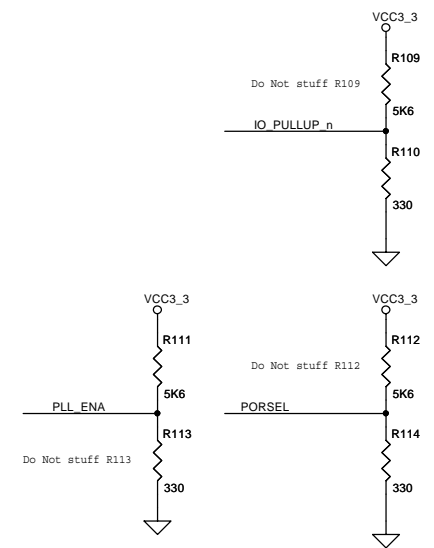
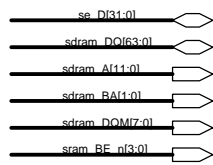
Title: DSP Pro Stratix II 2S180 (Maine Pro)

Size	Document Number	Rev
B	P06-10217-01	01

Date: Thursday, August 18, 2005 Sheet 22 of 40



EP2S180F1020C3



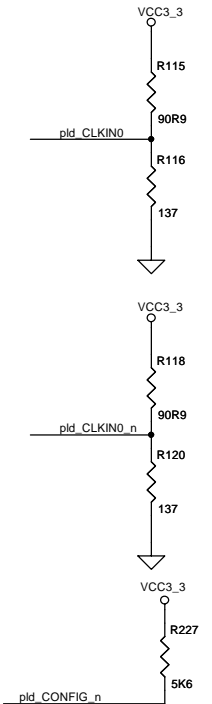
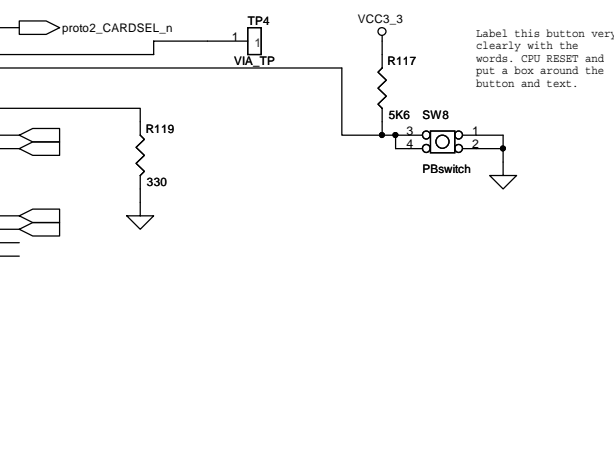
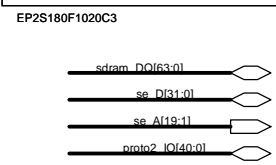
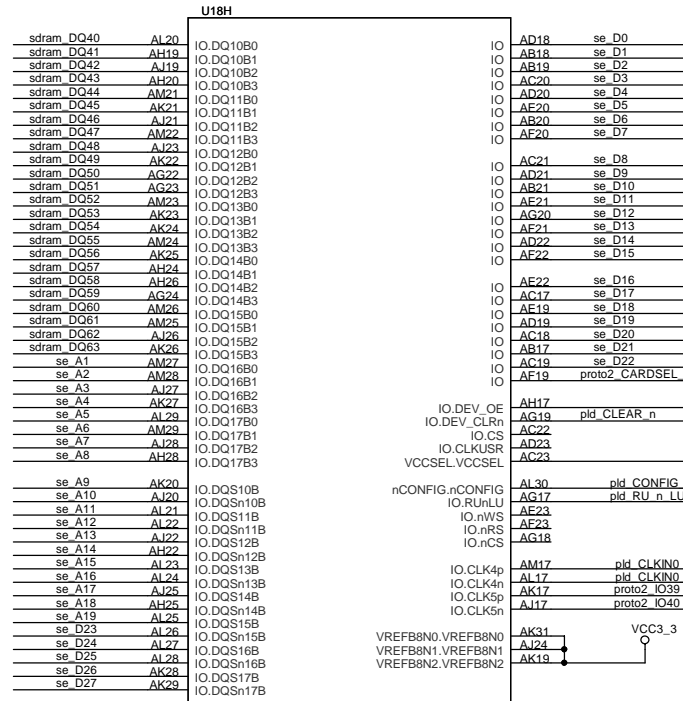
<Core Design>

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Size B	Document Number P06-10217-01	Rev 01
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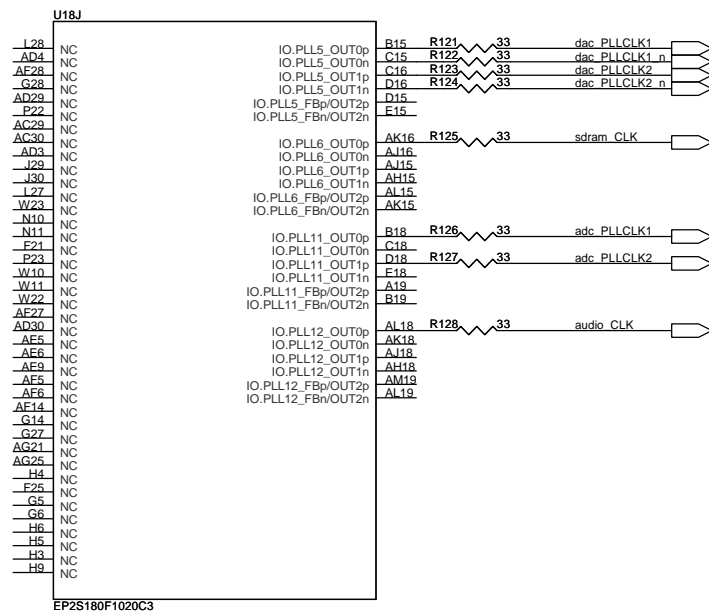
Date: Thursday, August 18, 2005 Sheet 23 of 40



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Title		DSP Pro Stratix II 2S180 (Maine Pro)
Size	Document Number	Rev
B	P06-10217-01	01
Date:	Thursday, August 18, 2005	Sheet 24 of 40



<Core Design>

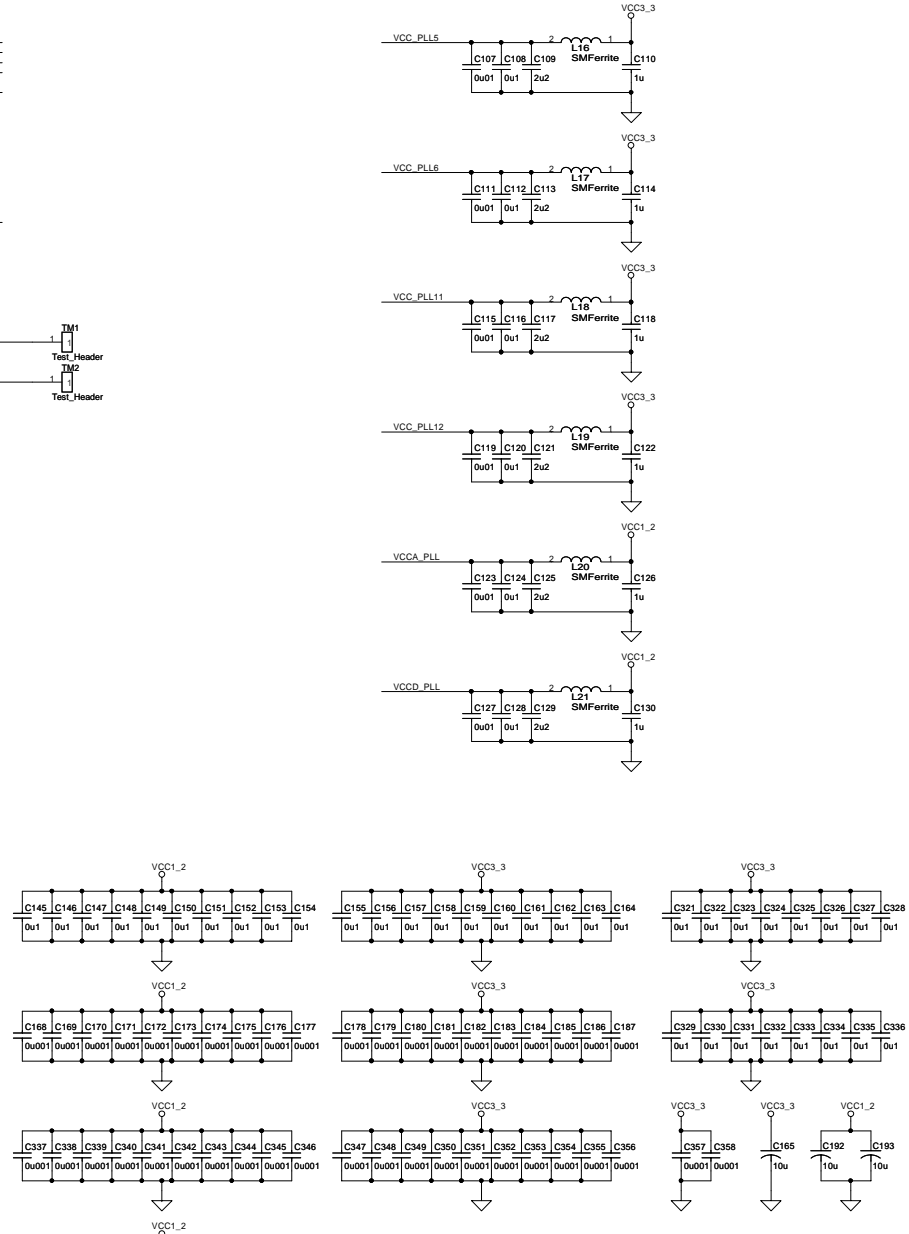
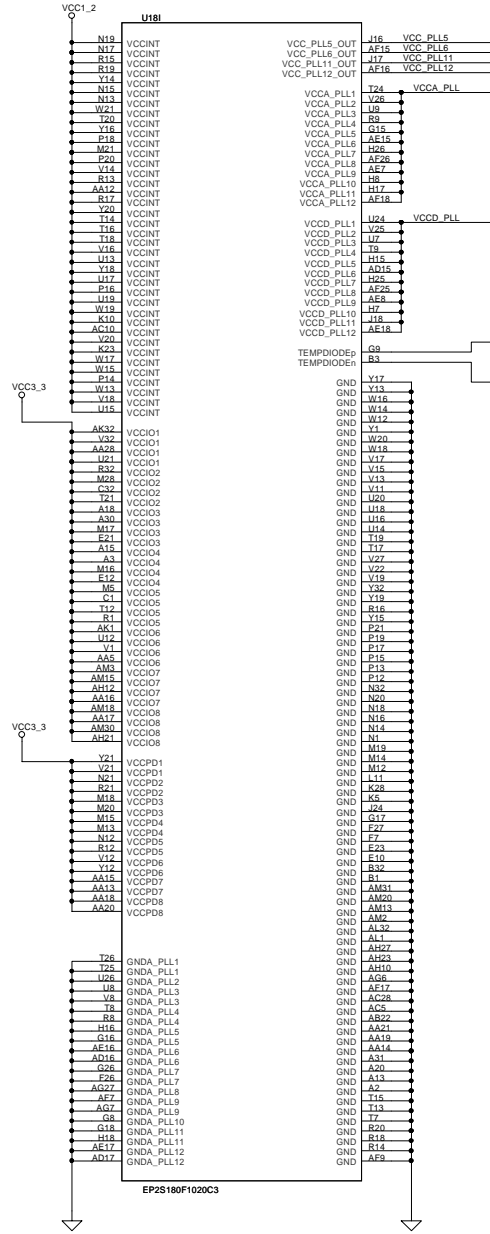
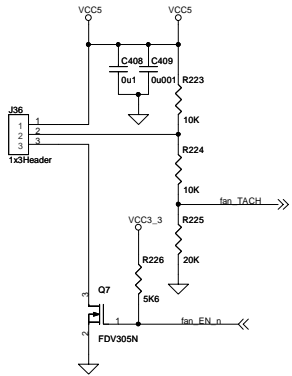
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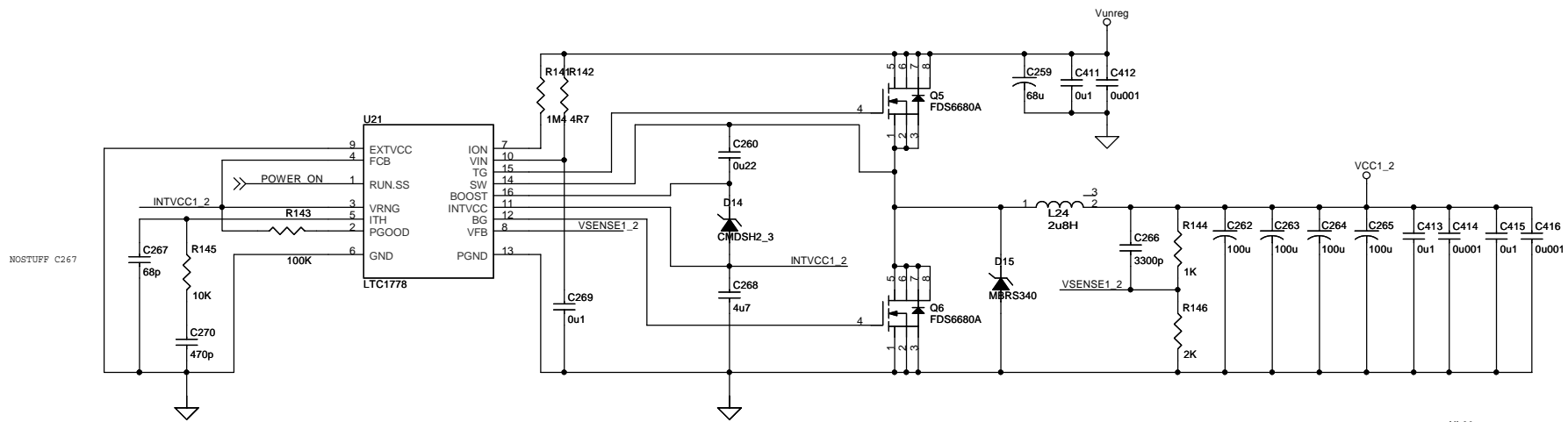
Size B	Document Number P06-10217-01	Rev 01
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Date: Thursday, August 18, 2005 Sheet 25 of 40

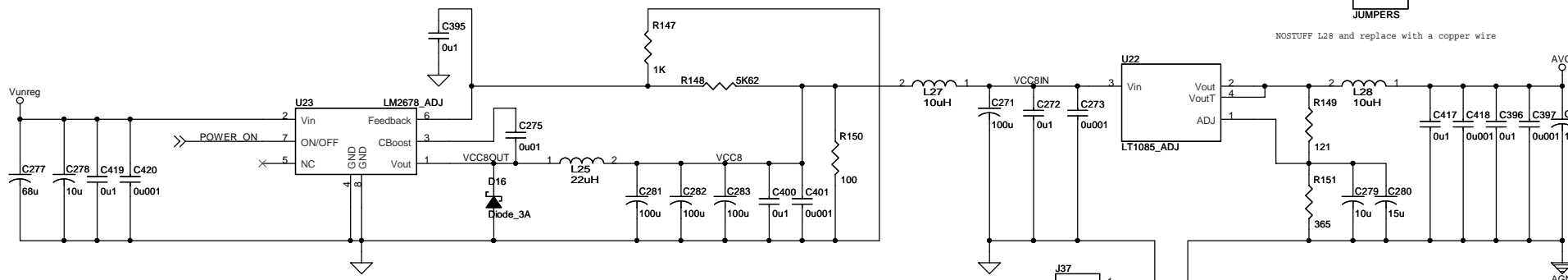


<Core Design>
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Title	DSP Pro Stratix II 2S180 (Maine Pro)	Rev	01
Size	Document Number P06-10217-01		
Date:	Thursday, August 18, 2005	Sheet	26 of 40



NOSTUFF L28 and replace with a copper wire



Note jumpers should always be installed to connect AGND to DGND unless and external GND source is being used.

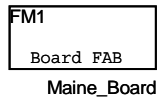
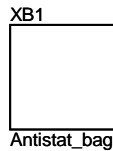
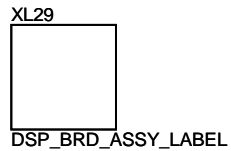
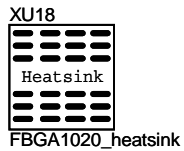
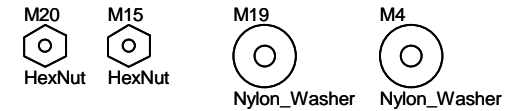
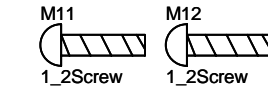
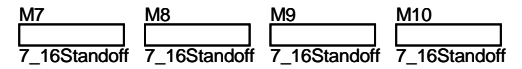
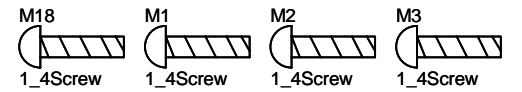
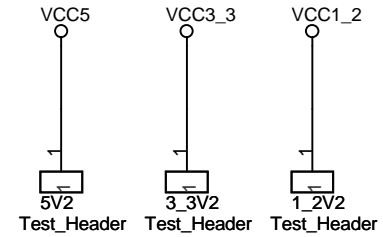
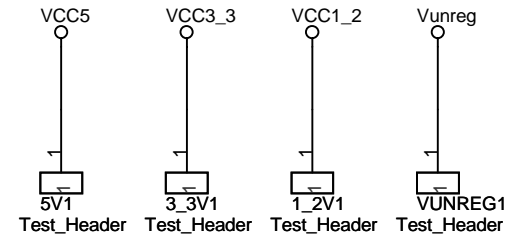
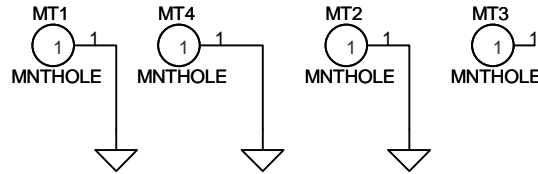
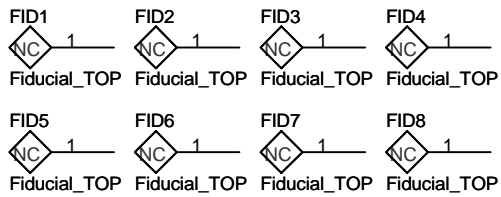
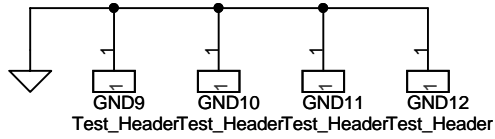
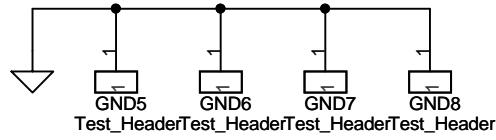
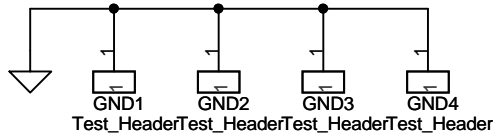


<Core Design>

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Title		
DSP Pro Stratix II 2S180 (Maine Pro)		
Size	Document Number	Rev
B	P06-10217-01	01
Date:	Thursday, August 18, 2005	Sheet 27 of 40

Reset and Test headers



<Core Design>

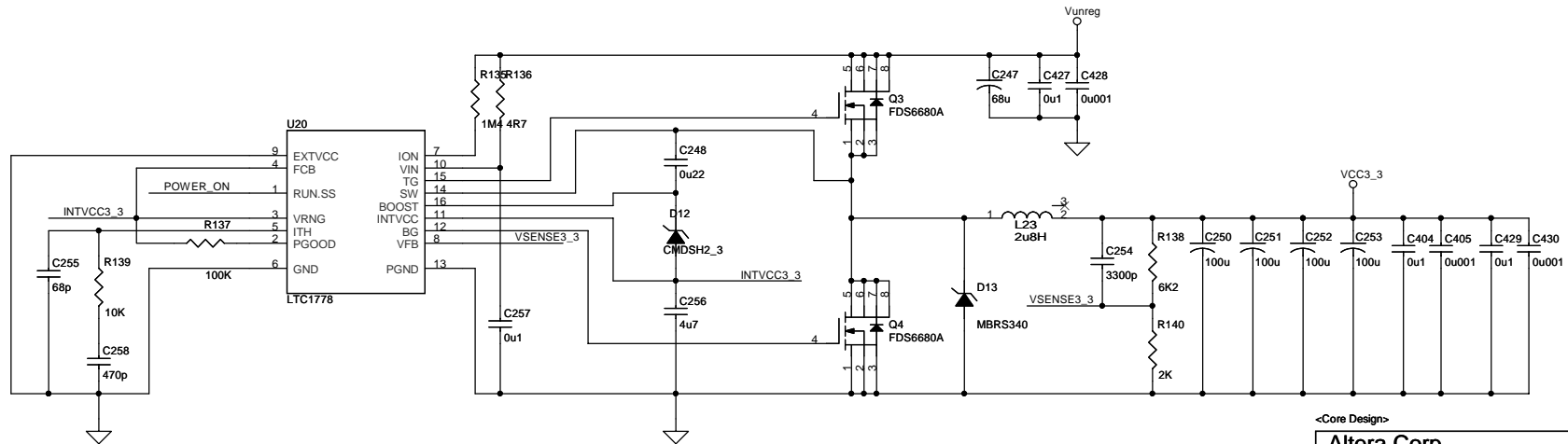
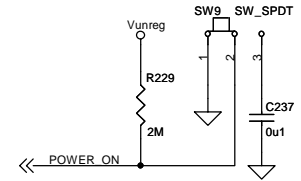
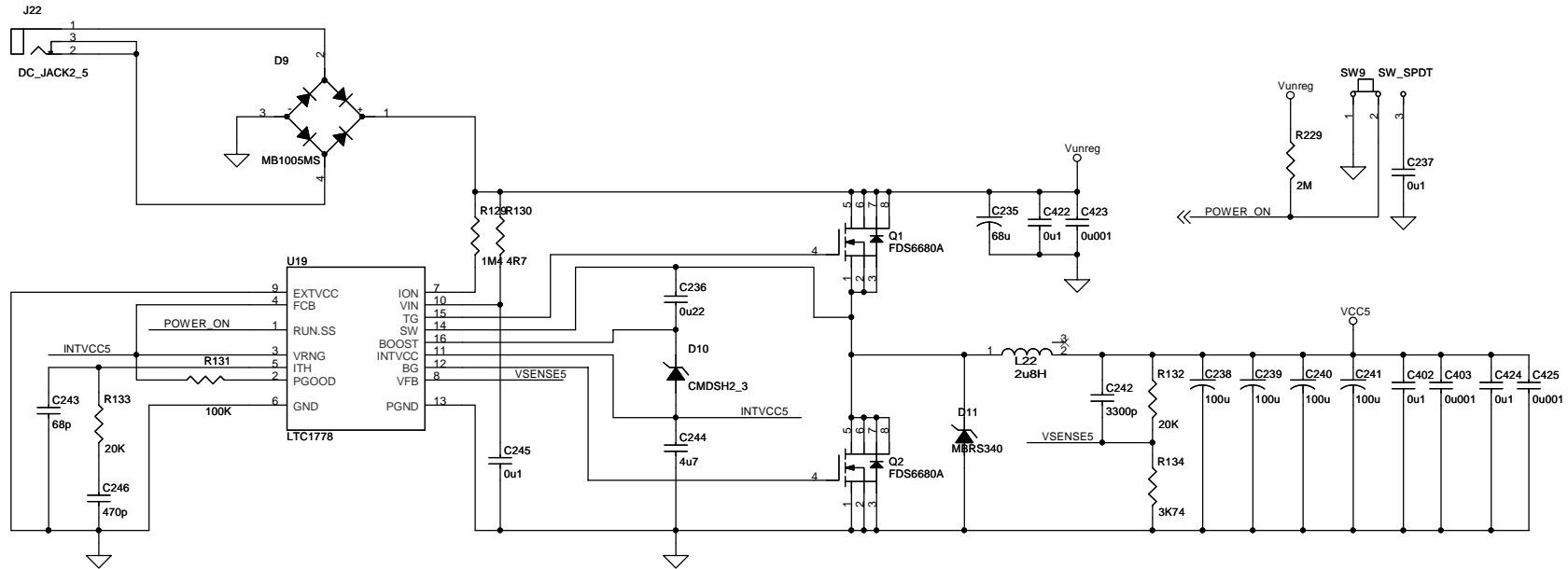
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Title
DSP Pro Stratix II 2S180 (Maine Pro)

Size A	Document Number P06-10217-01	Rev 01
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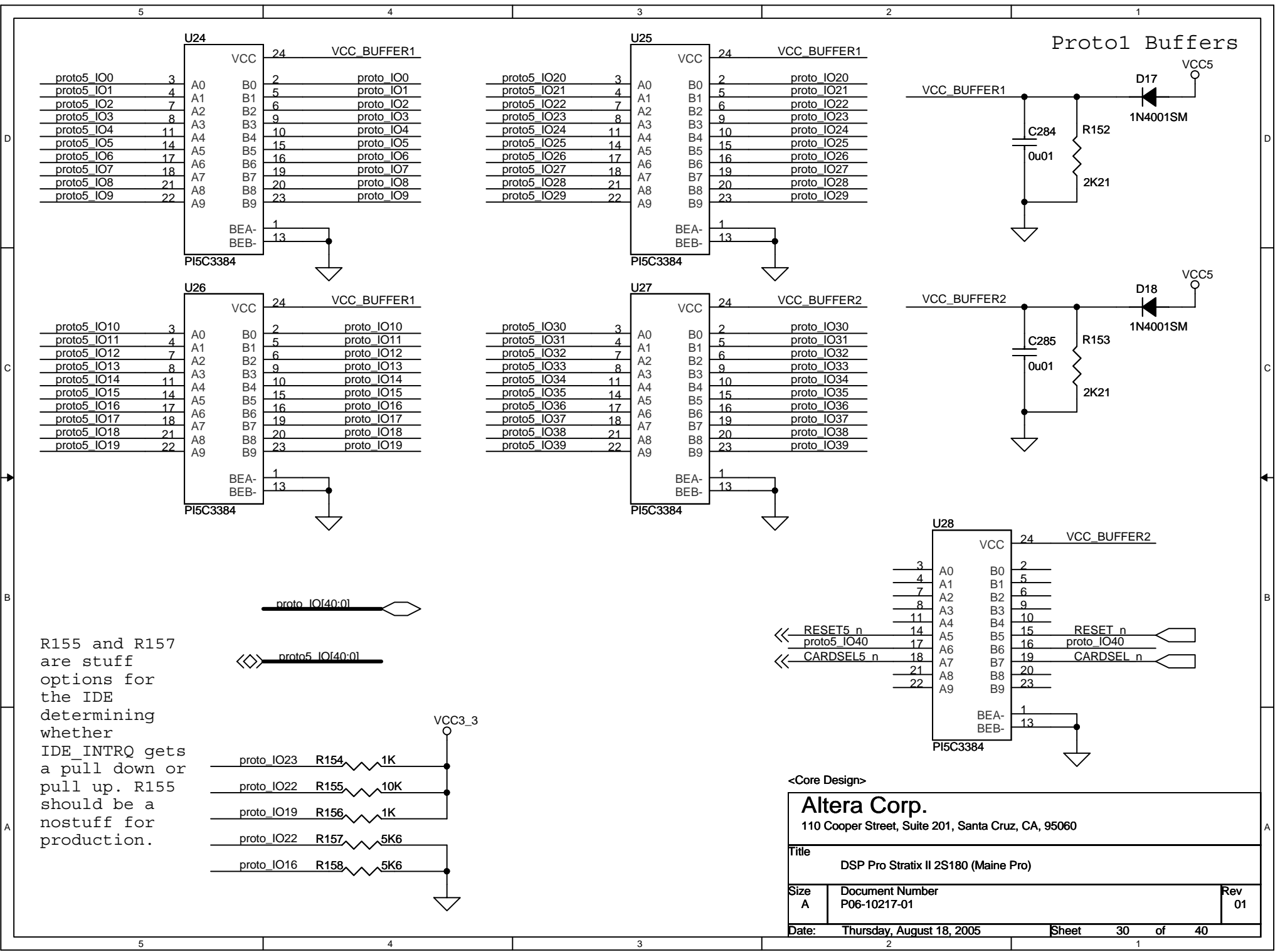
Date: Thursday, August 18, 2005 Sheet 28 of 40



<Core Design>

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Title		DSP Pro Stratix II 2S180 (Maine Pro)	
Size	Document Number	Rev	
B	P06-10217-01	01	
Date:	Thursday, August 18, 2005	Sheet	29 of 40



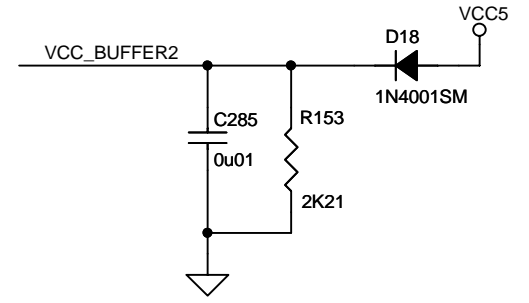
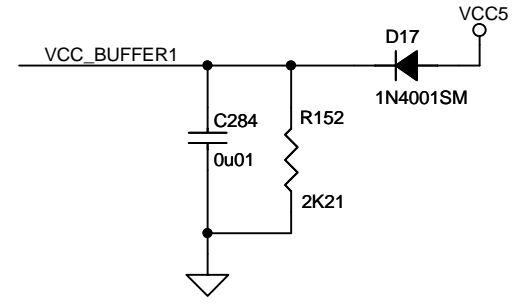
Protol Buffers

proto5_IO0	3	A0	B0	2	proto_IO0
proto5_IO1	4	A1	B1	5	proto_IO1
proto5_IO2	7	A2	B2	6	proto_IO2
proto5_IO3	8	A3	B3	9	proto_IO3
proto5_IO4	11	A4	B4	10	proto_IO4
proto5_IO5	14	A5	B5	15	proto_IO5
proto5_IO6	17	A6	B6	16	proto_IO6
proto5_IO7	18	A7	B7	19	proto_IO7
proto5_IO8	21	A8	B8	20	proto_IO8
proto5_IO9	22	A9	B9	23	proto_IO9

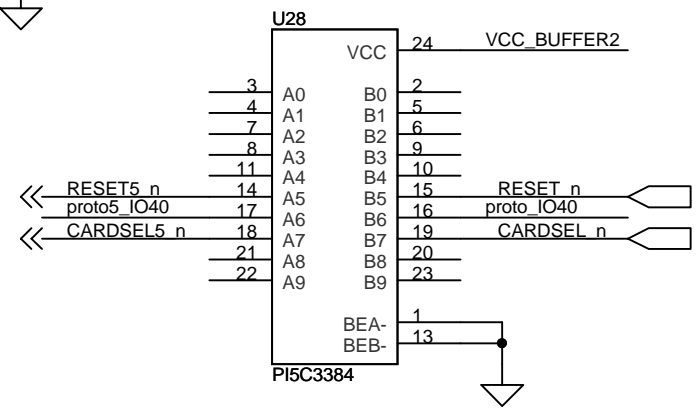
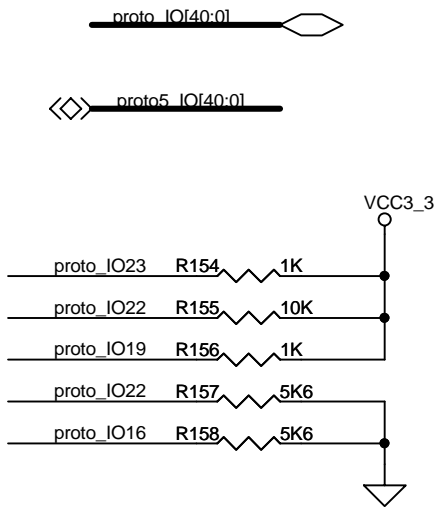
proto5_IO20	3	A0	B0	2	proto_IO20
proto5_IO21	4	A1	B1	5	proto_IO21
proto5_IO22	7	A2	B2	6	proto_IO22
proto5_IO23	8	A3	B3	9	proto_IO23
proto5_IO24	11	A4	B4	10	proto_IO24
proto5_IO25	14	A5	B5	15	proto_IO25
proto5_IO26	17	A6	B6	16	proto_IO26
proto5_IO27	18	A7	B7	19	proto_IO27
proto5_IO28	21	A8	B8	20	proto_IO28
proto5_IO29	22	A9	B9	23	proto_IO29

proto5_IO10	3	A0	B0	2	proto_IO10
proto5_IO11	4	A1	B1	5	proto_IO11
proto5_IO12	7	A2	B2	6	proto_IO12
proto5_IO13	8	A3	B3	9	proto_IO13
proto5_IO14	11	A4	B4	10	proto_IO14
proto5_IO15	14	A5	B5	15	proto_IO15
proto5_IO16	17	A6	B6	16	proto_IO16
proto5_IO17	18	A7	B7	19	proto_IO17
proto5_IO18	21	A8	B8	20	proto_IO18
proto5_IO19	22	A9	B9	23	proto_IO19

proto5_IO30	3	A0	B0	2	proto_IO30
proto5_IO31	4	A1	B1	5	proto_IO31
proto5_IO32	7	A2	B2	6	proto_IO32
proto5_IO33	8	A3	B3	9	proto_IO33
proto5_IO34	11	A4	B4	10	proto_IO34
proto5_IO35	14	A5	B5	15	proto_IO35
proto5_IO36	17	A6	B6	16	proto_IO36
proto5_IO37	18	A7	B7	19	proto_IO37
proto5_IO38	21	A8	B8	20	proto_IO38
proto5_IO39	22	A9	B9	23	proto_IO39



R155 and R157 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R155 should be a nostuff for production.



<Core Design>

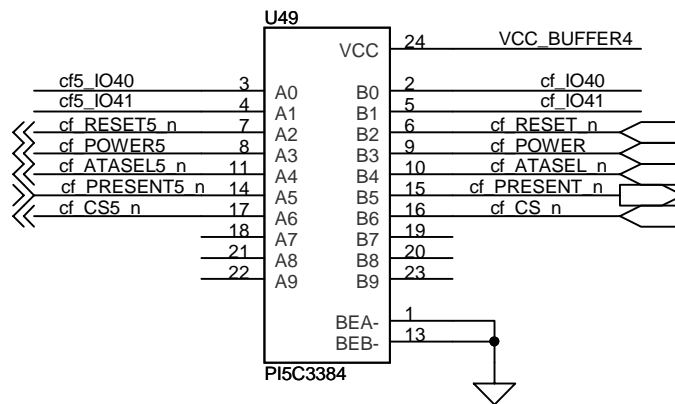
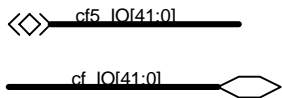
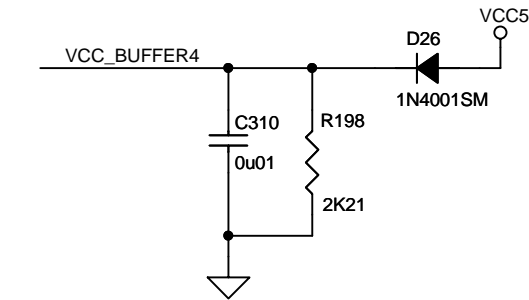
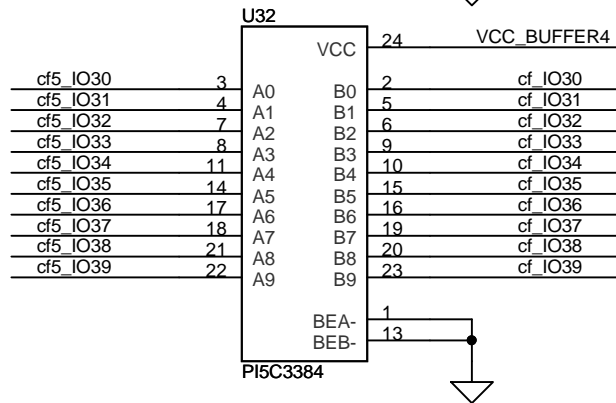
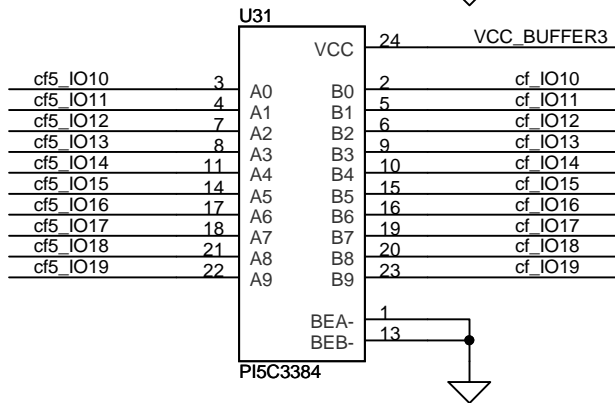
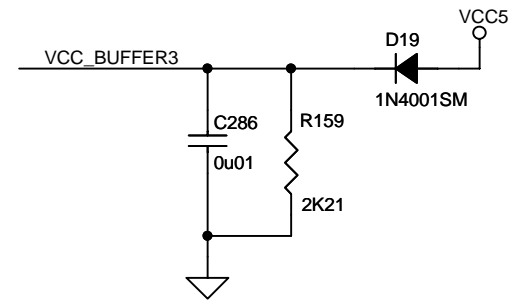
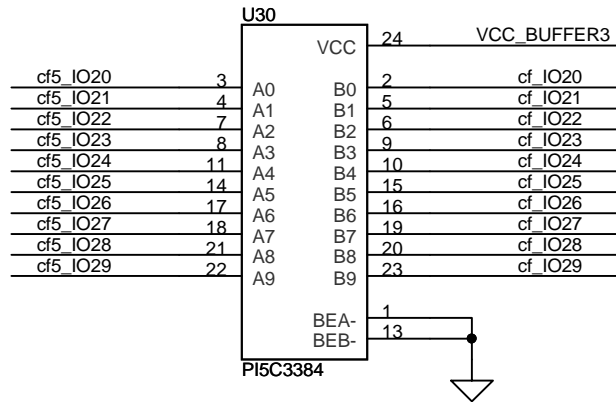
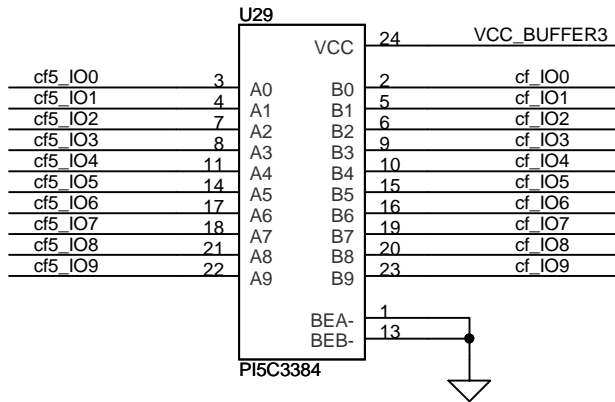
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Title: DSP Pro Stratix II 2S180 (Maine Pro)

Size A	Document Number P06-10217-01	Rev 01
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Date: Thursday, August 18, 2005 Sheet 30 of 40

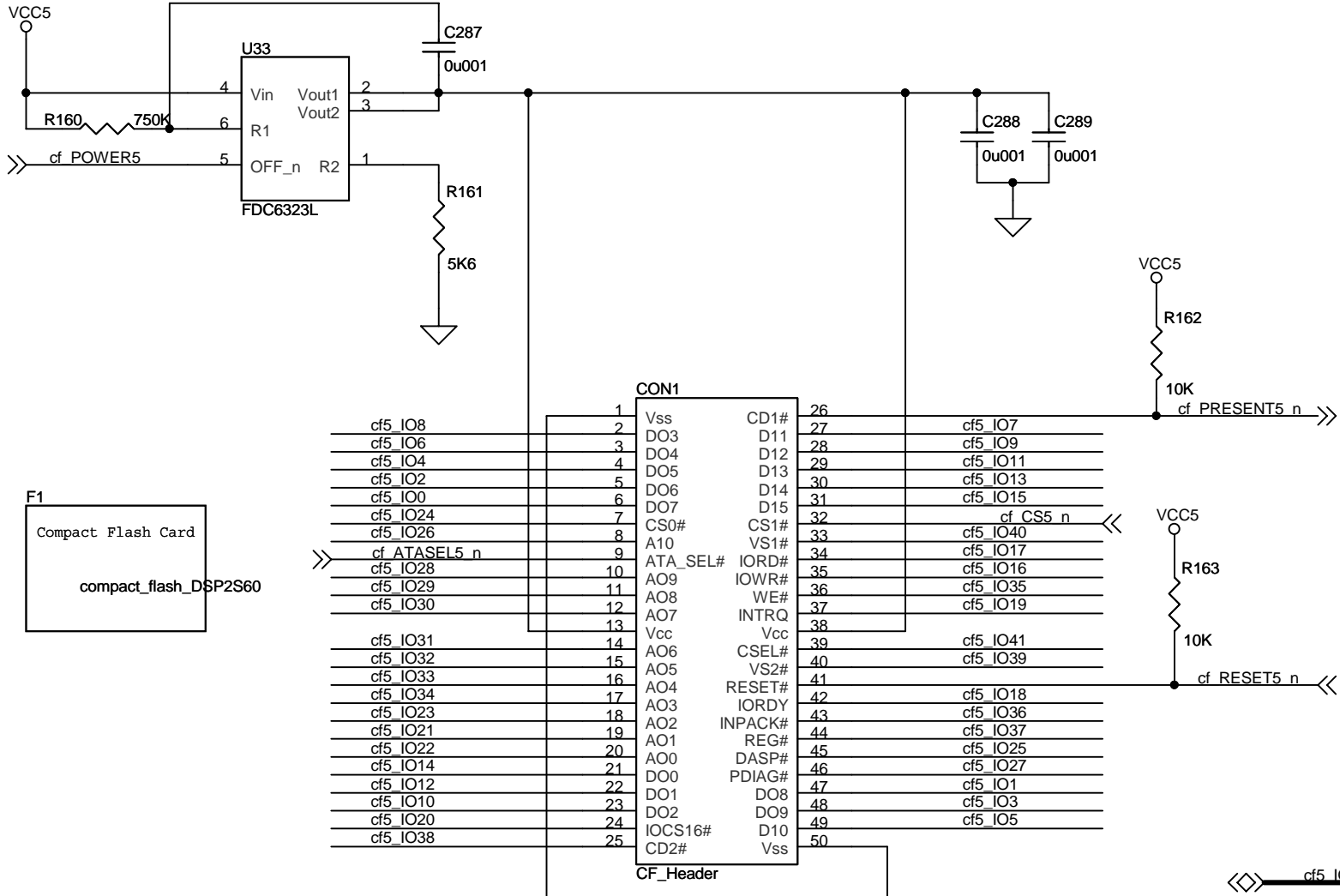
Protol Buffers



<Core Design>

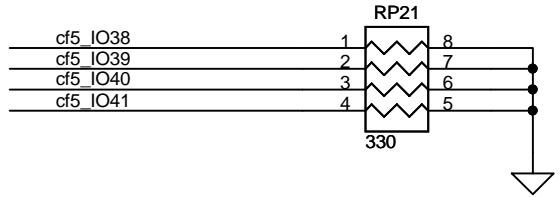
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110 Cooper Street, Suite 201, Santa Cruz, CA, 95060		
Title DSP Pro Stratix II 2S180 (Maine Pro)		
Size A	Document Number P06-10217-01	Rev 01
Date:	Thursday, August 18, 2005	Sheet 31 of 40

Compact Flash Socket



CF_Header	
1	Vss
2	DO3
3	DO4
4	DO5
5	DO6
6	DO7
7	CS0#
8	A10
9	ATA_SEL#
10	AO9
11	AO8
12	AO7
13	Vcc
14	AO6
15	AO5
16	AO4
17	AO3
18	AO2
19	AO1
20	AO0
21	DO0
22	DO1
23	DO2
24	IOCS16#
25	CD2#
26	CD1#
27	D03
28	D12
29	D13
30	D14
31	D15
32	CS1#
33	VS1#
34	IORD#
35	IOWR#
36	WE#
37	INTRQ
38	Vcc
39	CSEL#
40	VS2#
41	RESET#
42	IORDY
43	INPACK#
44	REG#
45	DASP#
46	PDIAG#
47	DO8
48	DO9
49	D10
50	Vss

F1
Compact Flash Card
compact_flash_DSP2S60



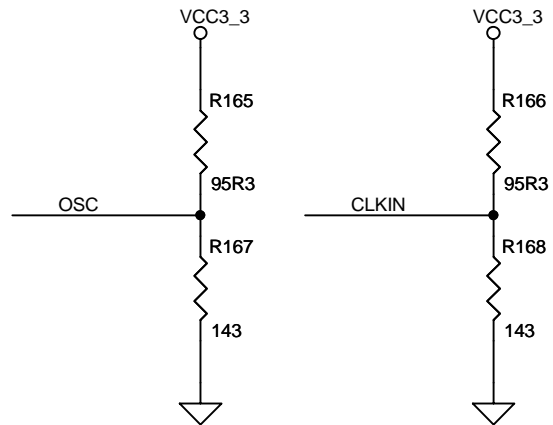
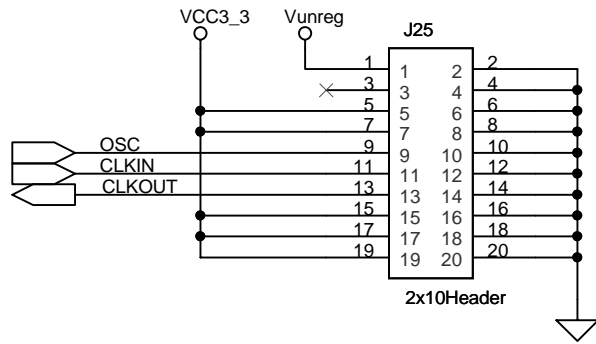
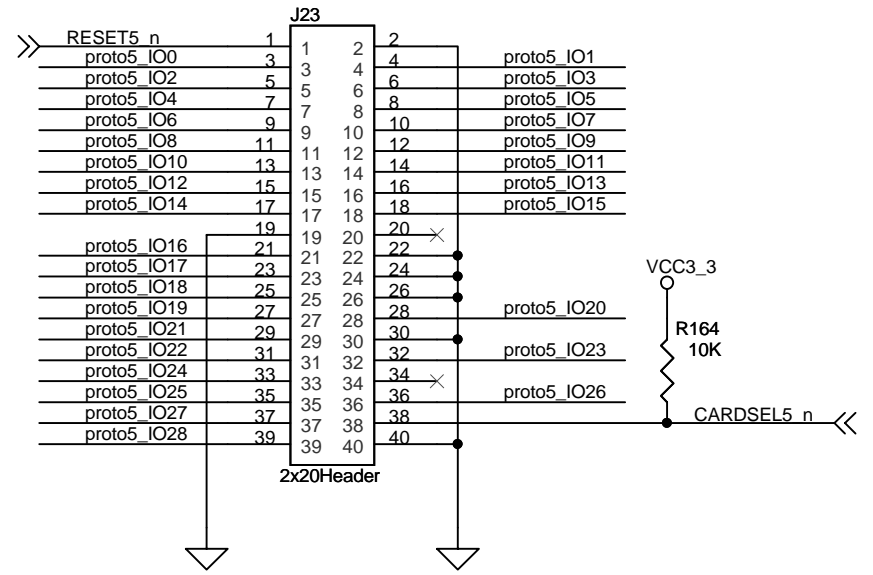
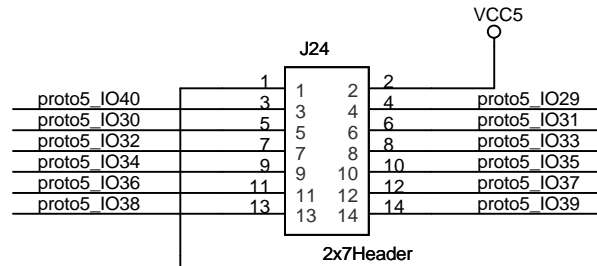
<Core Design>

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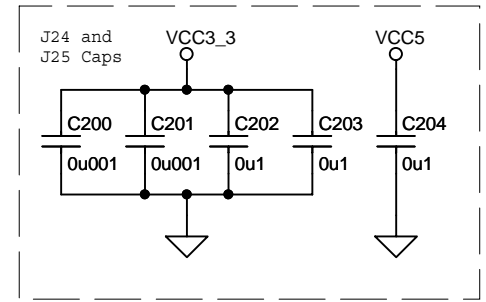
Title: DSP Pro Stratix II 2S180 (Maine Pro)

Size: A	Document Number: P06-10217-01	Rev: 01
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Date: Thursday, August 18, 2005 Sheet 32 of 40

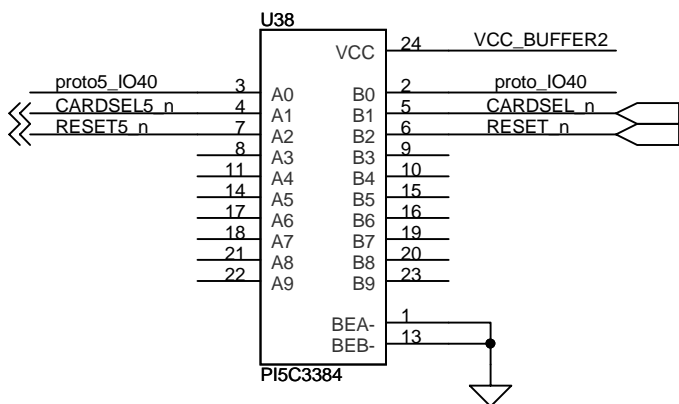
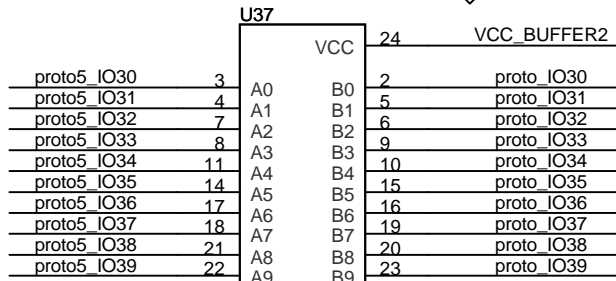
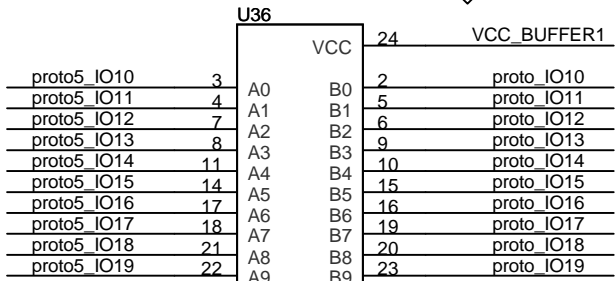
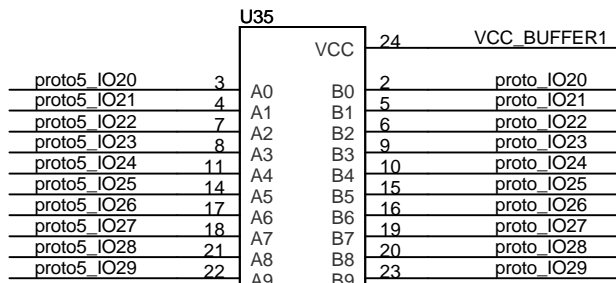
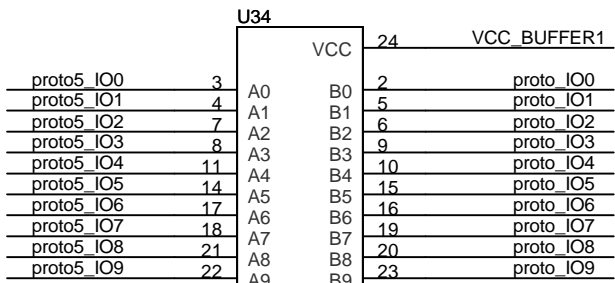


proto5 IO[40:0]

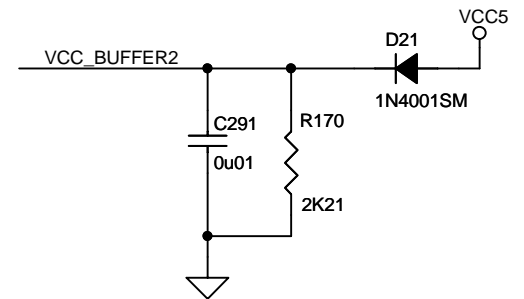
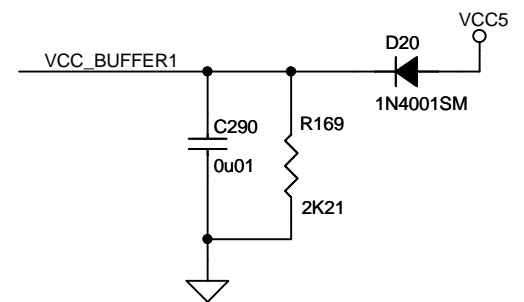


<Core Design>

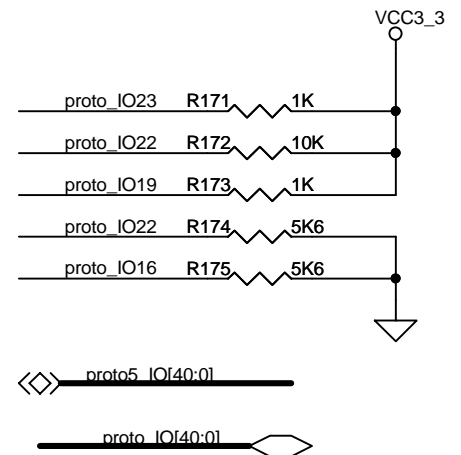
<p>Altera Corp. 110 Cooper Street, Suite 201, Santa Cruz, CA, 95060</p>		
<p>Title DSP Pro Stratix II 2S180 (Maine Pro)</p>		
Size A	Document Number P06-10217-01	Rev 01
Date:	Thursday, August 18, 2005	Sheet 33 of 40



Proto2 Buffers



R172 and R174 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R172 should be a nostuff for production.



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Title

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Size

Document Number
P06-10217-01

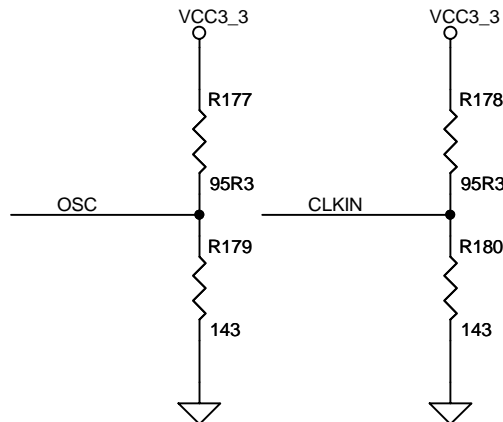
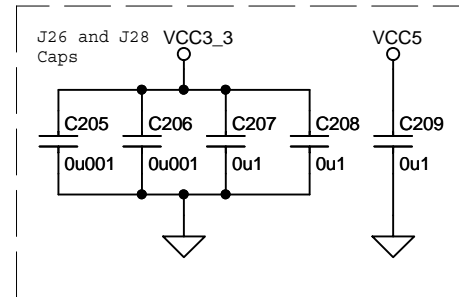
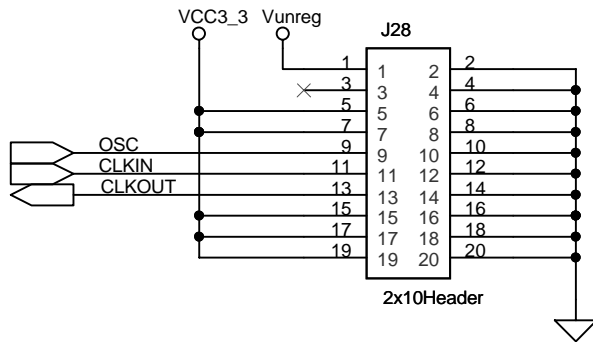
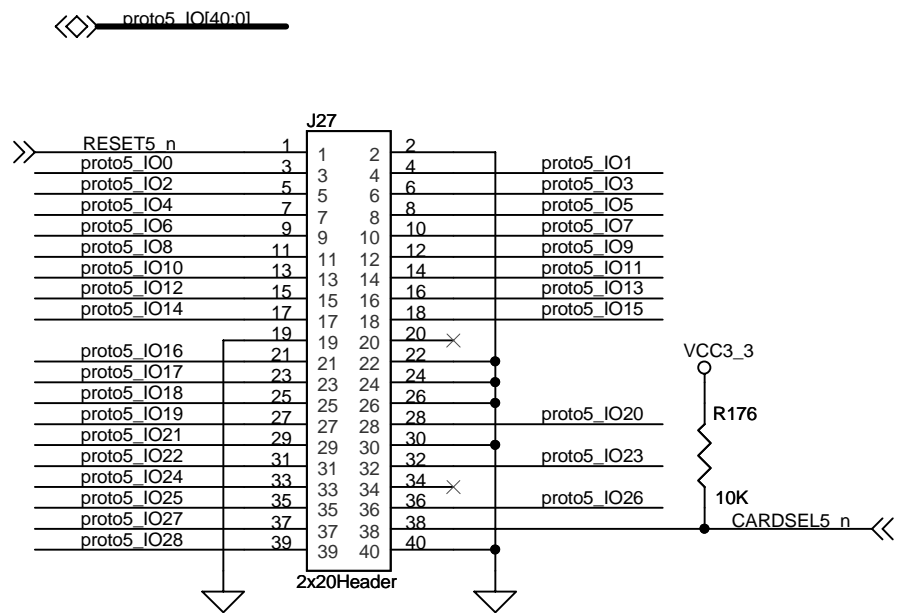
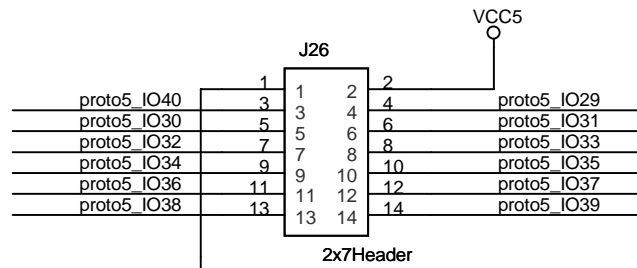
Rev

01

Date: Thursday, August 18, 2005

Sheet 34 of 40

Proto2 Headers



<Core Design>

Altera Corp.		
110 Cooper Street, Suite 201, Santa Cruz, CA, 95060		
Title DSP Pro Stratix II 2S180 (Maine Pro)		
Size A	Document Number P06-10217-01	Rev 01
Date:	Thursday, August 18, 2005	Sheet 35 of 40

U39

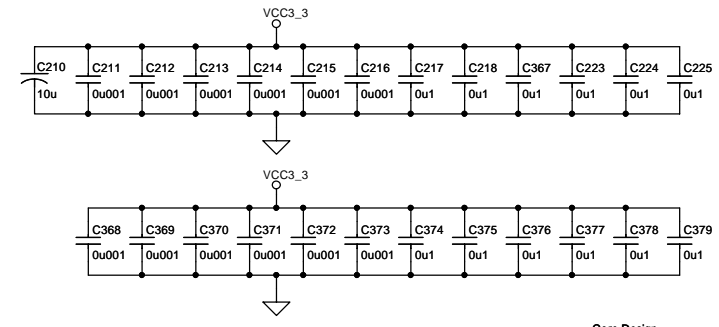
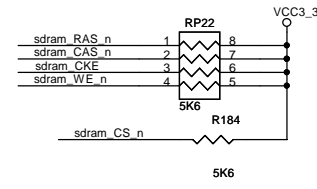
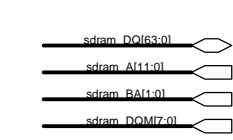
sdram A0	25	A0	DQ0	2	sdram DQ0
sdram A1	26	A1	DQ1	4	sdram DQ1
sdram A2	27	A2	DQ2	5	sdram DQ2
sdram A3	60	A3	DQ3	7	sdram DQ3
sdram A4	61	A3	DQ3	8	sdram DQ4
sdram A5	62	A4	DQ4	10	sdram DQ5
sdram A6	63	A5	DQ5	11	sdram DQ6
sdram A7	64	A6	DQ6	13	sdram DQ7
sdram A8	65	A7	DQ7	14	sdram DQ8
sdram A9	66	A8	DQ8	74	sdram DQ8
sdram A10	24	A9	DQ9	76	sdram DQ9
sdram A11	21	A10	DQ10	77	sdram DQ10
		A11	DQ11	79	sdram DQ11
sdram BA0	22	BA0	DQ12	80	sdram DQ12
sdram BA1	23	BA1	DQ13	82	sdram DQ13
			DQ14	83	sdram DQ14
sdram DQM0	16	DQM0	DQ15	85	sdram DQ15
sdram DQM1	71	DQM1	DQ16	31	sdram DQ16
sdram DQM2	28	DQM2	DQ17	33	sdram DQ17
sdram DQM3	59	DQM3	DQ18	34	sdram DQ18
			DQ19	36	sdram DQ19
			DQ20	37	sdram DQ20
sdram WE_n	17	WE_n	DQ21	39	sdram DQ21
sdram CAS_n	18	CAS_n	DQ22	40	sdram DQ22
sdram RAS_n	19	RAS_n	DQ23	42	sdram DQ23
sdram CS_n	20	CS_n	DQ24	45	sdram DQ24
			DQ25	47	sdram DQ25
sdram CLK	68	CLK	DQ26	48	sdram DQ26
sdram CKE	67	CKE	DQ27	50	sdram DQ27
			DQ28	51	sdram DQ28
			DQ29	53	sdram DQ29
			DQ30	54	sdram DQ30
			DQ31	56	sdram DQ31

MT48LC4M32B2

U40

sdram A0	25	A0	DQ0	2	sdram DQ32
sdram A1	26	A1	DQ1	4	sdram DQ33
sdram A2	27	A2	DQ2	5	sdram DQ34
sdram A3	60	A3	DQ3	7	sdram DQ35
sdram A4	61	A3	DQ3	8	sdram DQ36
sdram A5	62	A4	DQ4	10	sdram DQ37
sdram A6	63	A5	DQ5	11	sdram DQ38
sdram A7	64	A6	DQ6	13	sdram DQ39
sdram A8	65	A7	DQ7	14	sdram DQ40
sdram A9	66	A8	DQ8	74	sdram DQ40
sdram A10	24	A9	DQ9	76	sdram DQ41
sdram A11	21	A10	DQ10	77	sdram DQ42
		A11	DQ11	79	sdram DQ43
sdram BA0	22	BA0	DQ12	80	sdram DQ44
sdram BA1	23	BA1	DQ13	82	sdram DQ45
			DQ14	83	sdram DQ46
sdram DQM4	16	DQM0	DQ15	85	sdram DQ47
sdram DQM5	71	DQM1	DQ16	31	sdram DQ48
sdram DQM6	28	DQM2	DQ17	33	sdram DQ49
sdram DQM7	59	DQM3	DQ18	34	sdram DQ50
			DQ19	36	sdram DQ51
			DQ20	37	sdram DQ52
sdram WE_n	17	WE_n	DQ21	39	sdram DQ53
sdram CAS_n	18	CAS_n	DQ22	40	sdram DQ54
sdram RAS_n	19	RAS_n	DQ23	42	sdram DQ55
sdram CS_n	20	CS_n	DQ24	45	sdram DQ56
			DQ25	47	sdram DQ57
sdram CLK	68	CLK	DQ26	48	sdram DQ58
sdram CKE	67	CKE	DQ27	50	sdram DQ59
			DQ28	51	sdram DQ60
			DQ29	53	sdram DQ61
			DQ30	54	sdram DQ62
			DQ31	56	sdram DQ63

MT48LC4M32B2



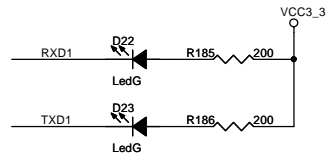
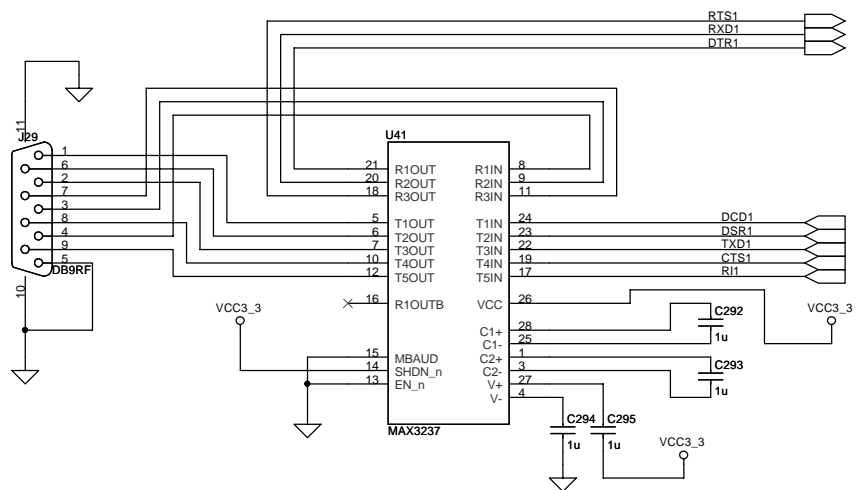
<Core Design>

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Size	Document Number	Rev
B	P06-10217-01	01

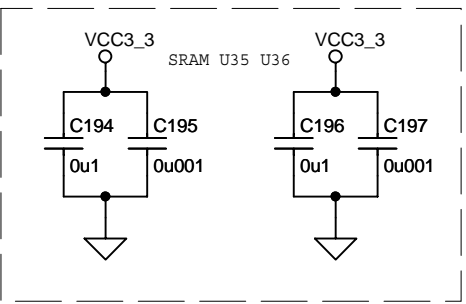
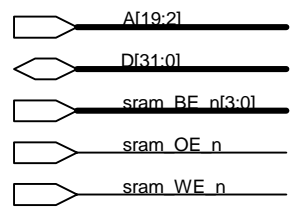
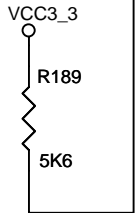
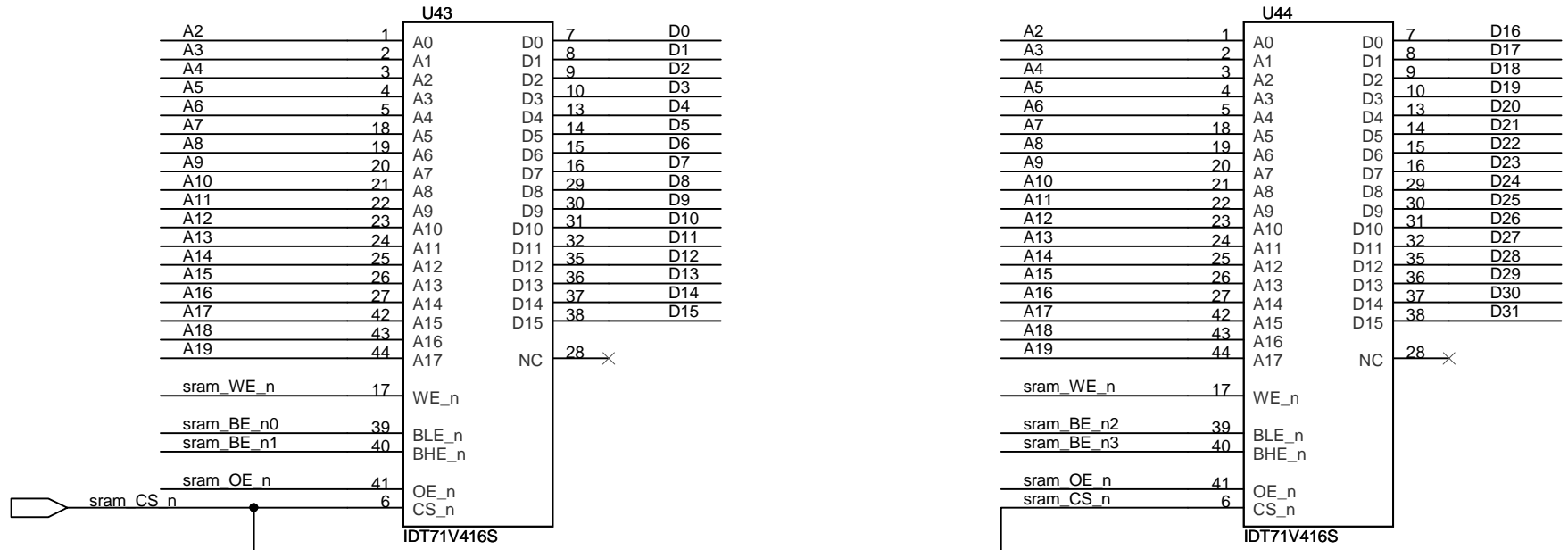
Date: Thursday, August 18, 2005 Sheet 36 of 40

Serial Ports



<Core Design>

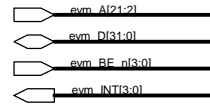
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Date:	Thursday, August 18, 2005	Sheet 37 of 40



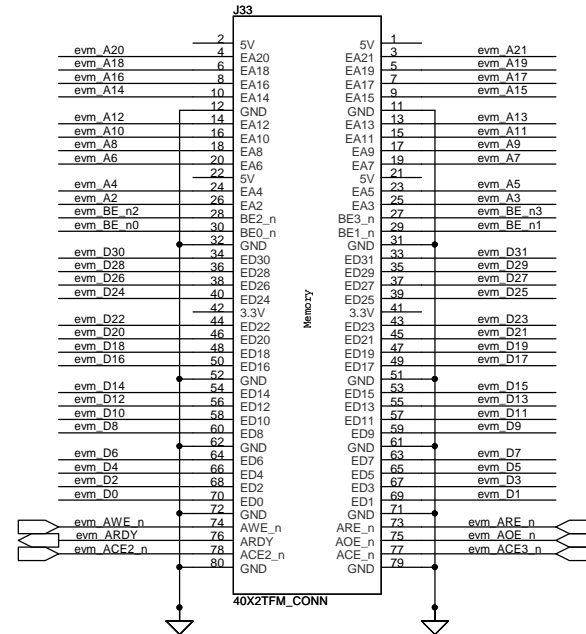
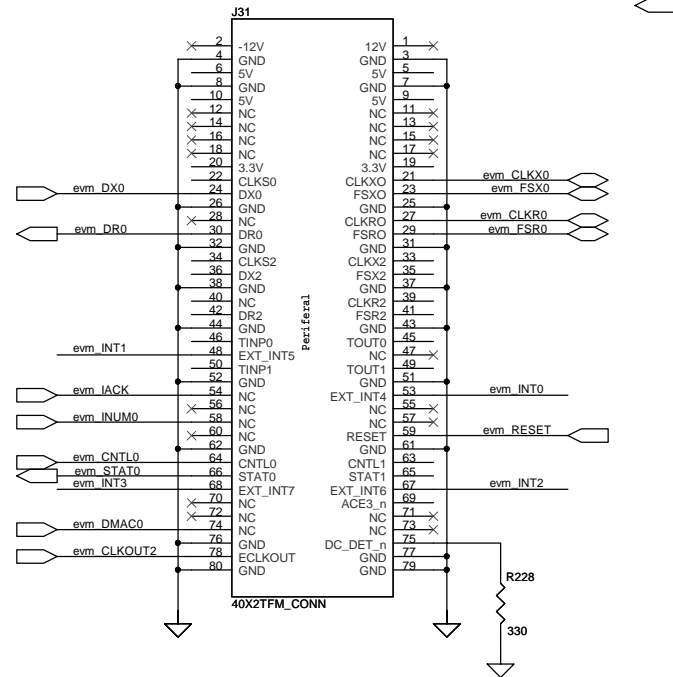
One bank of 256K x 32 SRAM (two 256K x 16 parts in parallel) = 1Mbyte of SRAM

<Core Design>

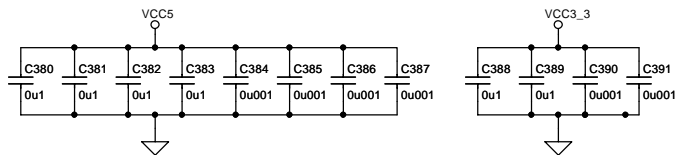
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Size A	Document Number P06-10217-01	Rev 01
Date:	Thursday, August 18, 2005	Sheet 38 of 40



3.00"
apart



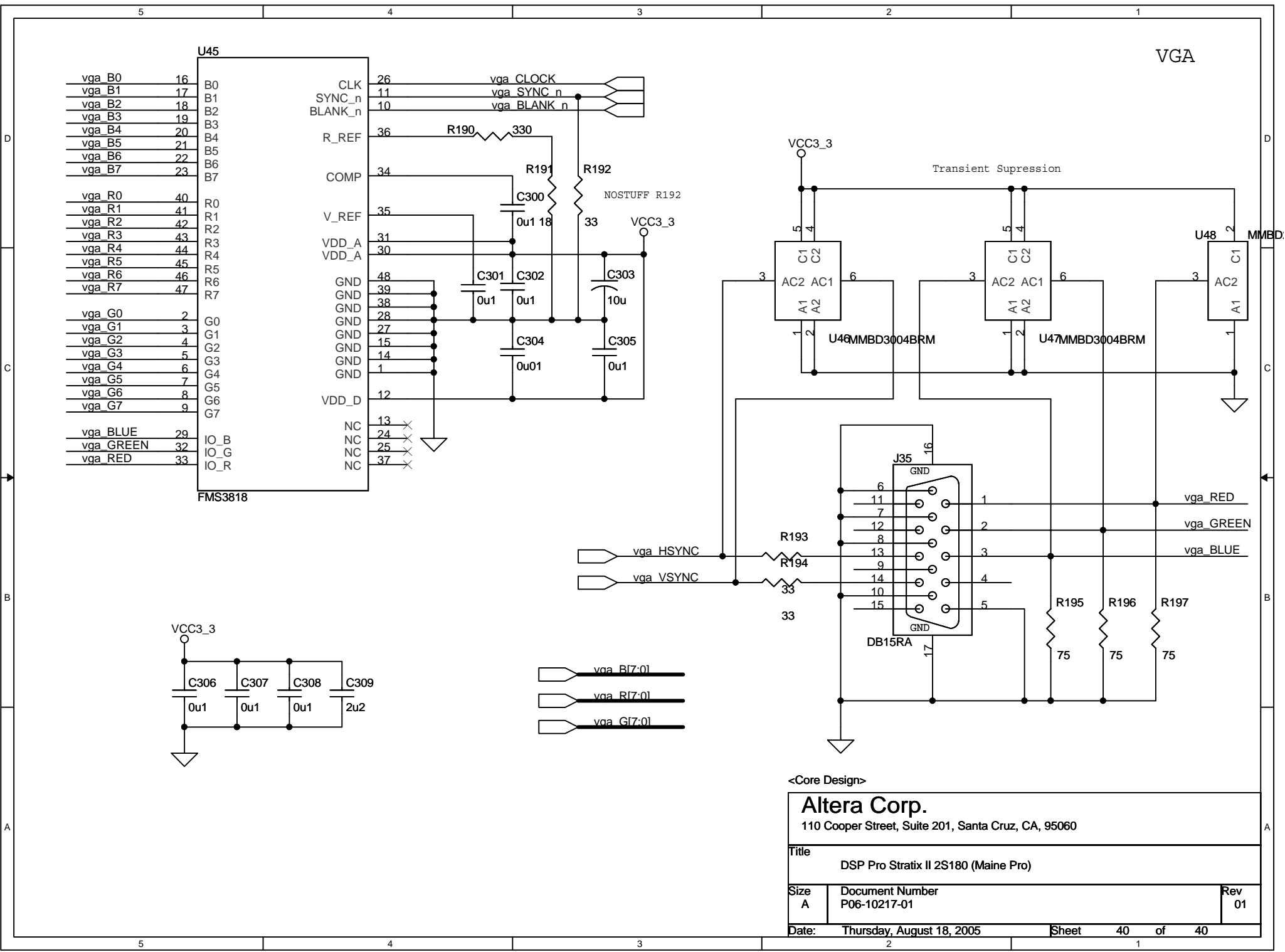
These connectors reference the TI 6416 board



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Size	Document Number	Rev
B	P06-10217-01	01
Date:	Thursday, August 18, 2005	Sheet 39 of 40



VGA

vga_B0	16	B0
vga_B1	17	B1
vga_B2	18	B2
vga_B3	19	B3
vga_B4	20	B4
vga_B5	21	B5
vga_B6	22	B6
vga_B7	23	B7
vga_R0	40	R0
vga_R1	41	R1
vga_R2	42	R2
vga_R3	43	R3
vga_R4	44	R4
vga_R5	45	R5
vga_R6	46	R6
vga_R7	47	R7
vga_G0	2	G0
vga_G1	3	G1
vga_G2	4	G2
vga_G3	5	G3
vga_G4	6	G4
vga_G5	7	G5
vga_G6	8	G6
vga_G7	9	G7
vga_BLUE	29	IO_B
vga_GREEN	32	IO_G
vga_RED	33	IO_R

U45
FMS3818

Transient Supression

U46 MMBD3004BRM

U47 MMBD3004BRM

U48 MMBD3004BRM

J35 DB15RA

R193, R194, R195, R196, R197

vga_RED, vga_GREEN, vga_BLUE

vga_BI7-01, vga_RI7-01, vga_GI7-01

VCC3_3

C306, C307, C308, C309

0u1, 0u1, 0u1, 2u2

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Size	Document Number	Rev
A	P06-10217-01	01
Date:	Thursday, August 18, 2005	Sheet 40 of 40