DSP Pro Development Board
Stratix II 2S180 Edition
Rev 01

Revision History

Date	Change Description	Rev
8/18/05	Created schematic and changed the component from the 2S60 on the DSP board to the 2S180 on this Pro version of the board	01

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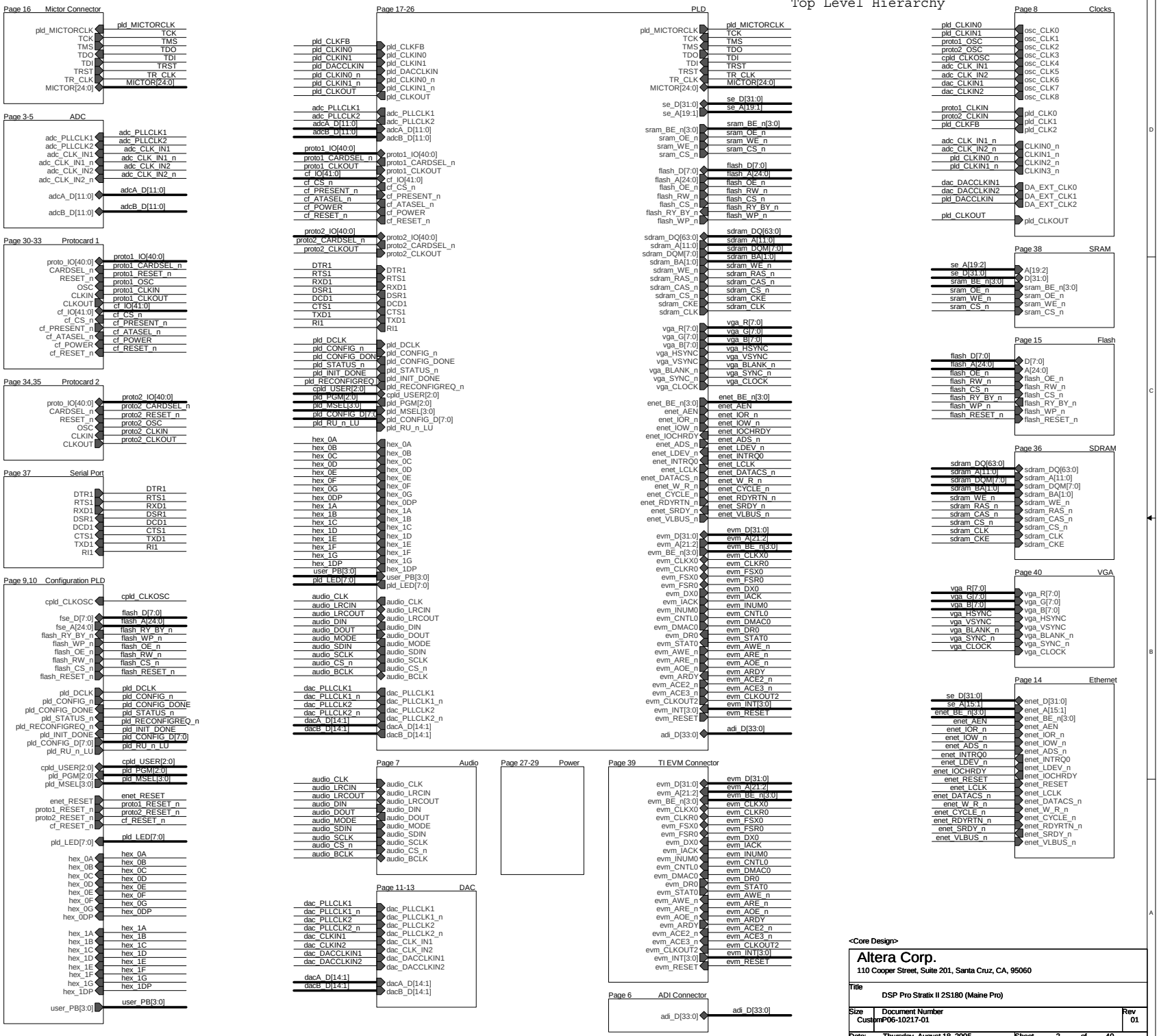
Top Level Hierarchy



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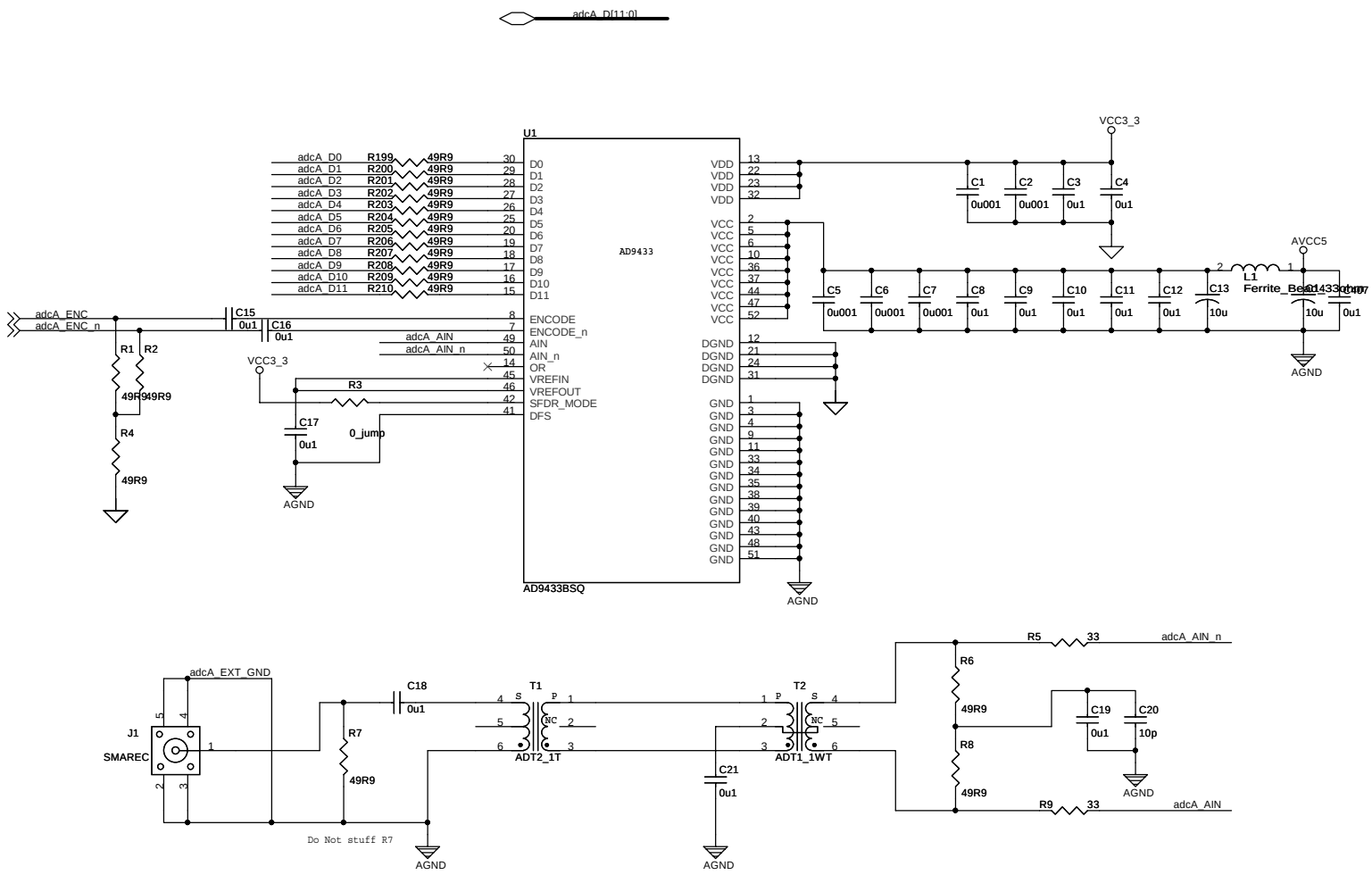
ADC A



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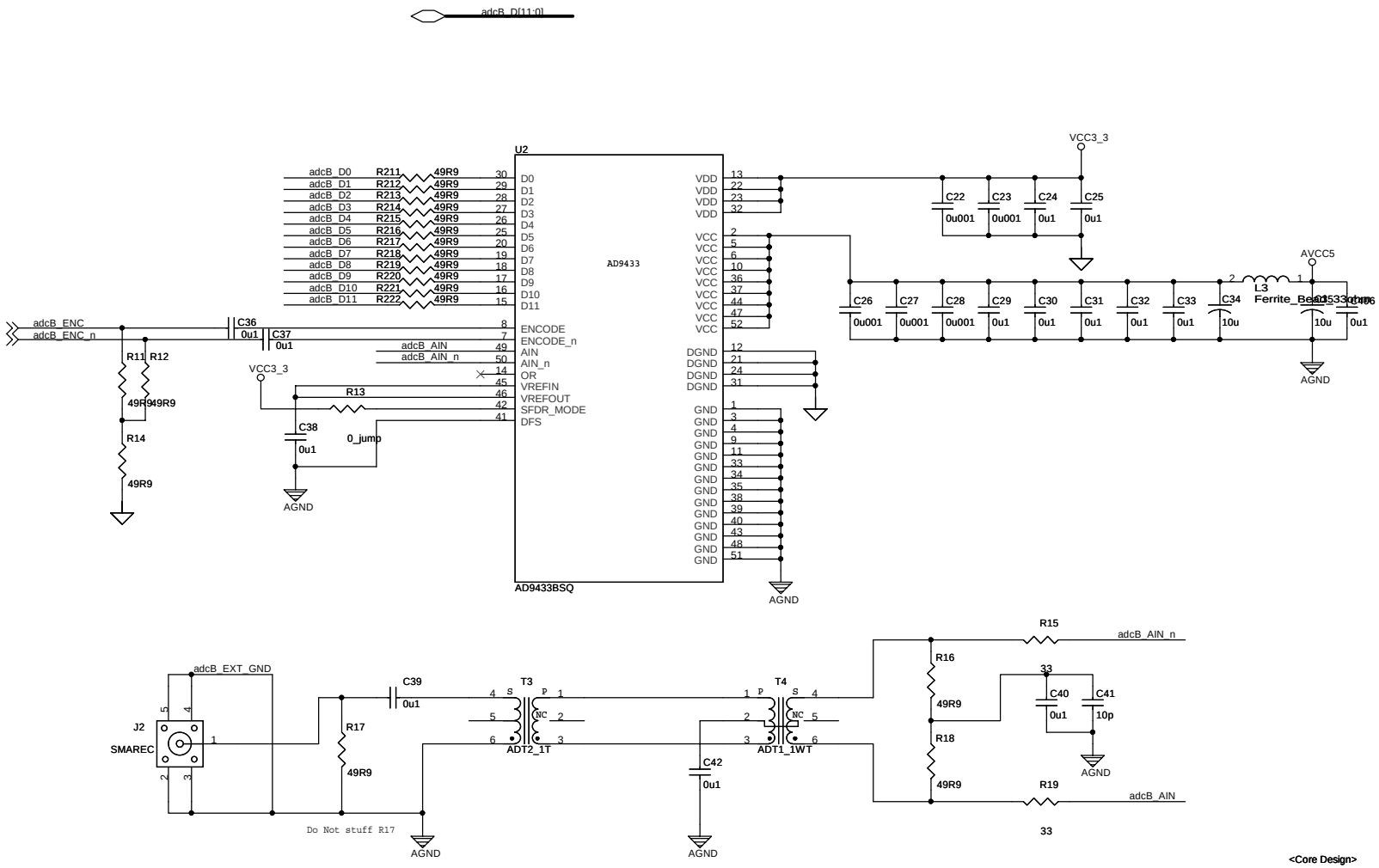
ADC B



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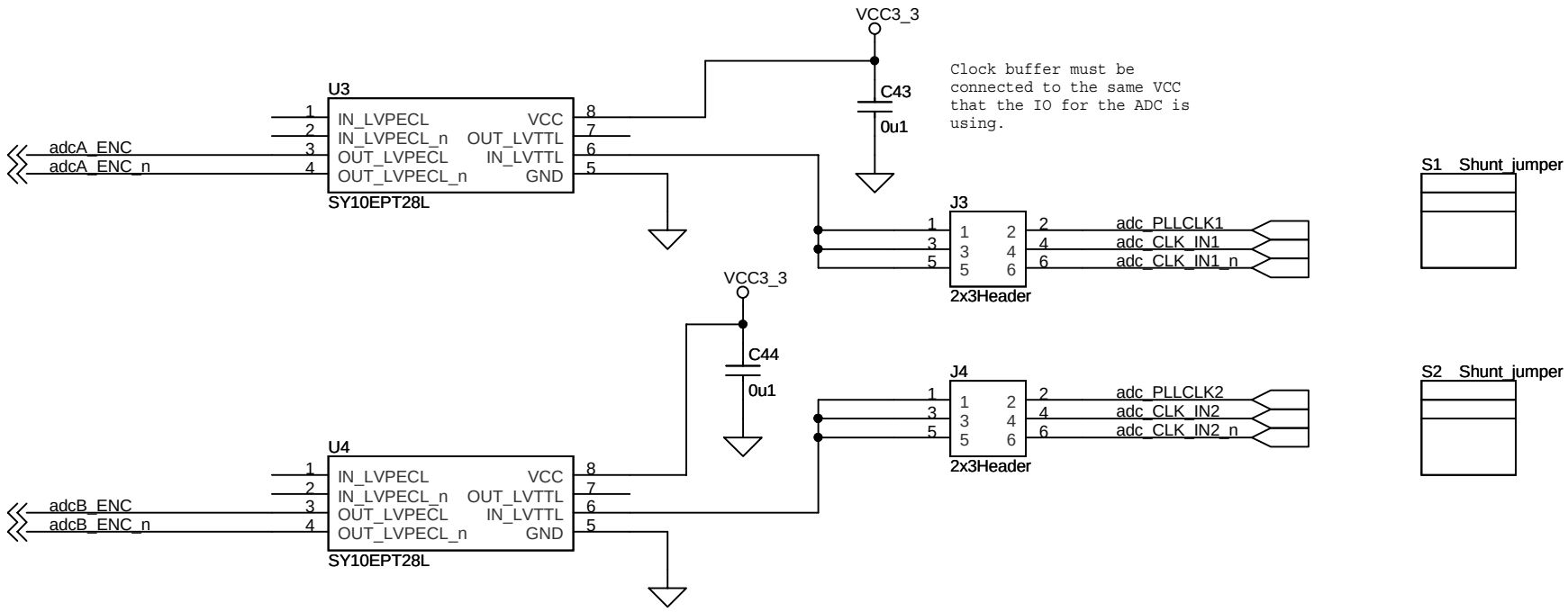
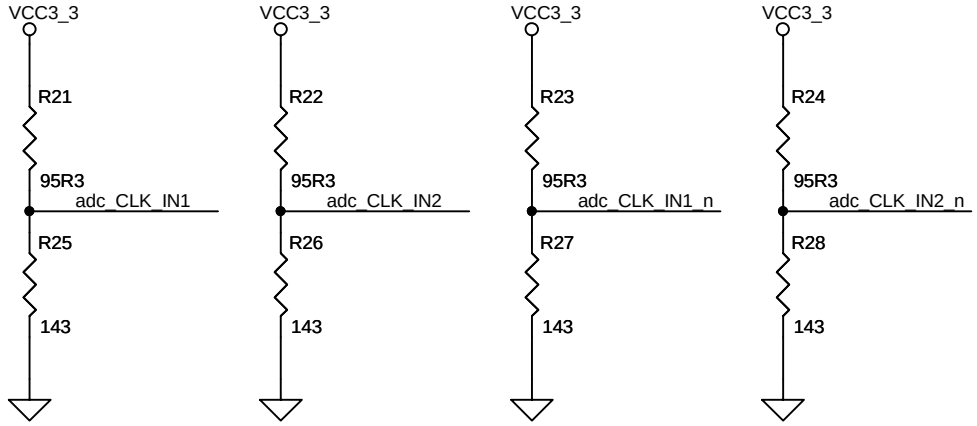
ADC Clock Selection





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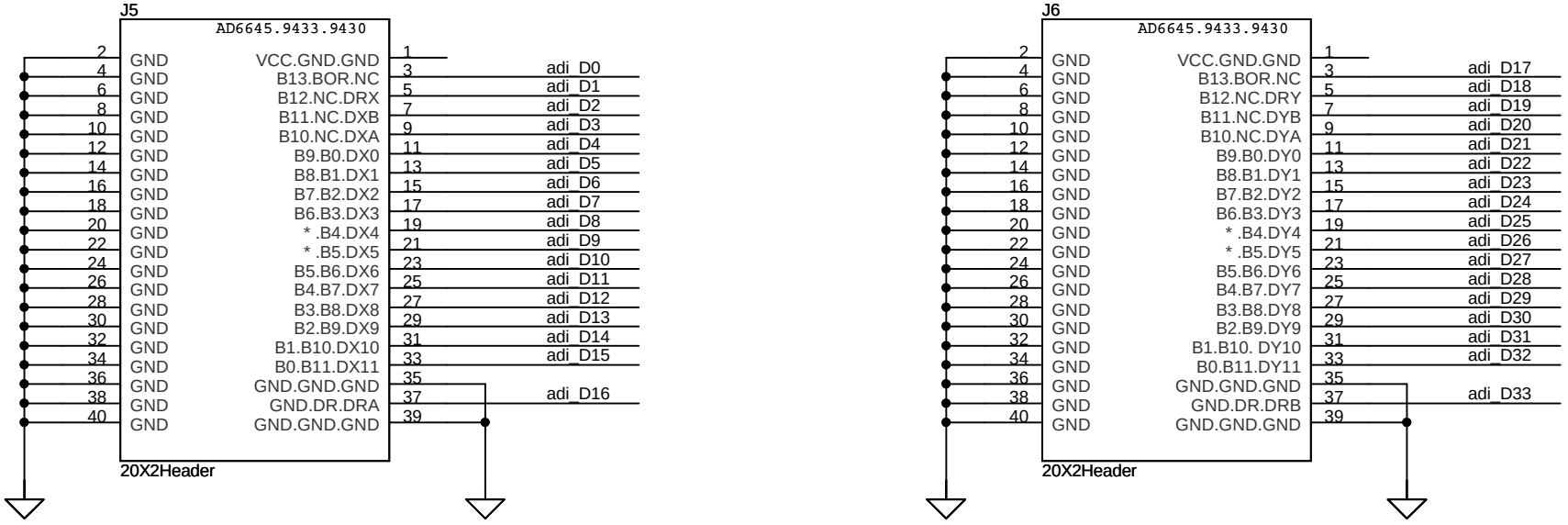
ADI Connector

adi_D[33:0]



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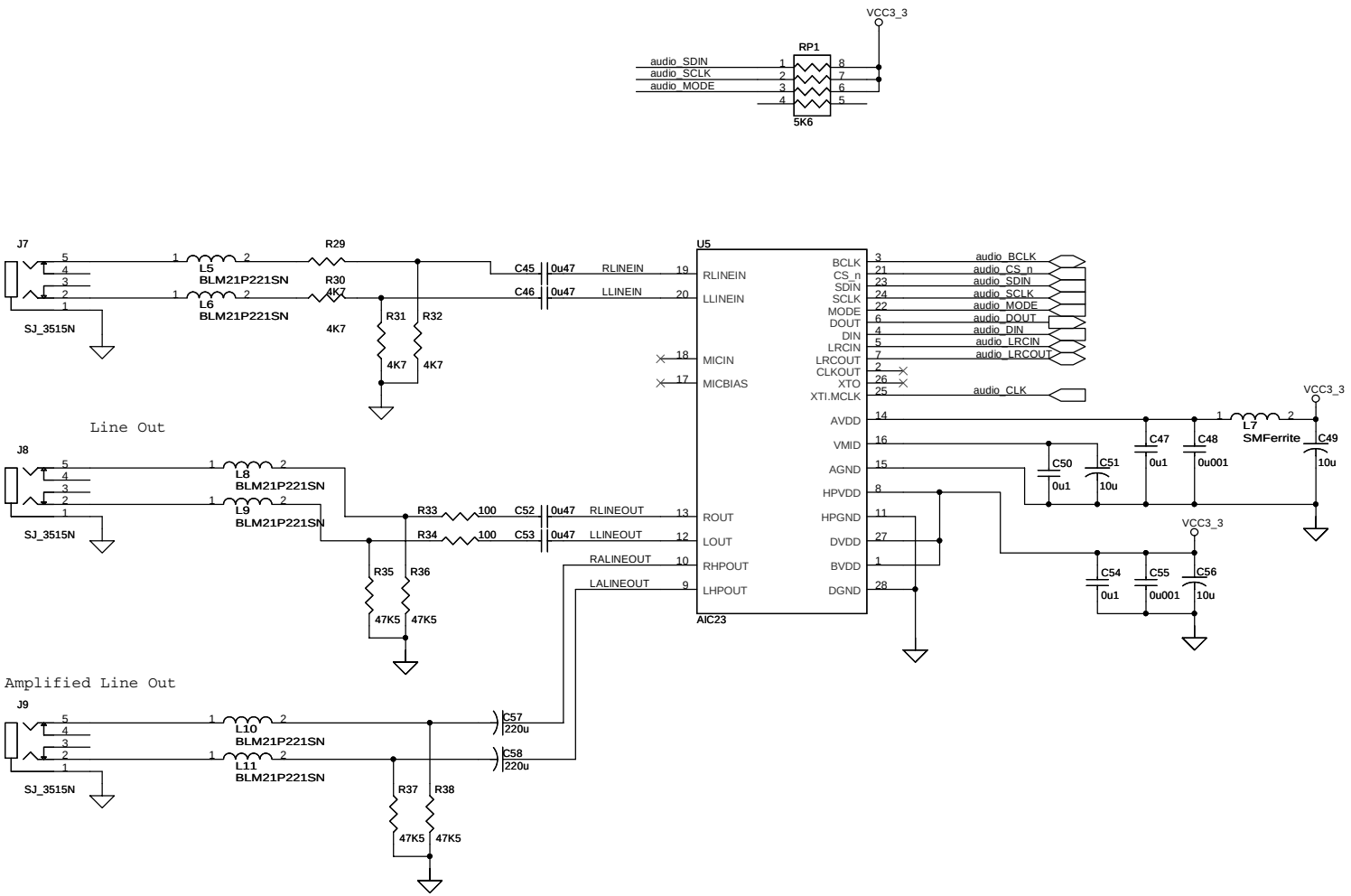

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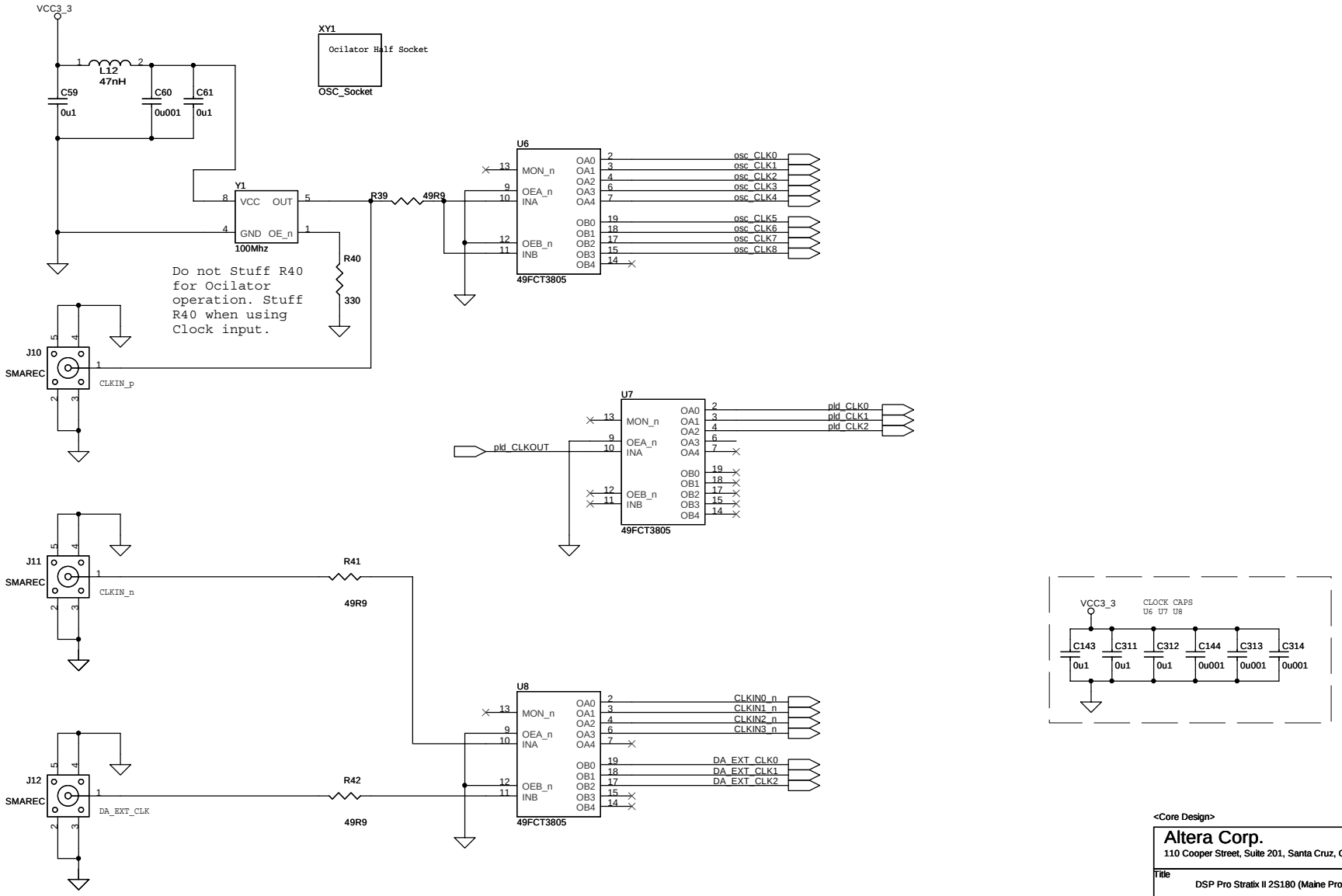
Clocks



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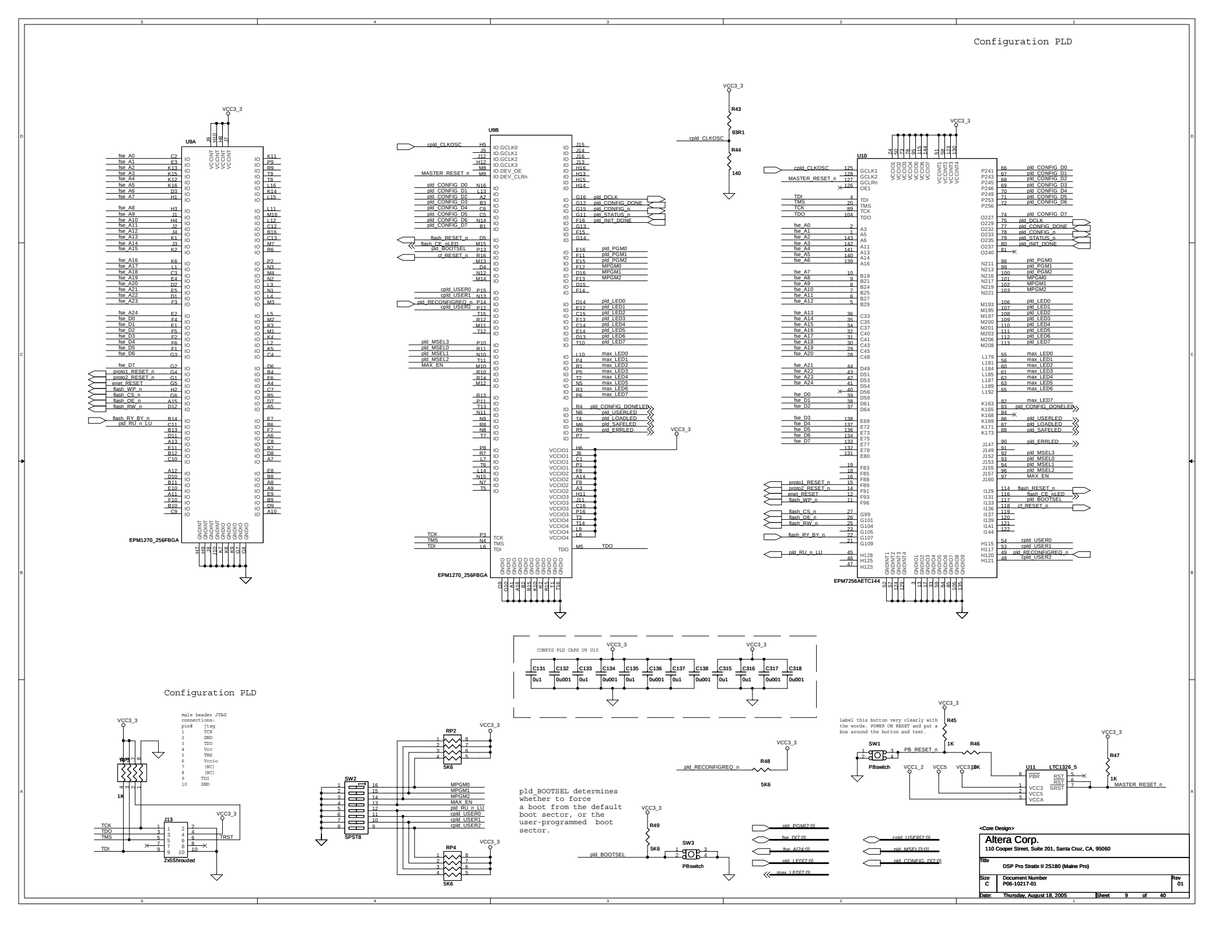
Configuration PLD
U9A
EPM1270_256FBGA
U9B
EPM1270_256FBGA
U10
EPM7256AETC144
R43
93R1
R44
140
cpld_CLKOSC
MASTER_RESET_n
pld_CONFIG_D0
pld_CONFIG_D1
pld_CONFIG_D2
pld_CONFIG_D3
pld_CONFIG_D4
pld_CONFIG_D5
pld_CONFIG_D6
pld_CONFIG_D7
flash_RESET_n
flash_CE_nLED
pld_BOOTSEL
cf_RESET_n
pld_DCLK
pld_CONFIG_DONE
pld_CONFIG_n
pld_STATUS_n
pld_INIT_DONE
pld_PGM0
pld_PGM1
pld_PGM2
MPGM0
MPGM1
MPGM2
pld_LED0
pld_LED1
pld_LED2
pld_LED3
pld_LED4
pld_LED5
pld_LED6
pld_LED7
max_LED0
max_LED1
max_LED2
max_LED3
max_LED4
max_LED5
max_LED6
max_LED7
pld_CONFIG_DONELED
pld_USERLED
pld_LOADLED
pld_SAFELED
pld_ERRLED
pld_MSEL3
pld_MSEL0
pld_MSEL1
pld_MSEL2
MAX_EN
cpld_USER0
cpld_USER1
pld_RECONFIGREQ_n
cpld_USER2
proto1_RESET_n
proto2_RESET_n
enet_RESET
flash_WP_n
flash_CS_n
flash_OE_n
flash_RW_n
flash_RY_BY_n
pld_RU_n_LU
TCK
TMS
TDI
TDO
VCC3_3
CONFIG PLD CAPS U9 U10
C131 C132 C133 C134 C135 C136 C137 C138
C315 C316 C317 C318
0u1
0u001
Configuration PLD
male header JTAG connections:
pin# jtag
1 TCK
2 GND
3 TDO
4 Vcc
5 TMS
6 Vccio
7 (NC)
8 (NC)
9 TDI
10 GND
RP3
1K
J13
2x5Shrouded
SW2
SPST8
RP2
RP4
5K6
MPGM0
MPGM1
MPGM2
MAX_EN
pld_RU_n_LU
cpld_USER0
cpld_USER1
cpld_USER2
pld_BOOTSEL determines whether to force a boot from the default boot sector, or the user-programmed boot sector.
R48
pld_RECONFIGREQ_n
R49
SW3
PBswitch
Label this button very clearly with the words POWER ON RESET and put a box around the button and text.
SW1
R45
R46
PB_RESET_n
U11
LTC1326_5
R47
pld_PGM[2:0]
fse_D[7:0]
fse_A[24:0]
pld_LED[7:0]
max_LED[7:0]
cpld_USER[2:0]
pld_MSEL[3:0]
pld_CONFIG_D[7:0]
<Core Design>
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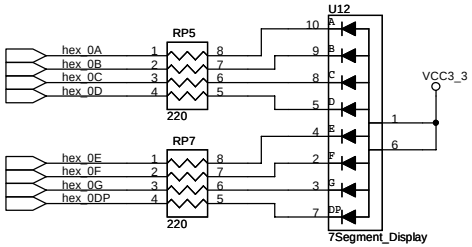

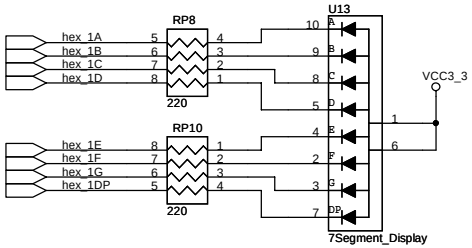

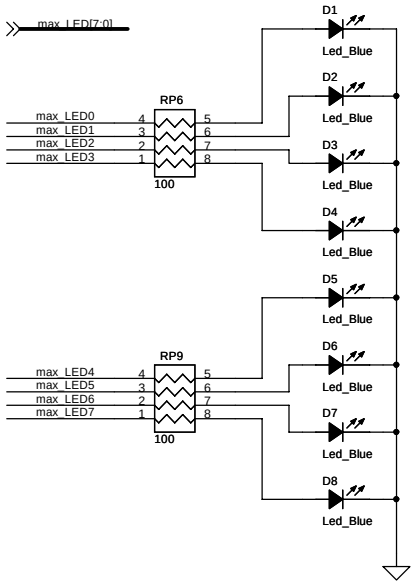

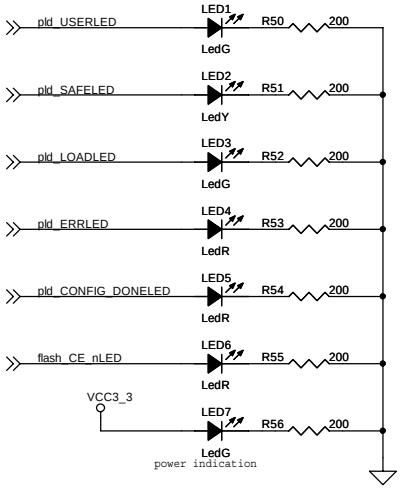

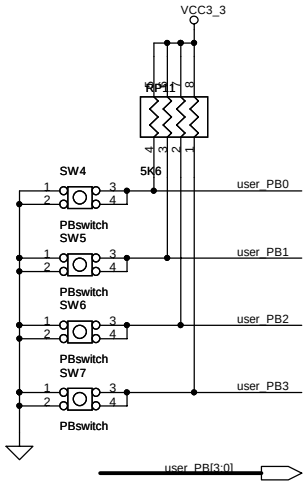

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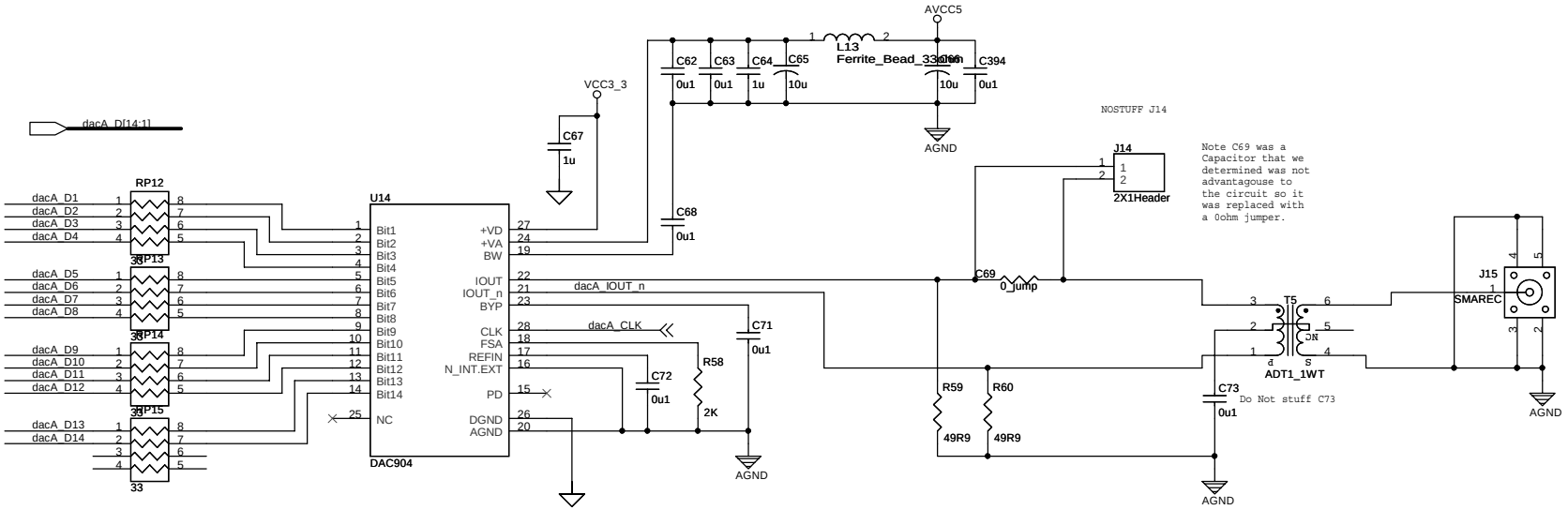
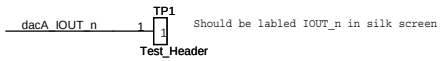
DAC A





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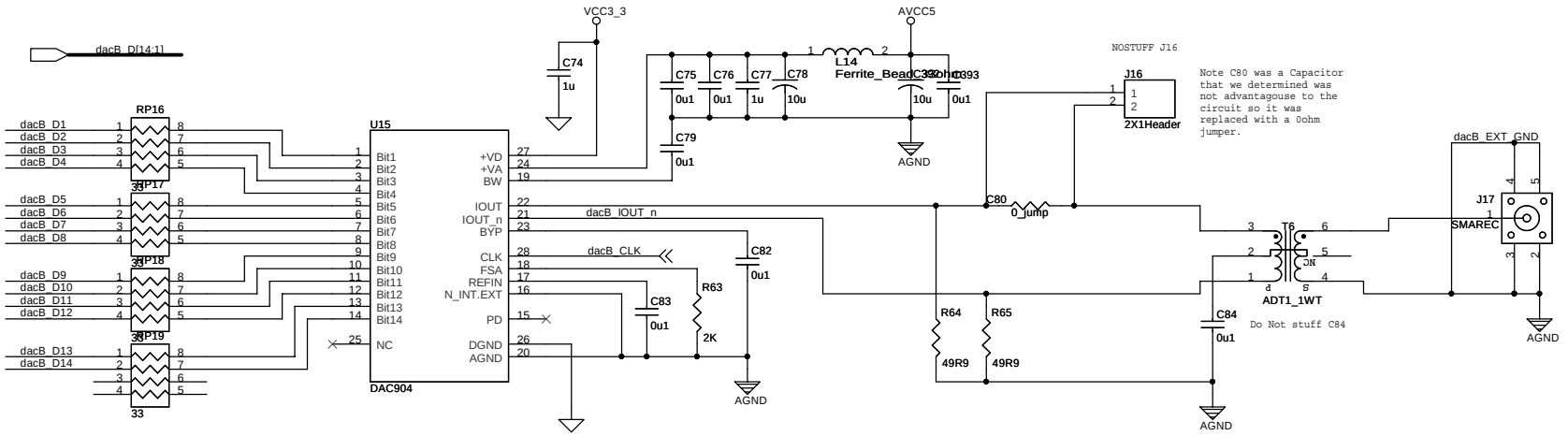
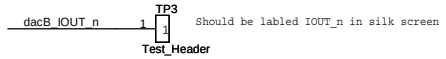
DAC B





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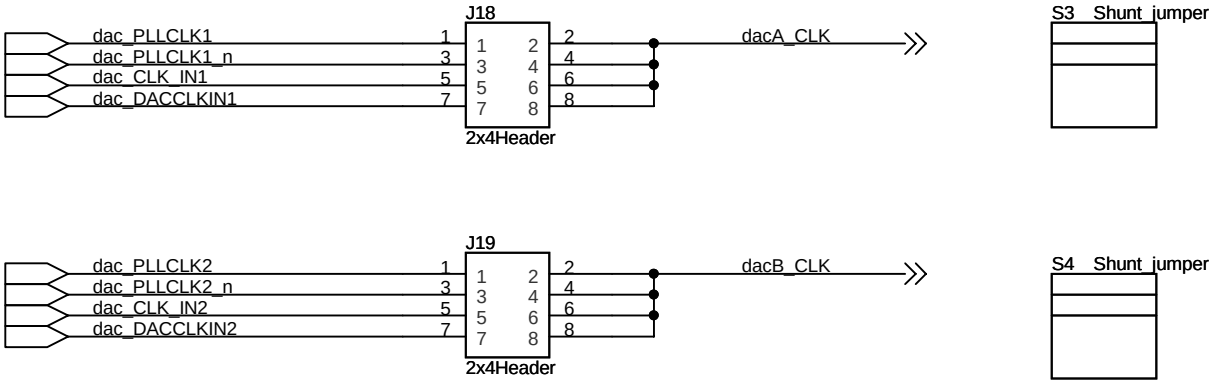
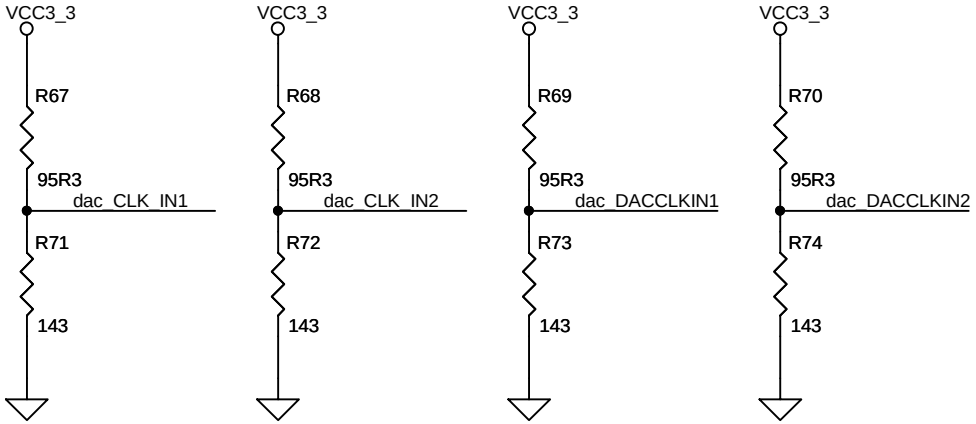
DAC Clock Jumper





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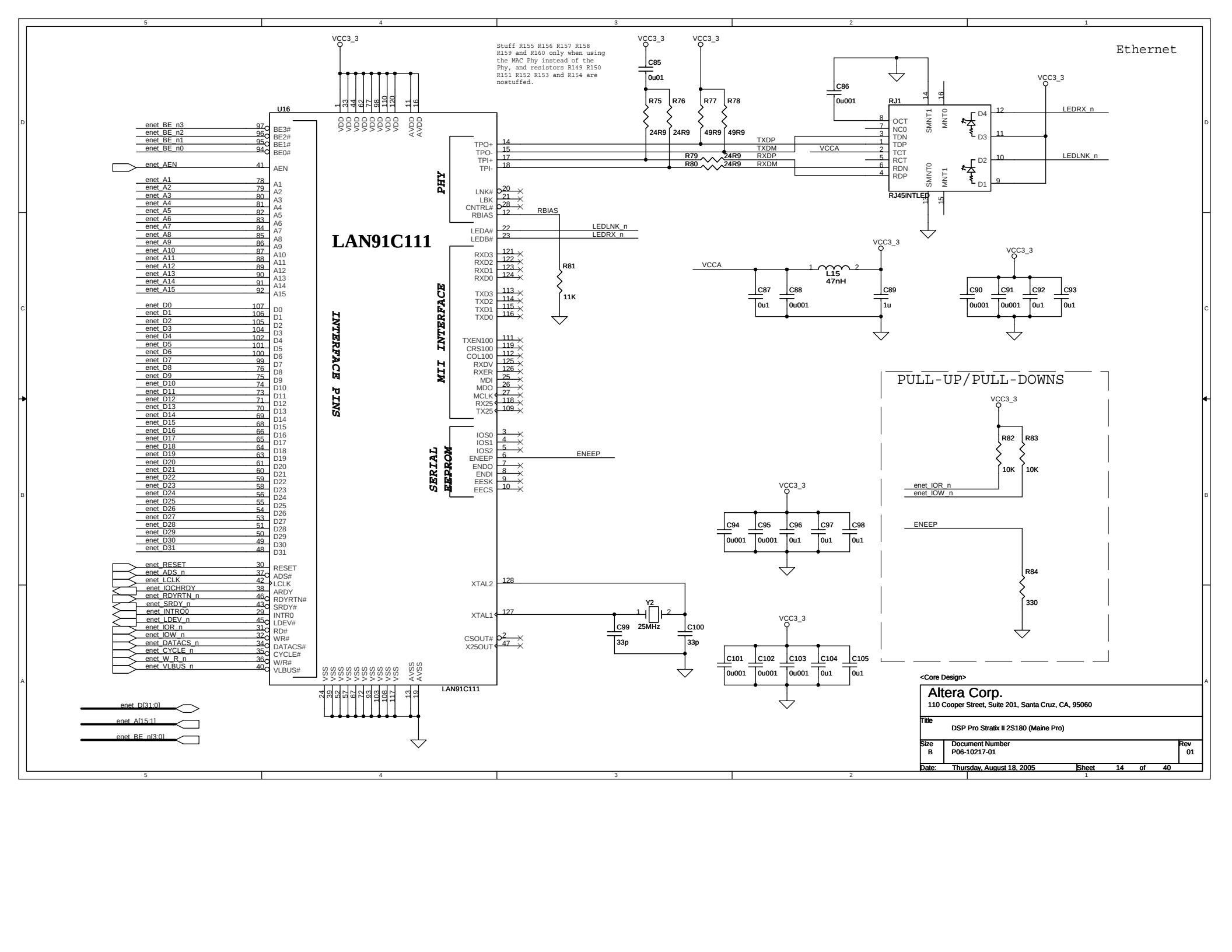
Ethernet
Stuff R155 R156 R157 R158 R159 and R160 only when using the MAC Phy instead of the Phy, and resistors R149 R150 R151 R152 R153 and R154 are nostuffed.
LAN91C111
U16
PHY
MII INTERFACE
SERIAL EEPROM
INTERFACE PINS
RJ1
RJ45INTLED
PULL-UP/PULL-DOWNS
Y2
25MHz
<Core Design>
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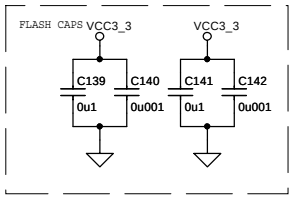

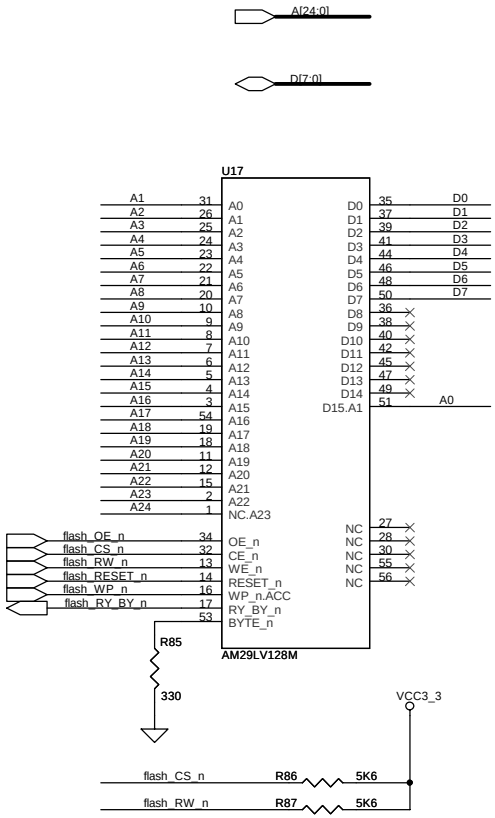

Flash chip is 16M x 8 for
16Mbytes of flash

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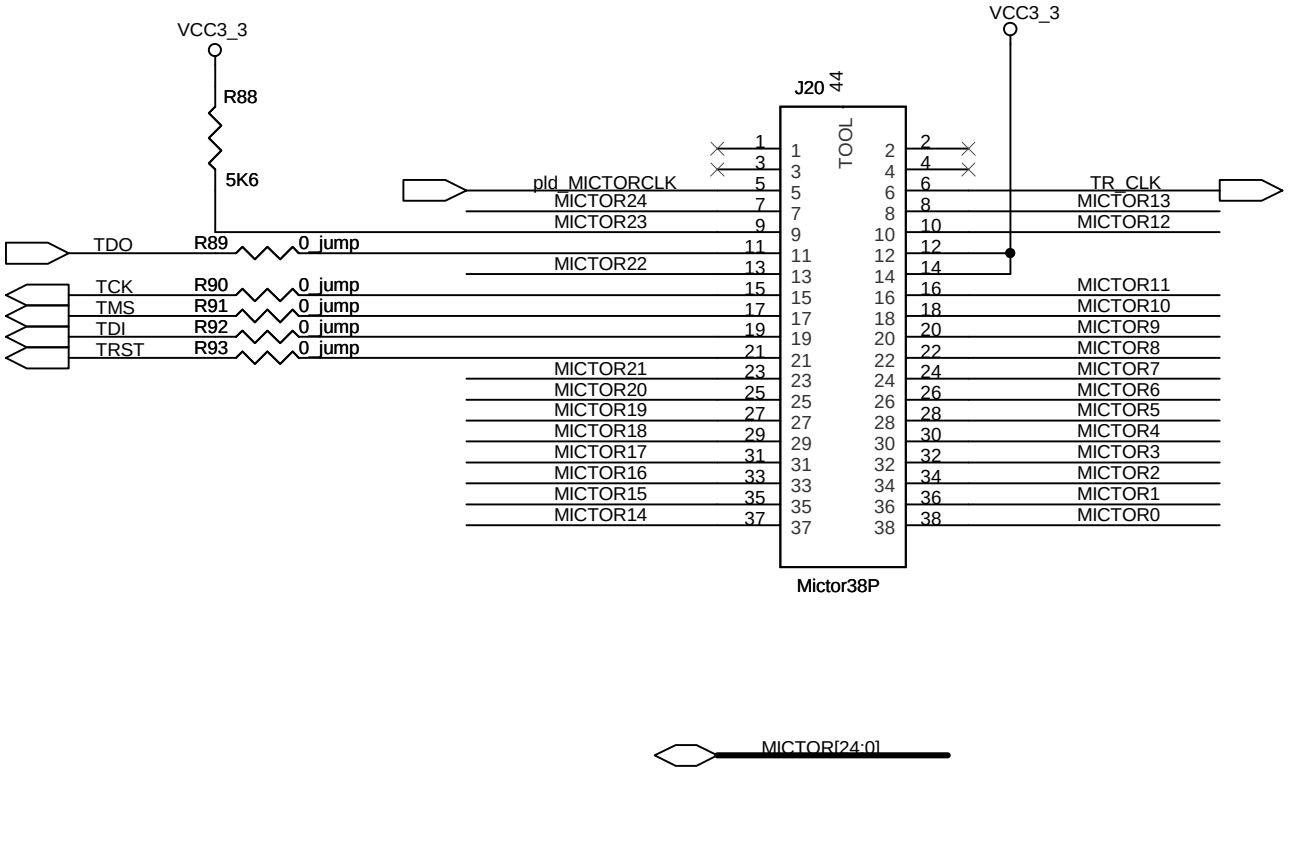
Mictor Connector



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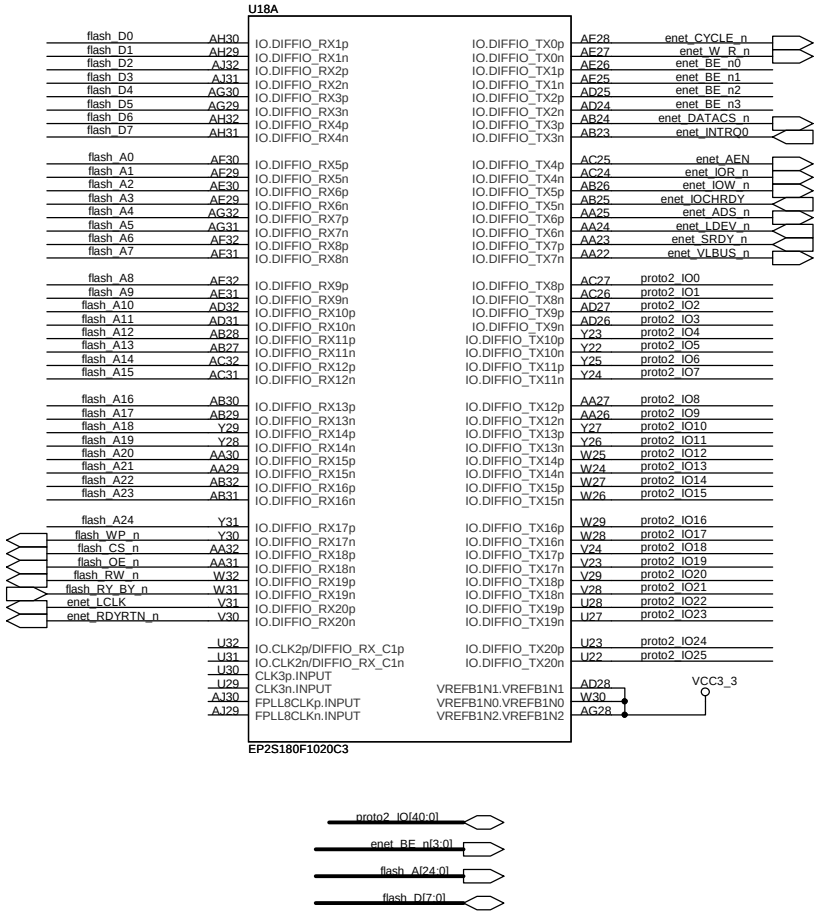

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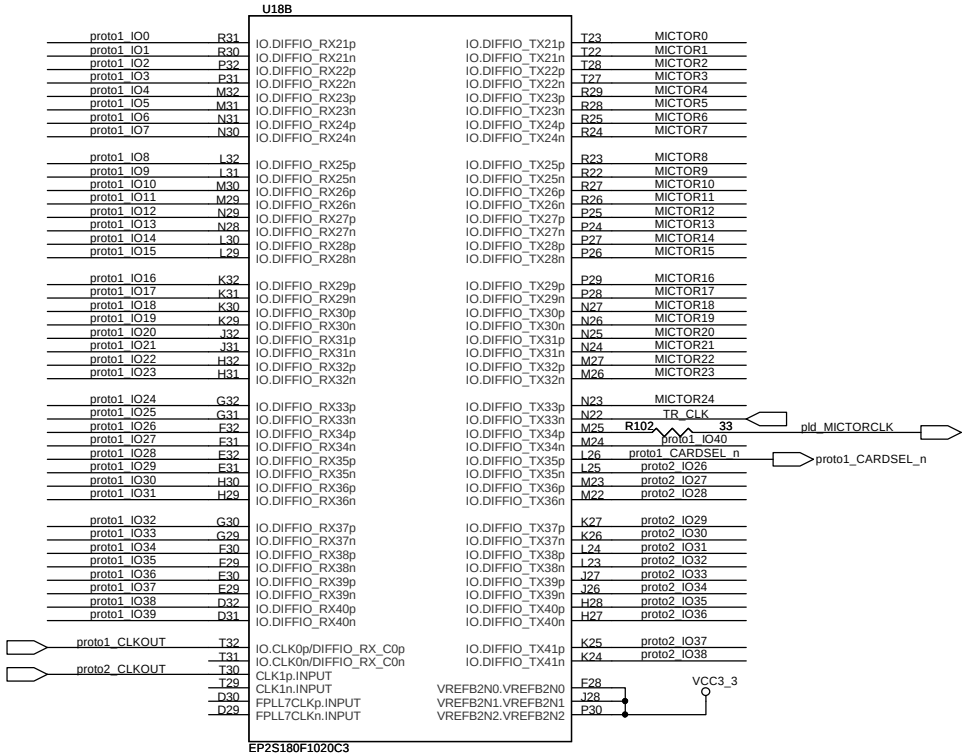
PLD Bank 2



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proto1_IO[40:0]

proto2_IO[40:0]

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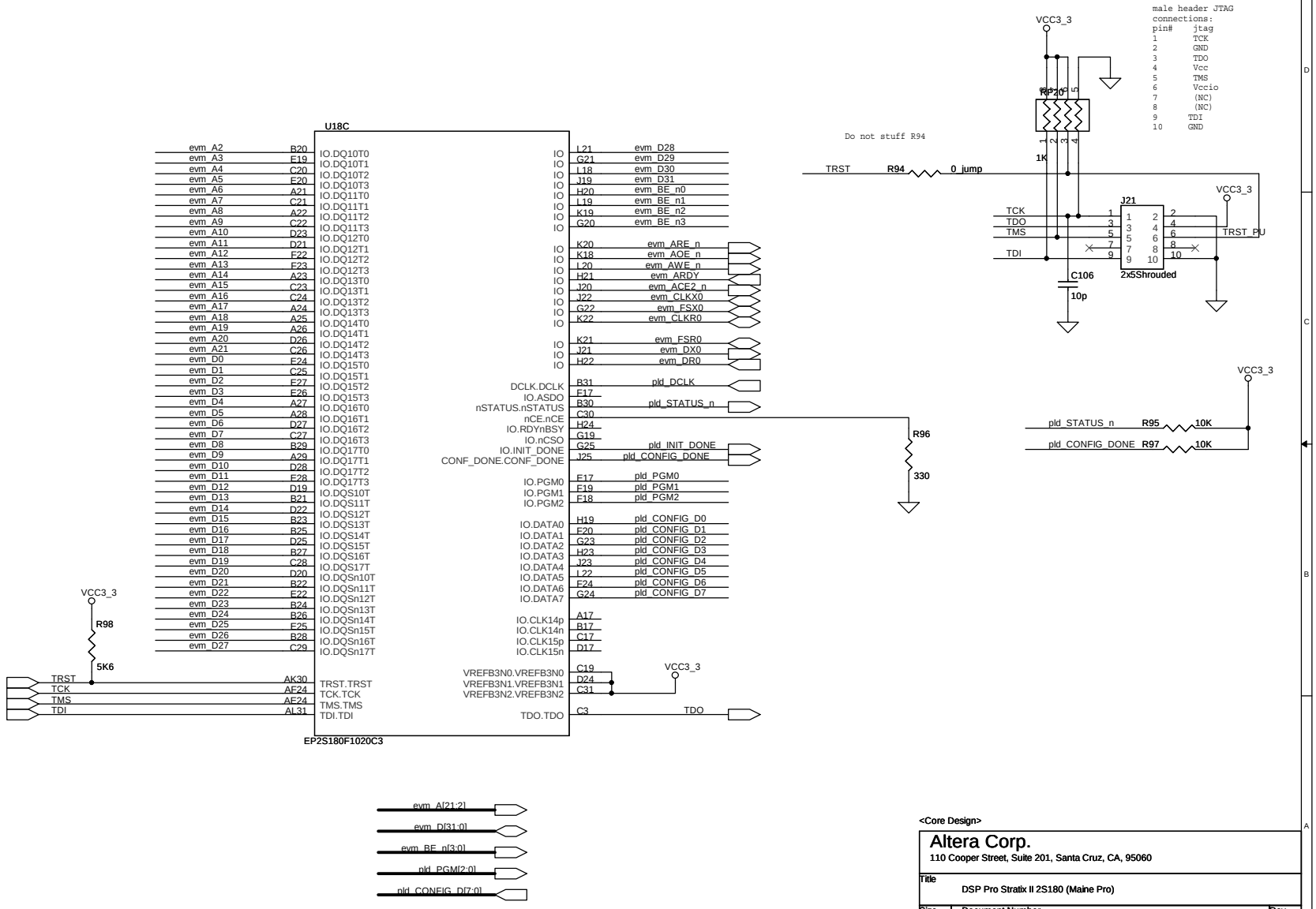
PLD Bank 3



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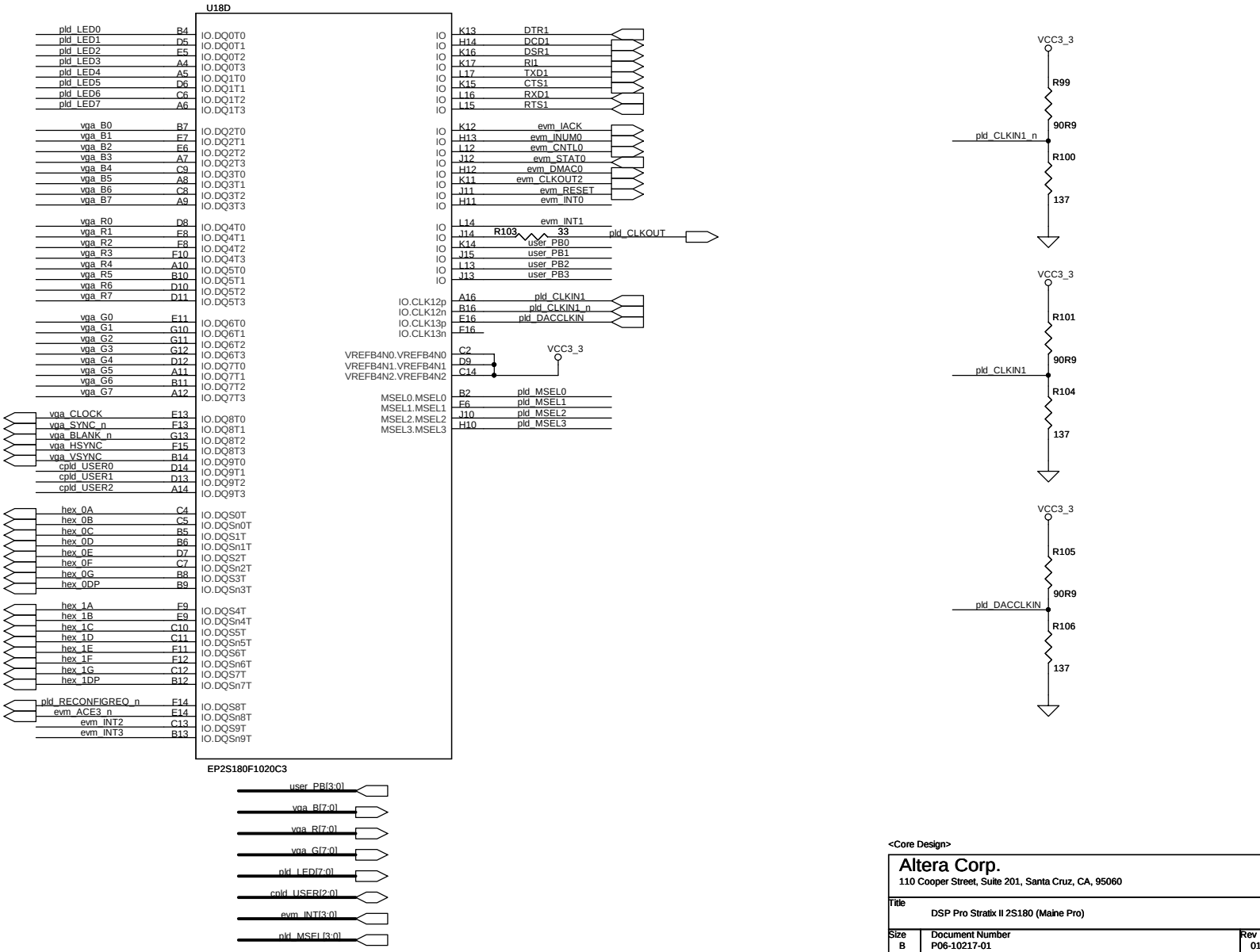
PLD Bank 4



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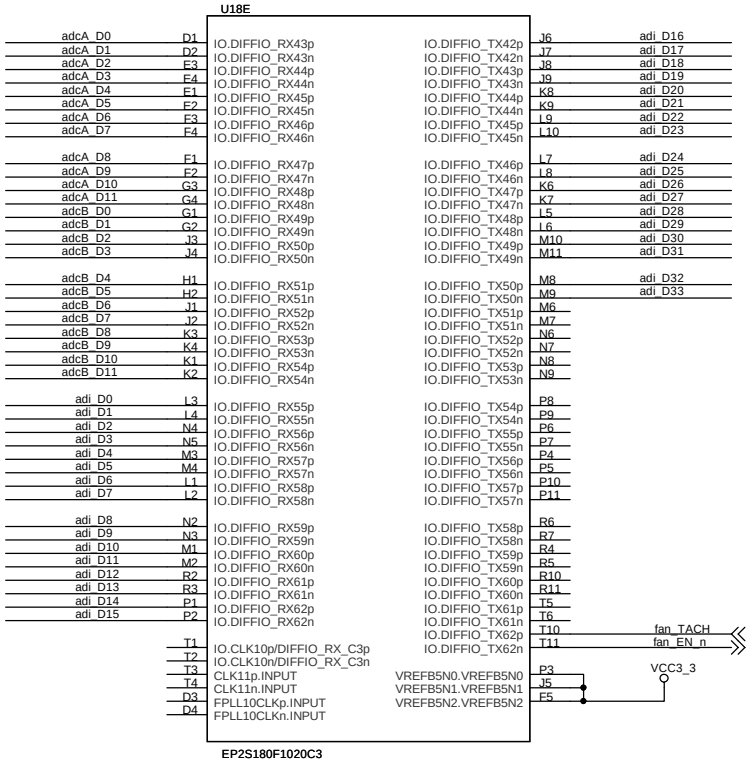
PLD Bank 5



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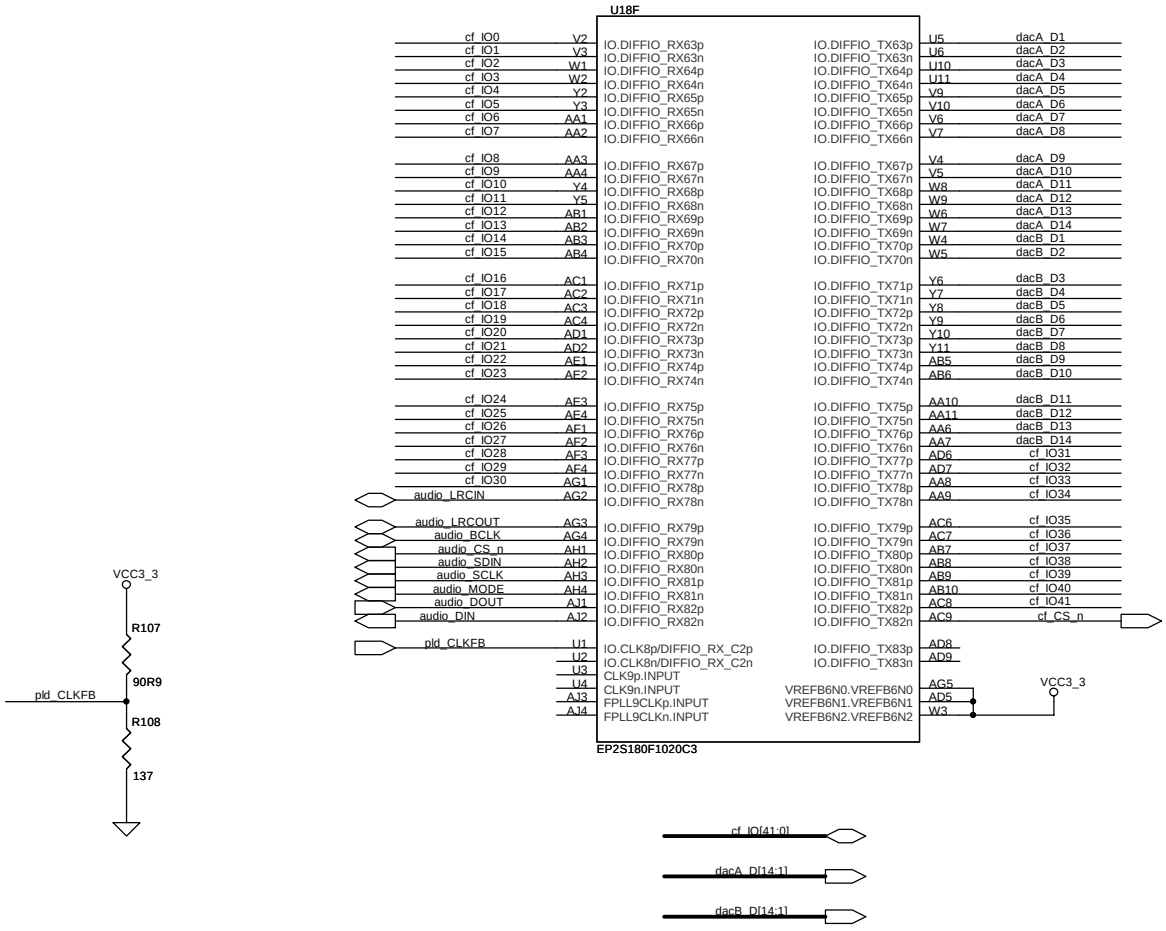
PLD Bank 6



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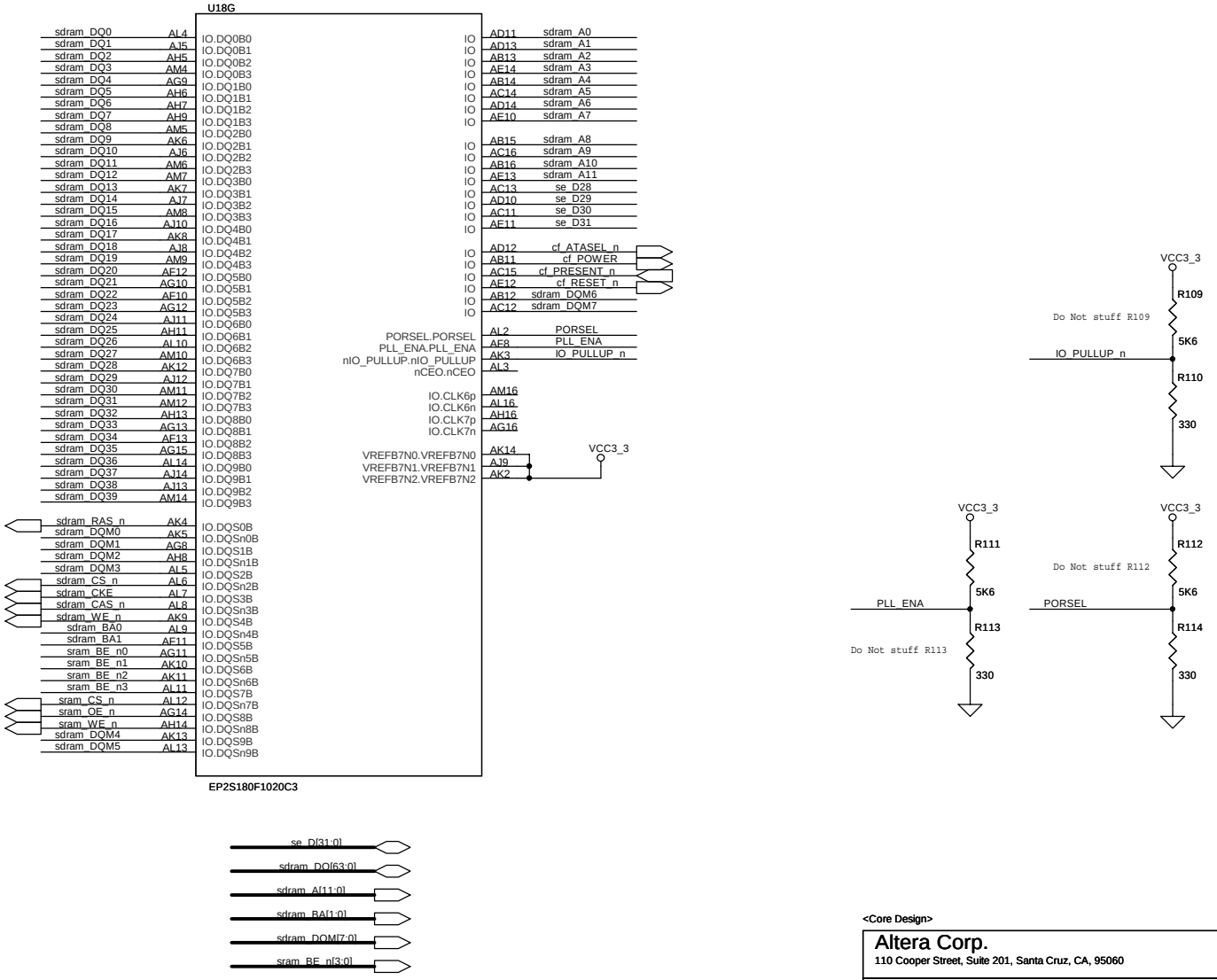
PLD Bank 7



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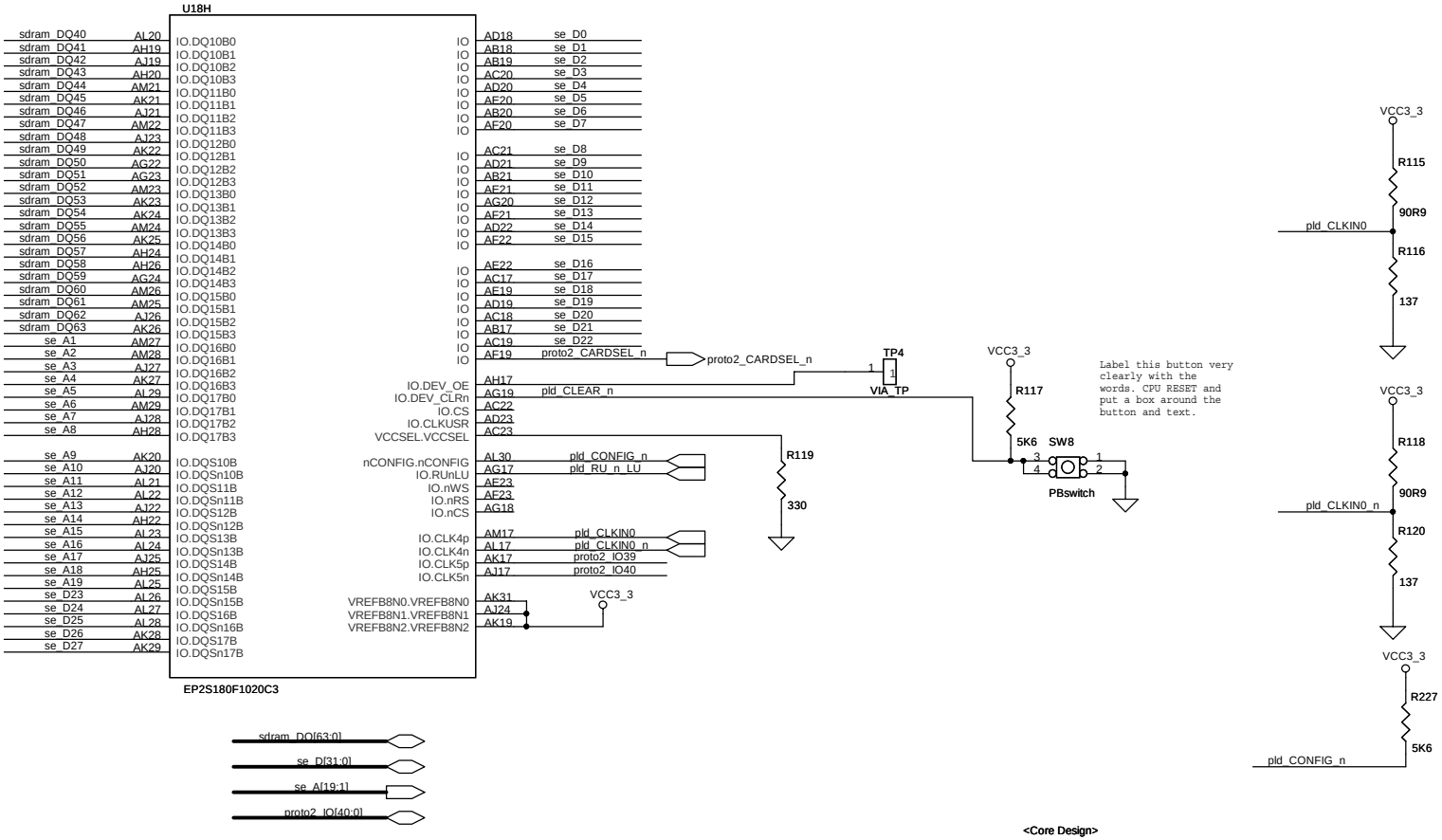
PLD Bank 8



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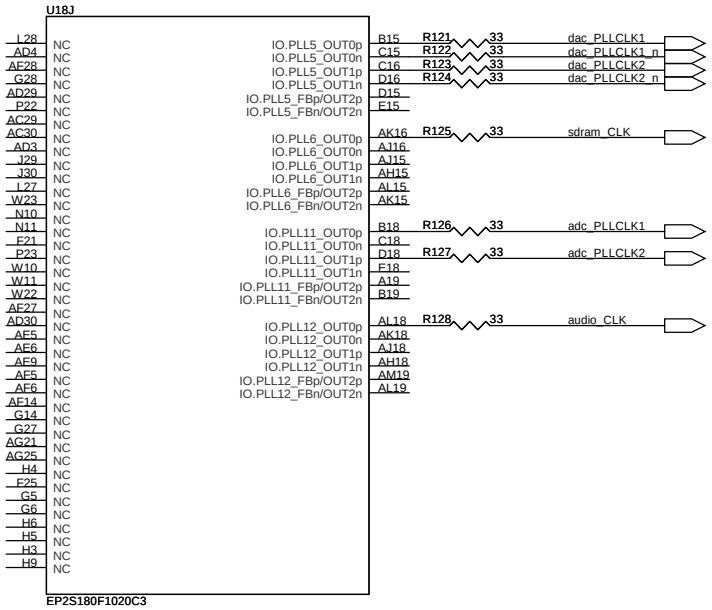

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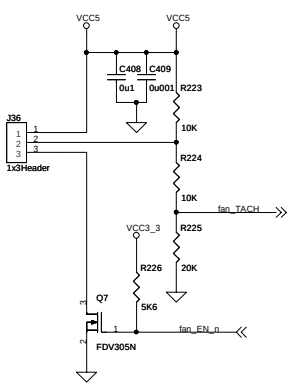

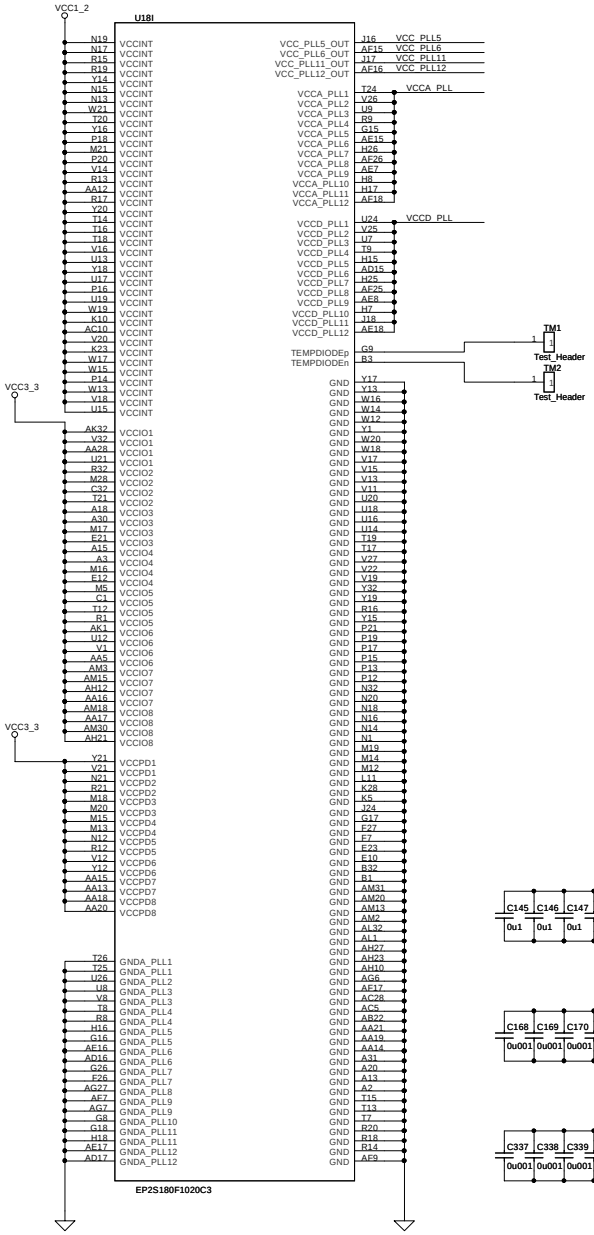

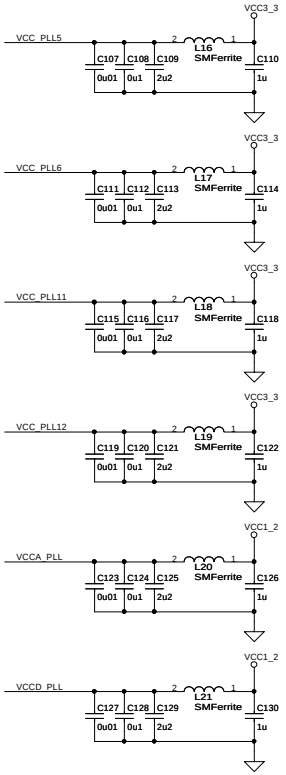

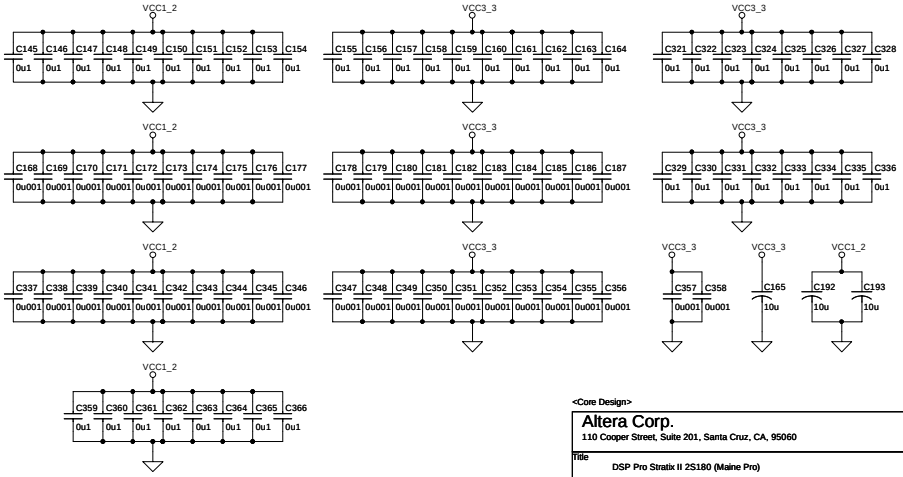

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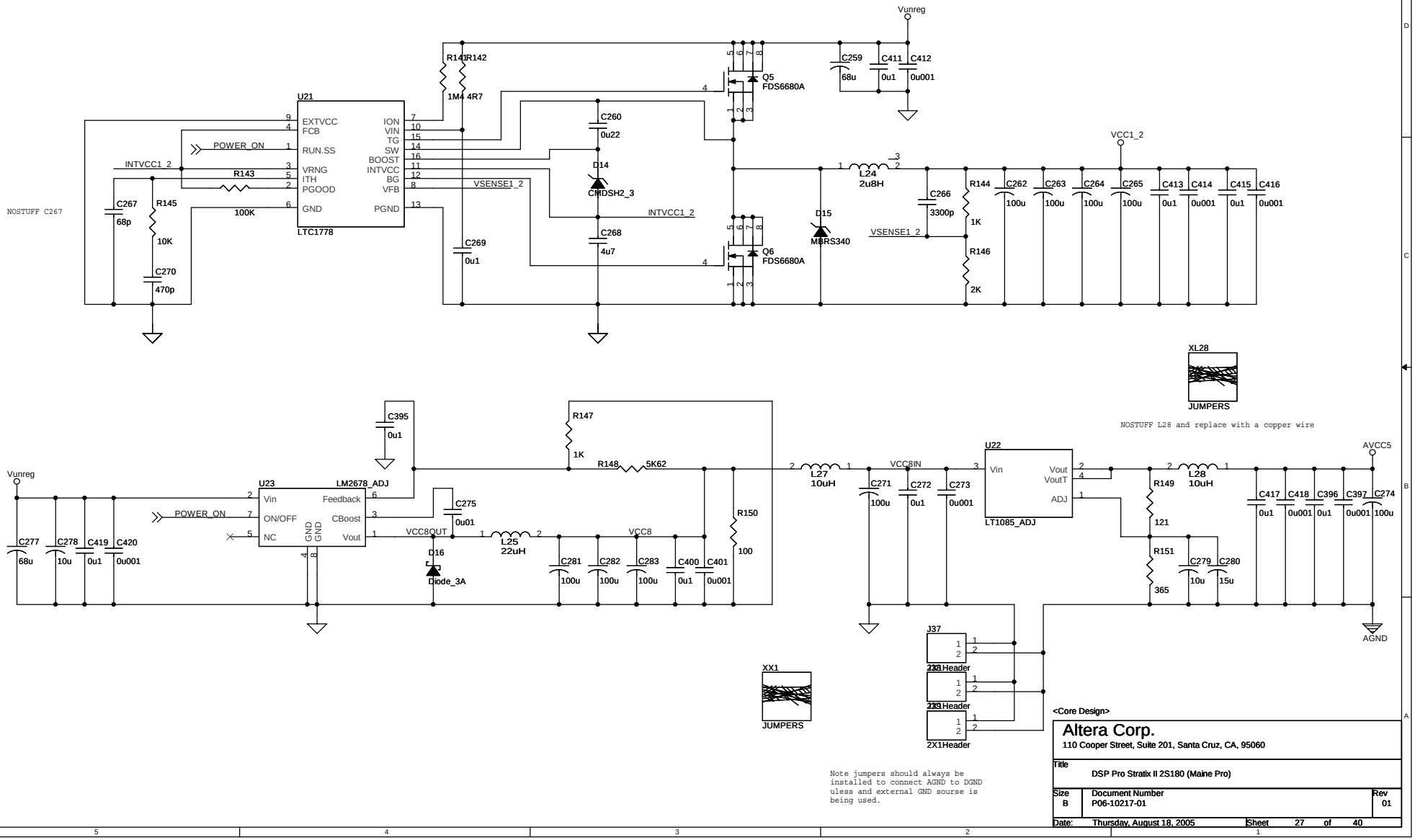

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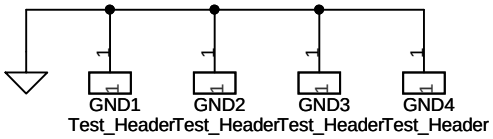
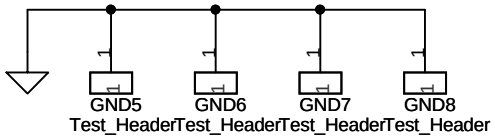
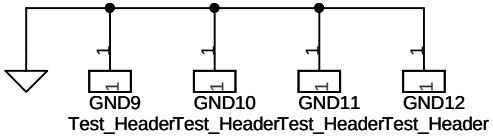
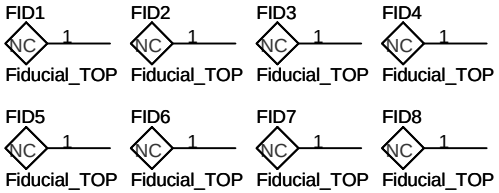
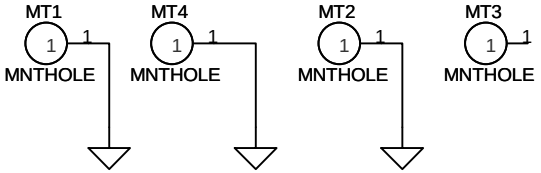
Reset and Test headers

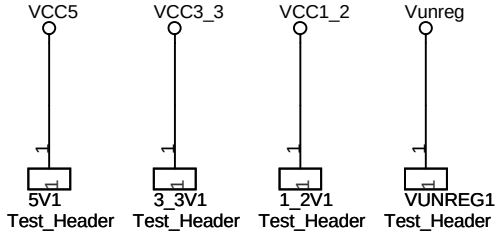


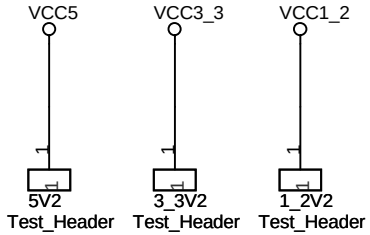


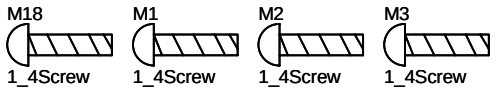


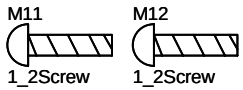


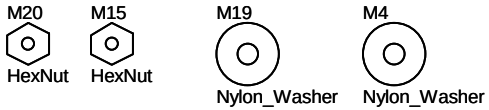


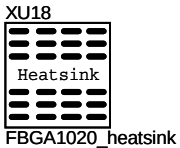


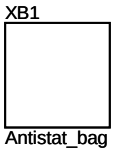


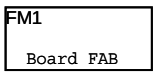












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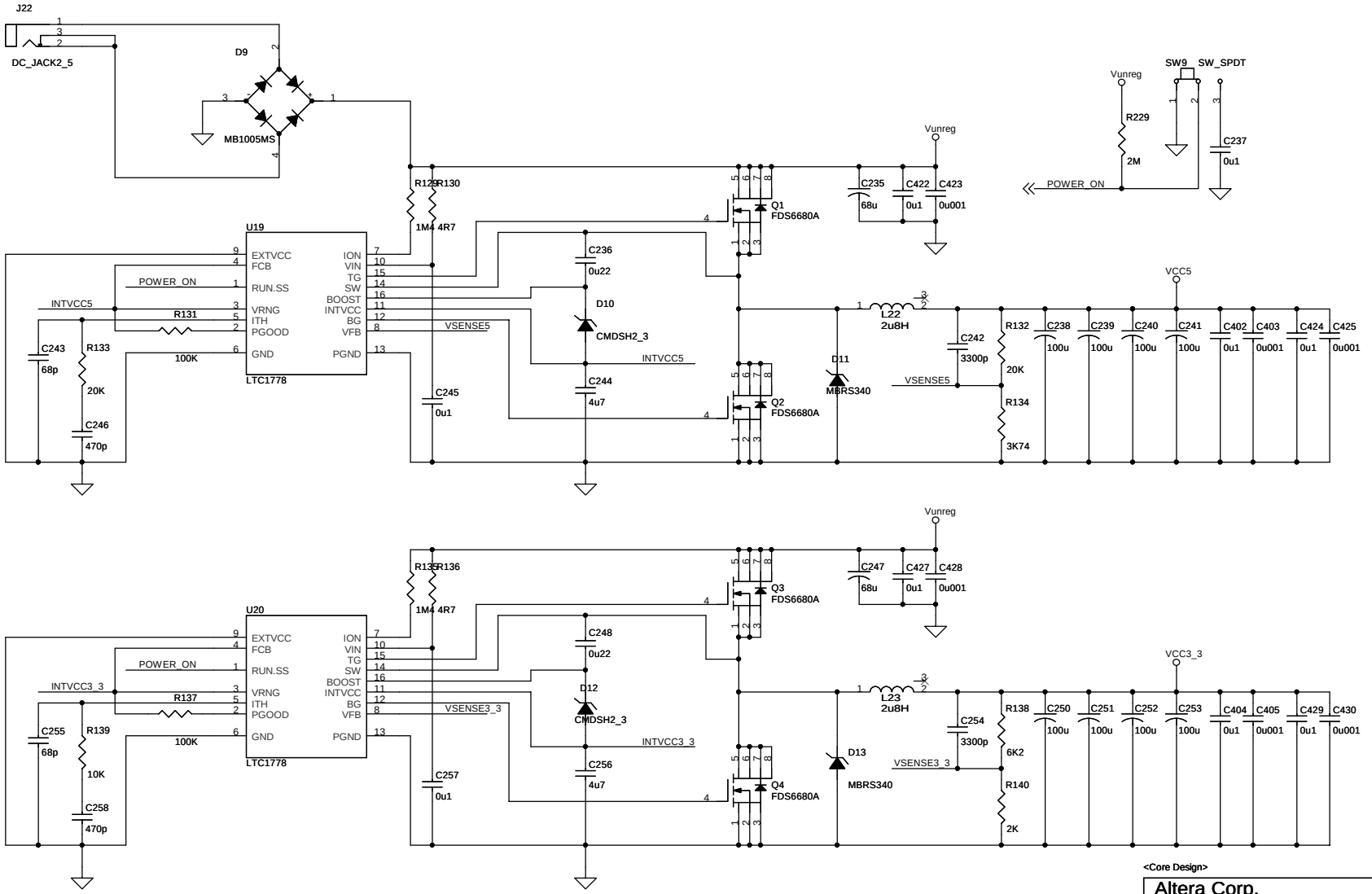

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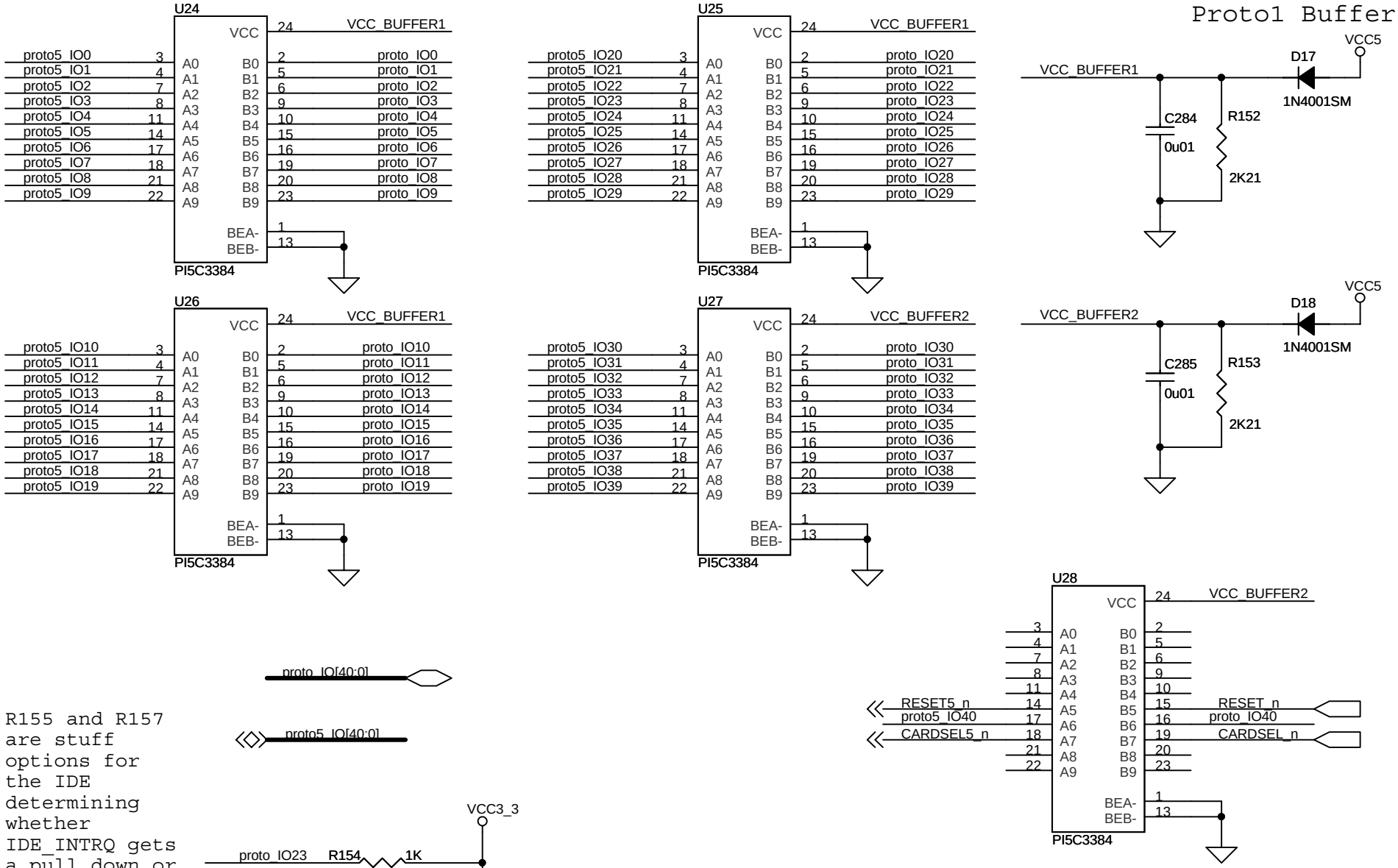
Proto1 Buffers



R155 and R157 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R155 should be a nostuff for production.

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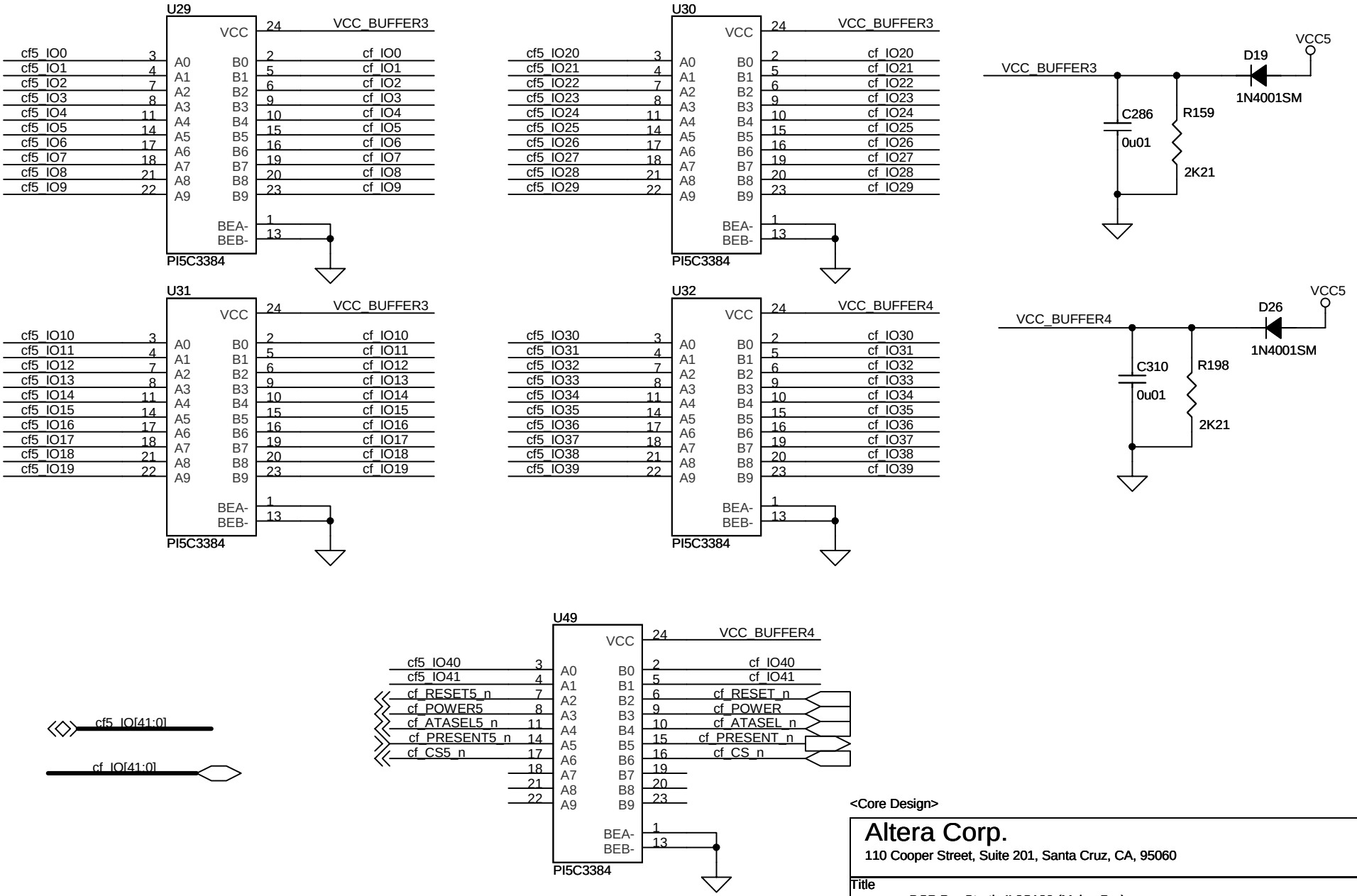
Proto1 Buffers



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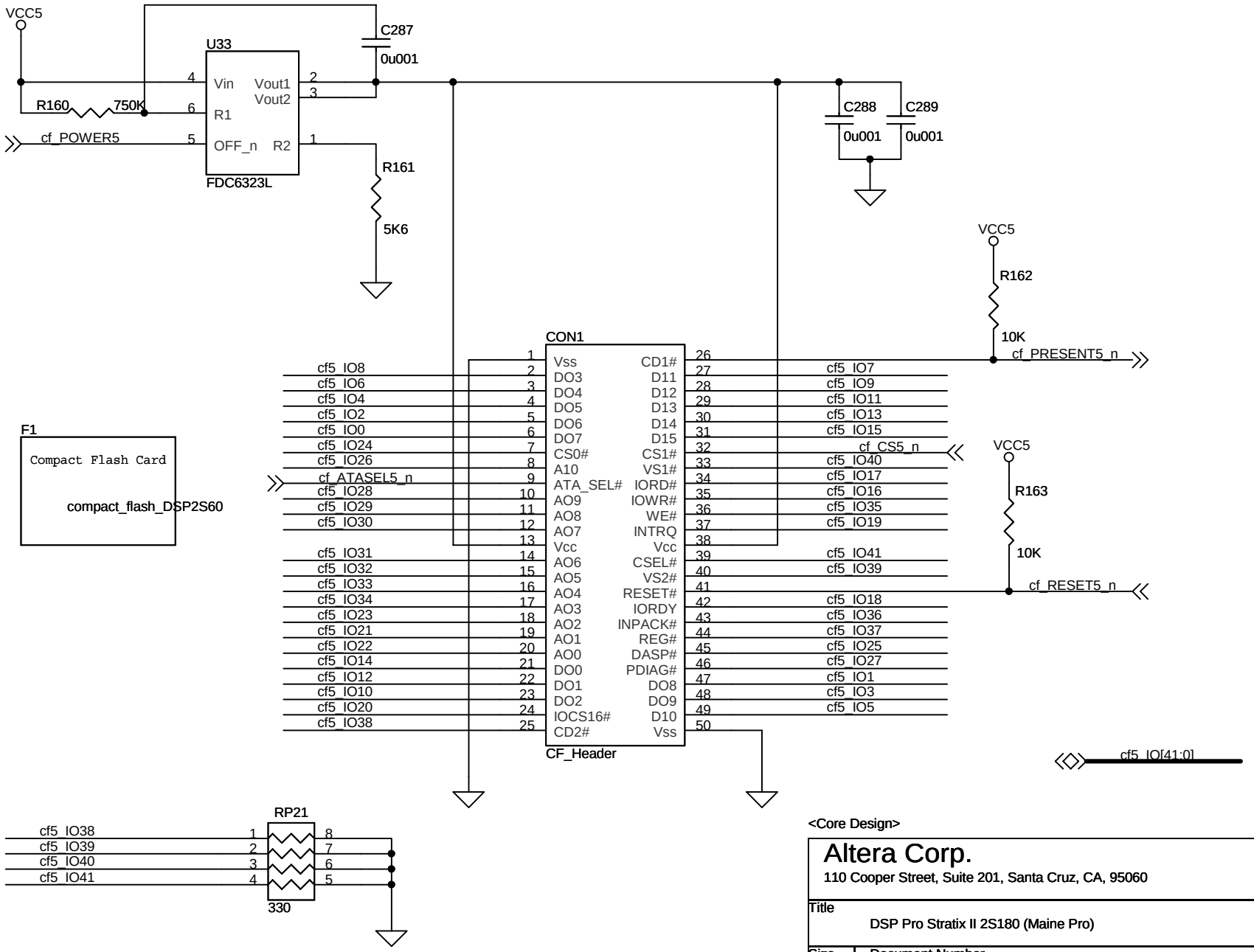
Compact Flash Socket



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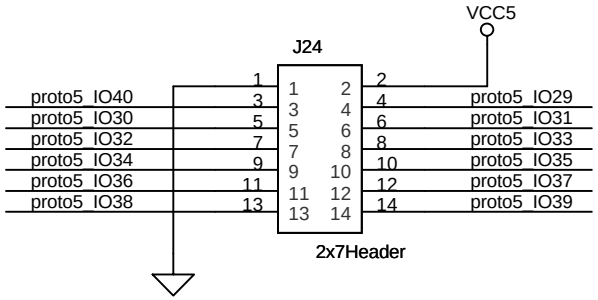
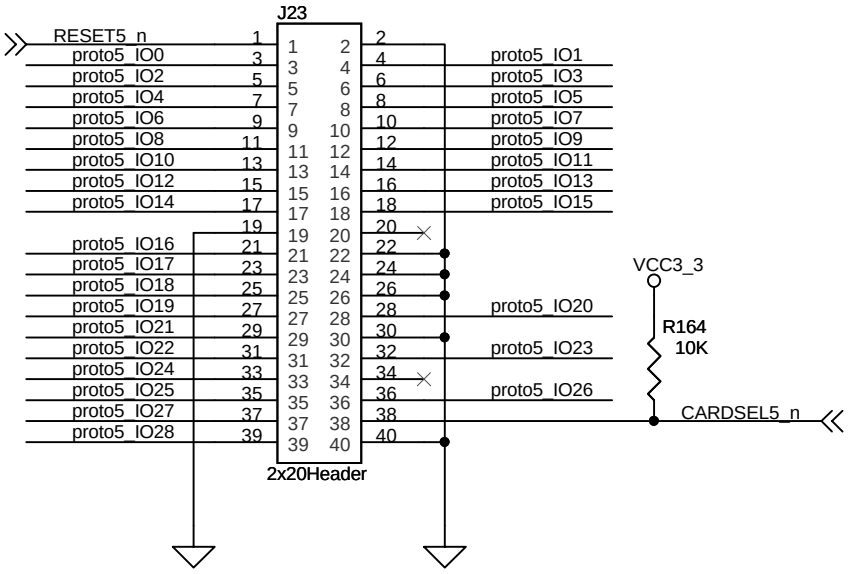
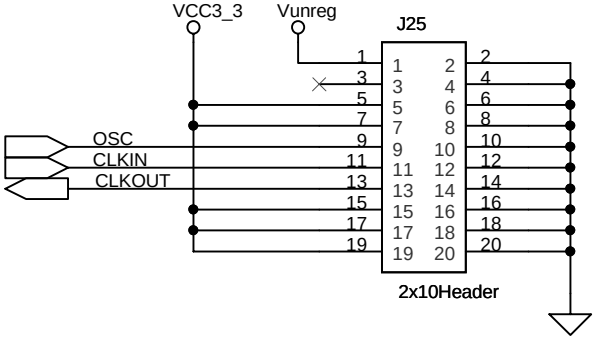
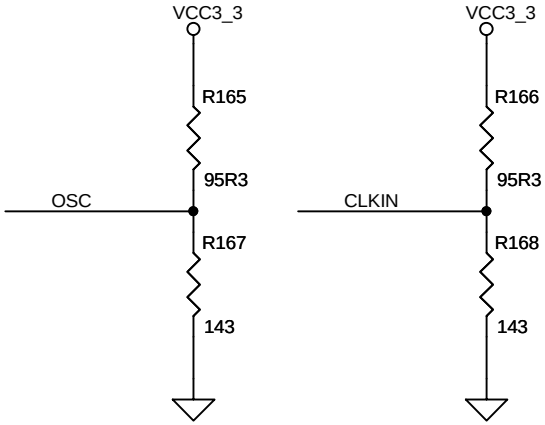
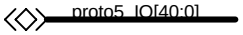
Protocard 1

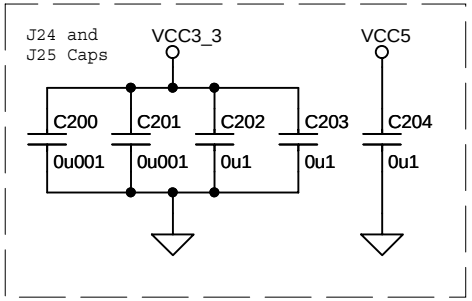












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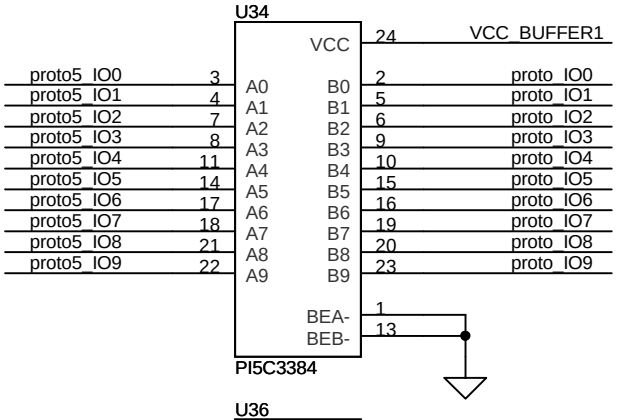
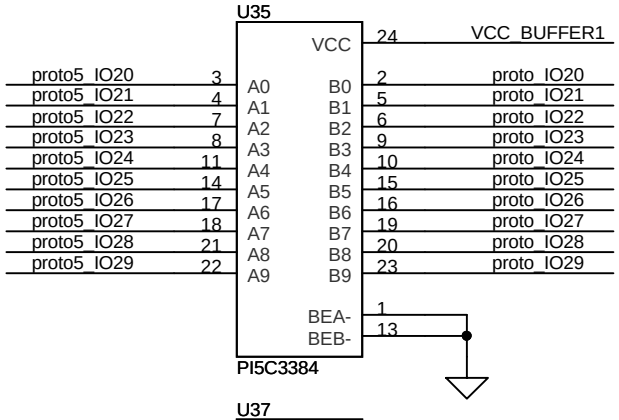
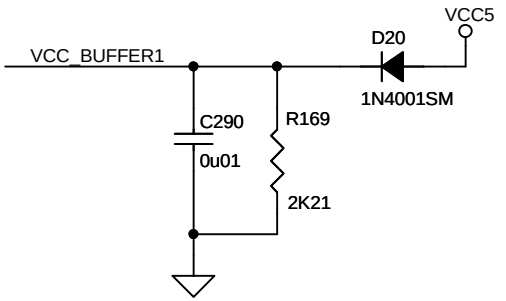
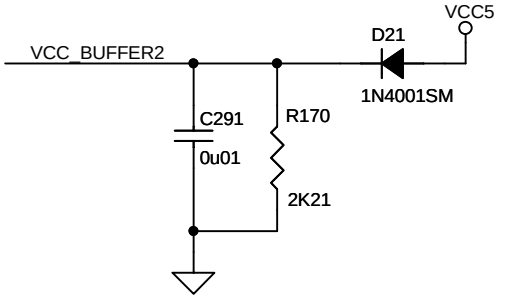
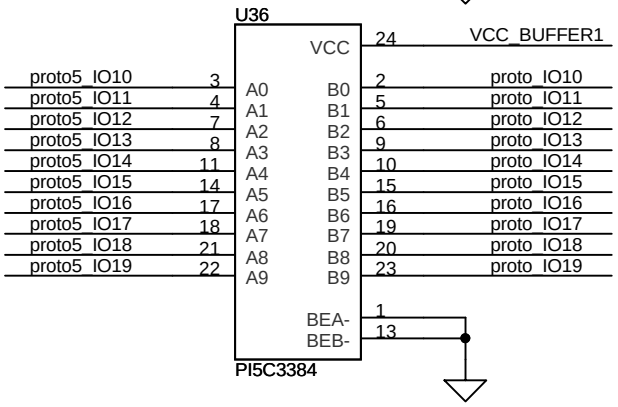
Proto2 Buffers

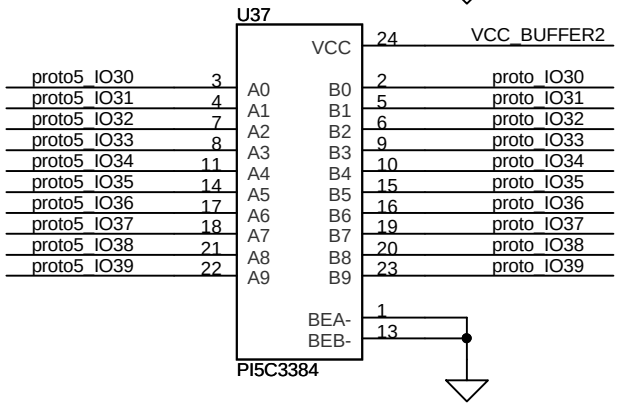




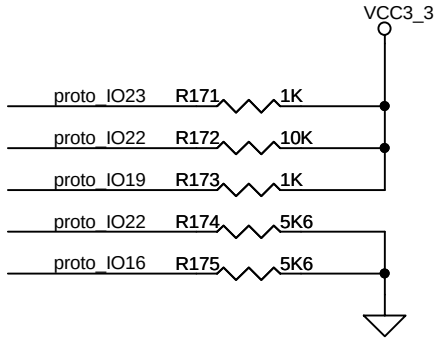


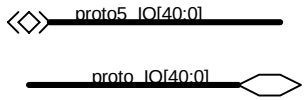


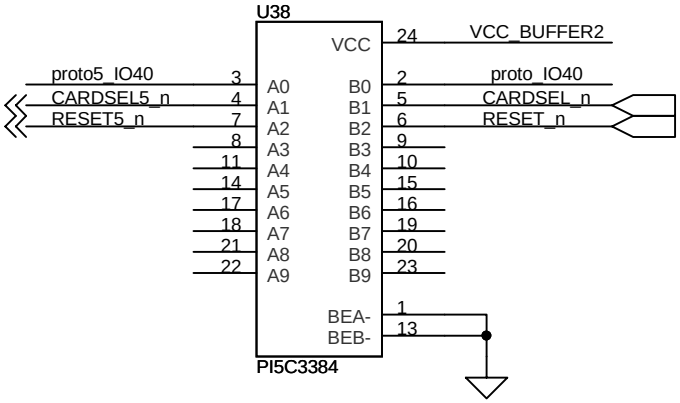




R172 and R174 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R172 should be a nostuff for production.







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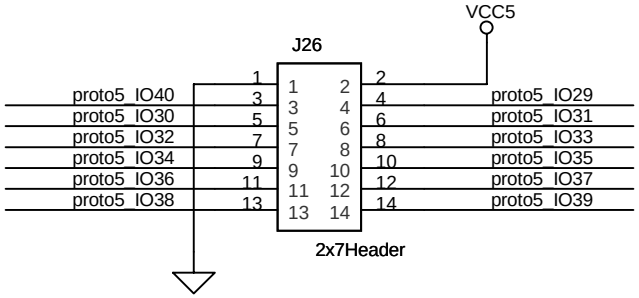

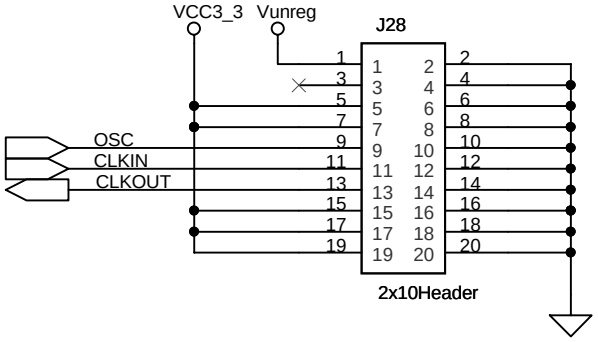

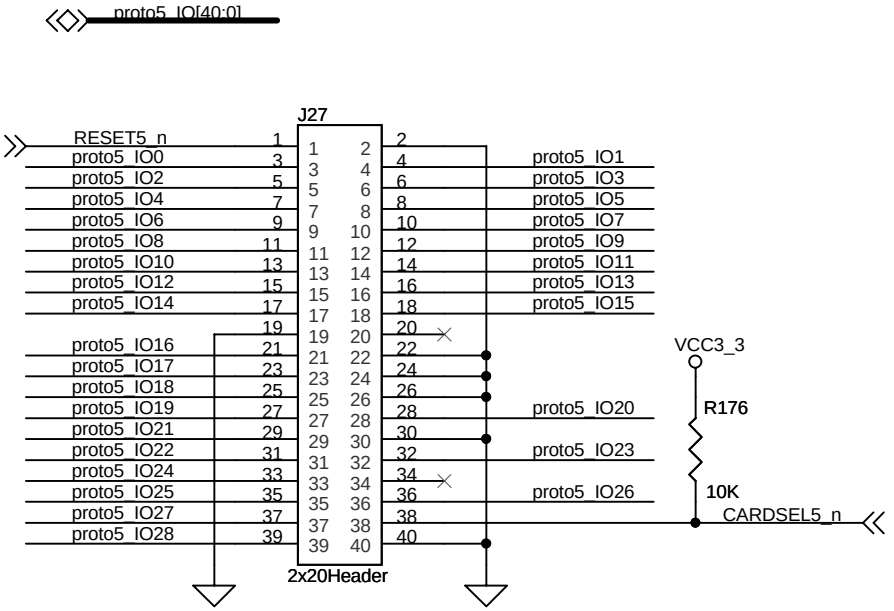

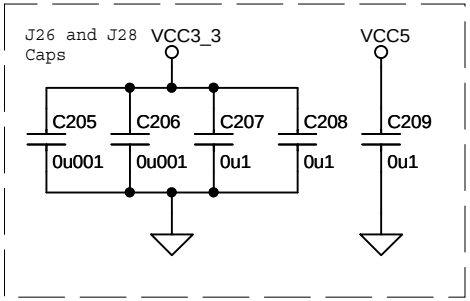

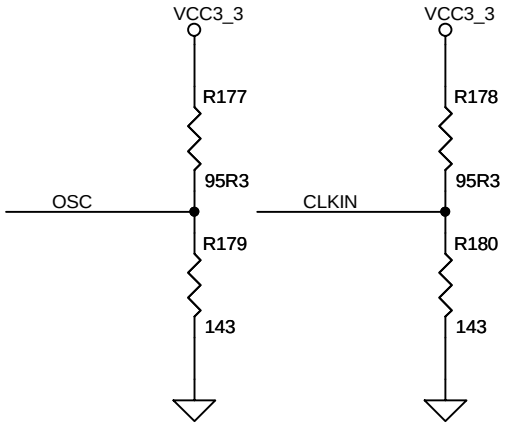

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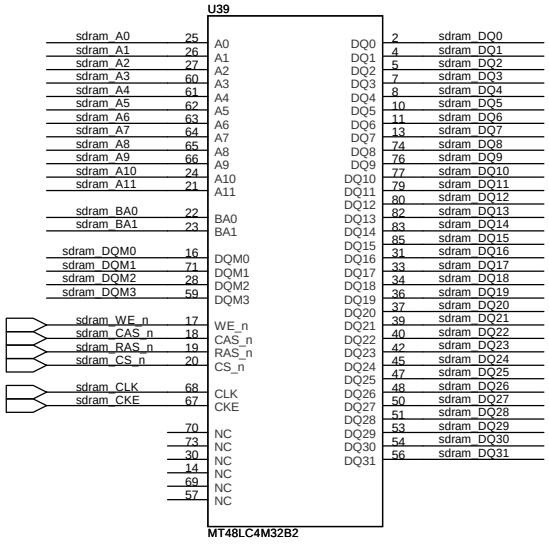

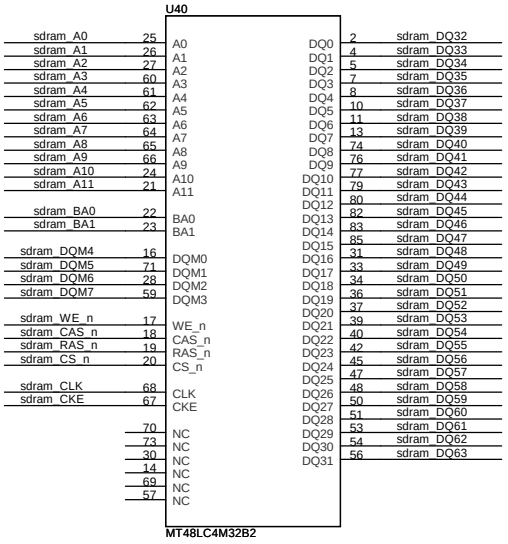

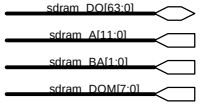

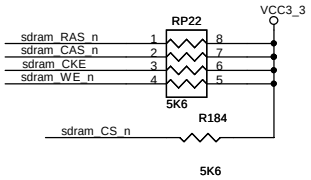

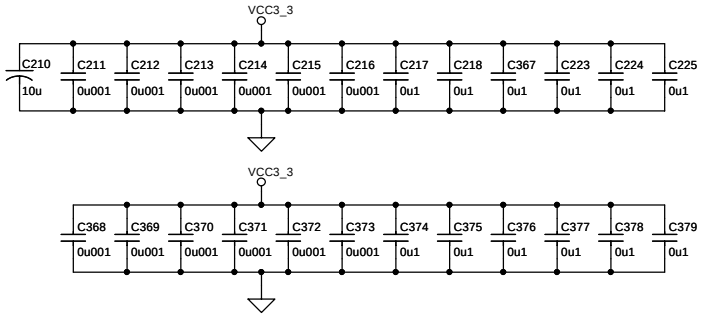

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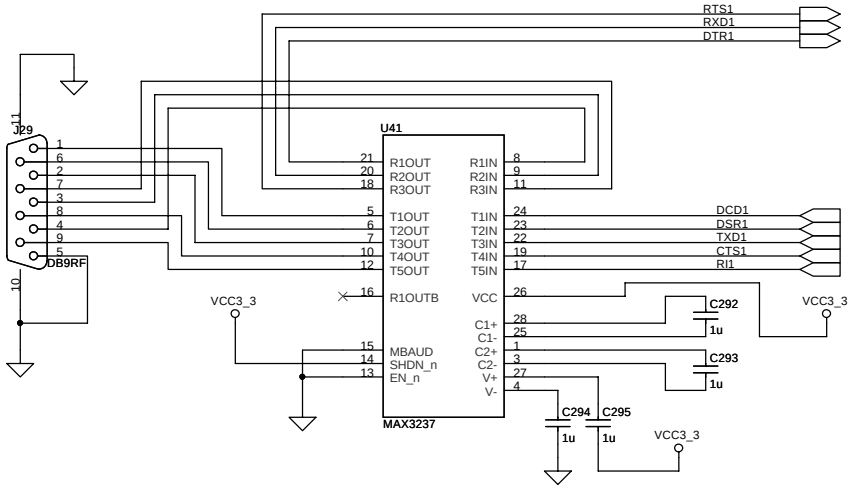
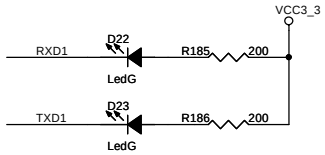
Serial Ports





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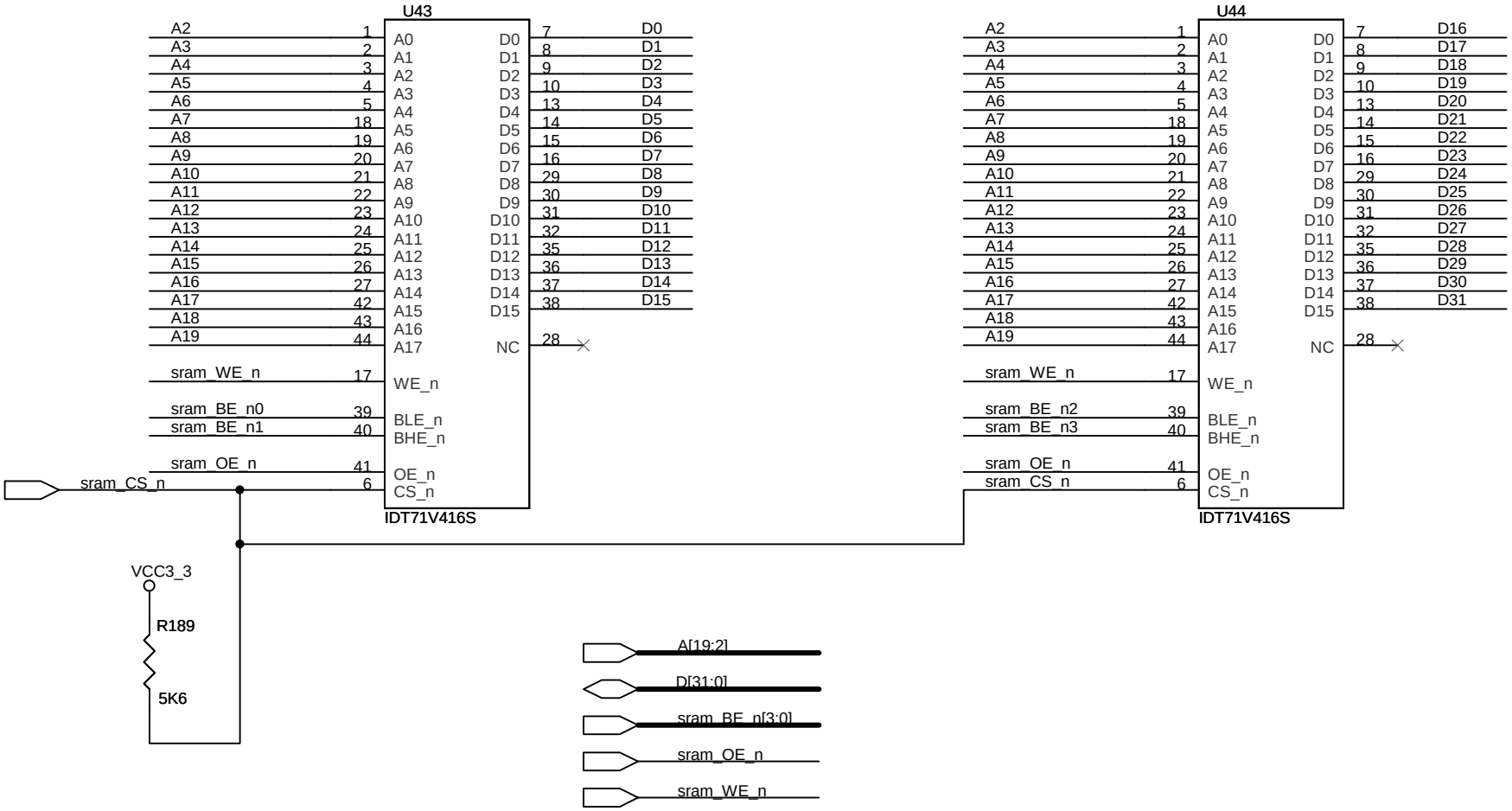
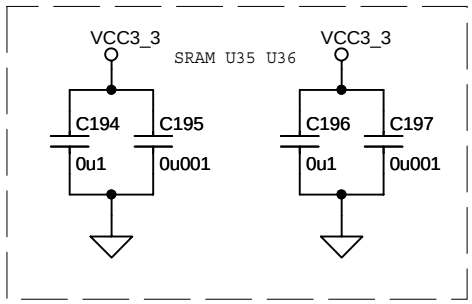
SRAM





One bank of 256K x 32 SRAM (two 256K x 16 parts in parallel) = 1Mbyte of SRAM

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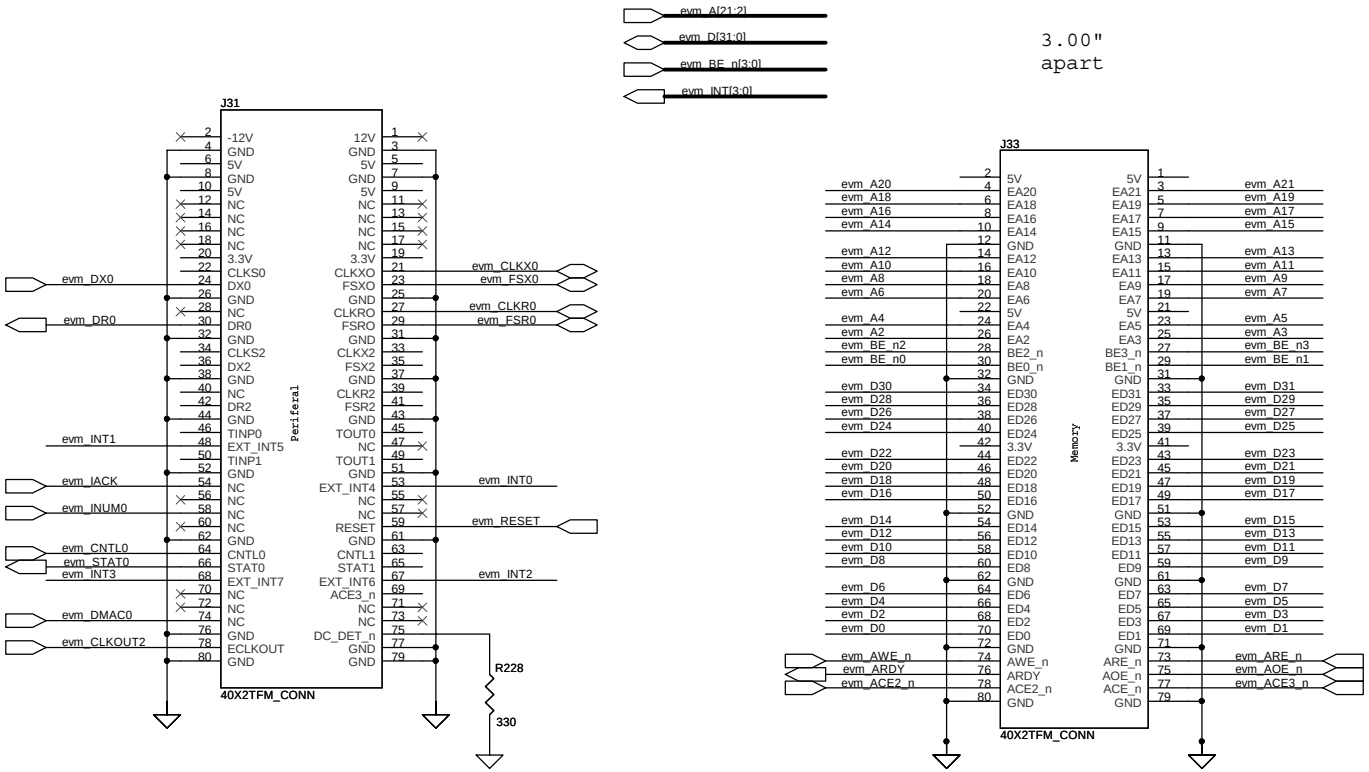
TI EVM Connector



These connectors reference the TI 6416 board

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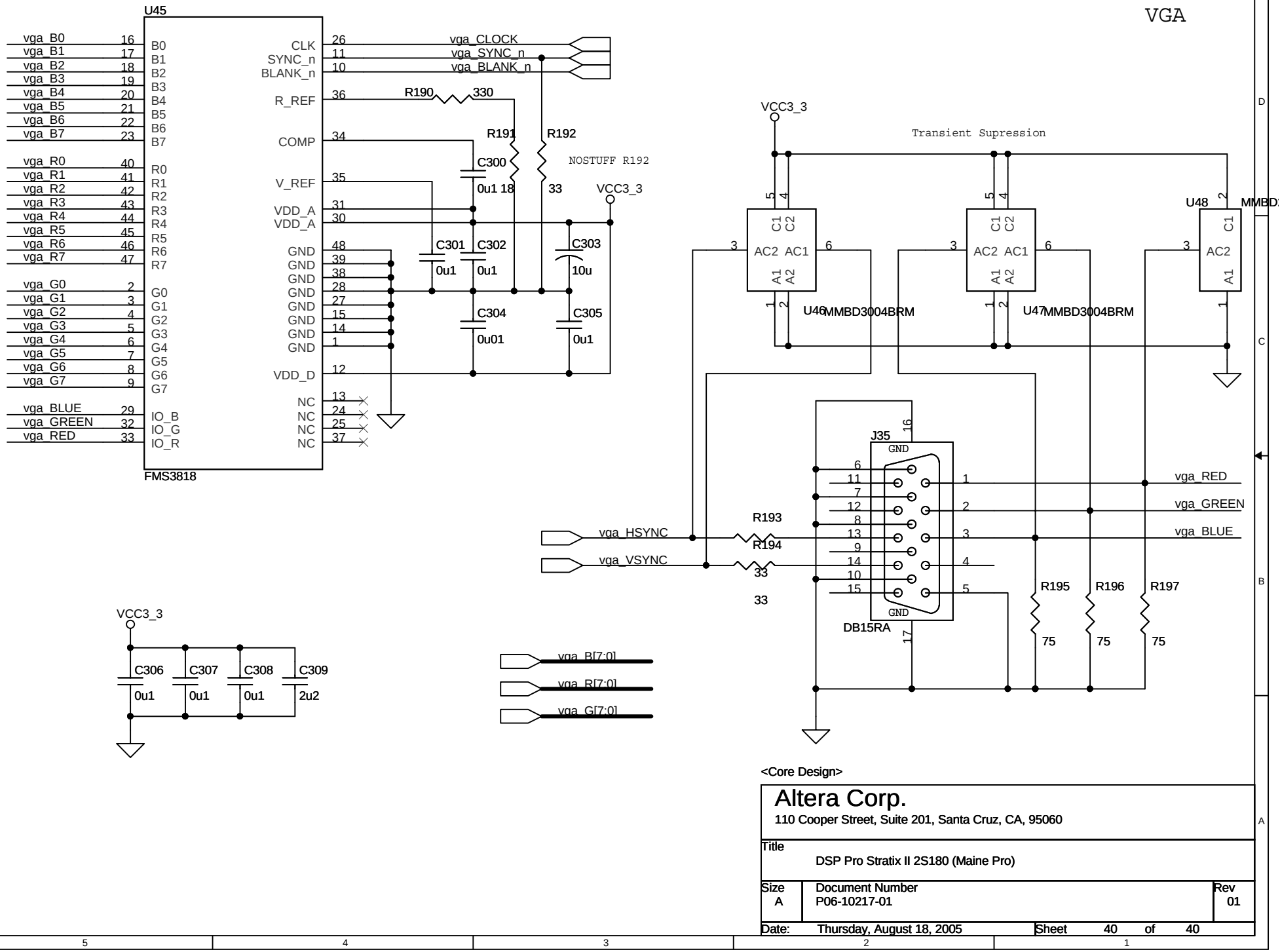
VGA
U45
FMS3818
vga_B0
vga_B1
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vga_B4
vga_B5
vga_B6
vga_B7
vga_R0
vga_R1
vga_R2
vga_R3
vga_R4
vga_R5
vga_R6
vga_R7
vga_G0
vga_G1
vga_G2
vga_G3
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vga_G7
vga_BLUE
vga_GREEN
vga_RED
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R190
330
R191
R192
NOSTUFF R192
C300
0u1
18
33
VCC3_3
C301
C302
C303
C304
C305
0u1
0u1
10u
0u01
0u1
Transient Supression
U46MMBD3004BRM
U47MMBD3004BRM
U48
MMBD
J35
DB15RA
vga_HSYNC
vga_VSYNC
R193
R194
33
33
R195
R196
R197
75
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