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April 1st, 2010
Renesas Electronics Corporation

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M62303FP

High Precision Double Integration Type A/D Converter

REJ03D0862-0201
Rev.2.01
Dec 27, 2007

Description

M62303FP is a double integration type A/D converter support system, and is a semiconductor integrated circuit which can work as A/D converter of 14 bits or more by being used with MCU and by inputting SI, SCK1, CS, and CONTIN.

High precision A/D translation system can be realized without using high precision external parts by proofreading A/D acquired values with two or more known conversion values such as reference voltage, grounding (zero) voltage and so forth.

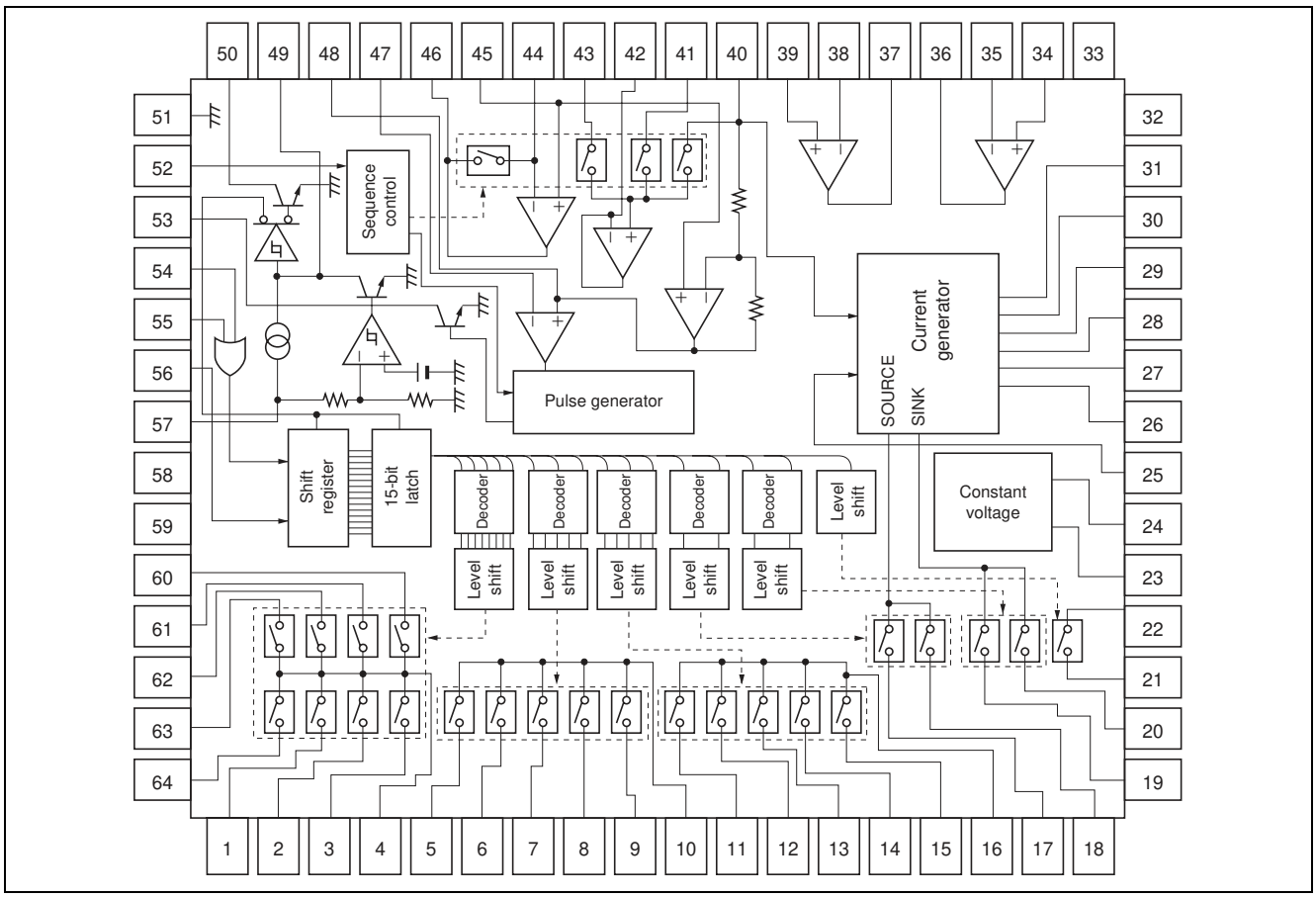
Features

- High precision (14 bits or more) double integration type A/D converter
- Positive/negative constant voltage source built-in (+6.3 V, –6.0 V Typ)
- Positive/negative constant current source built-in (Isource = 2 mA, Isink = 0.2 mA Max)
- Independent 2ch operational amplifier built-in
- System reset built-in (4.5 V Typ)

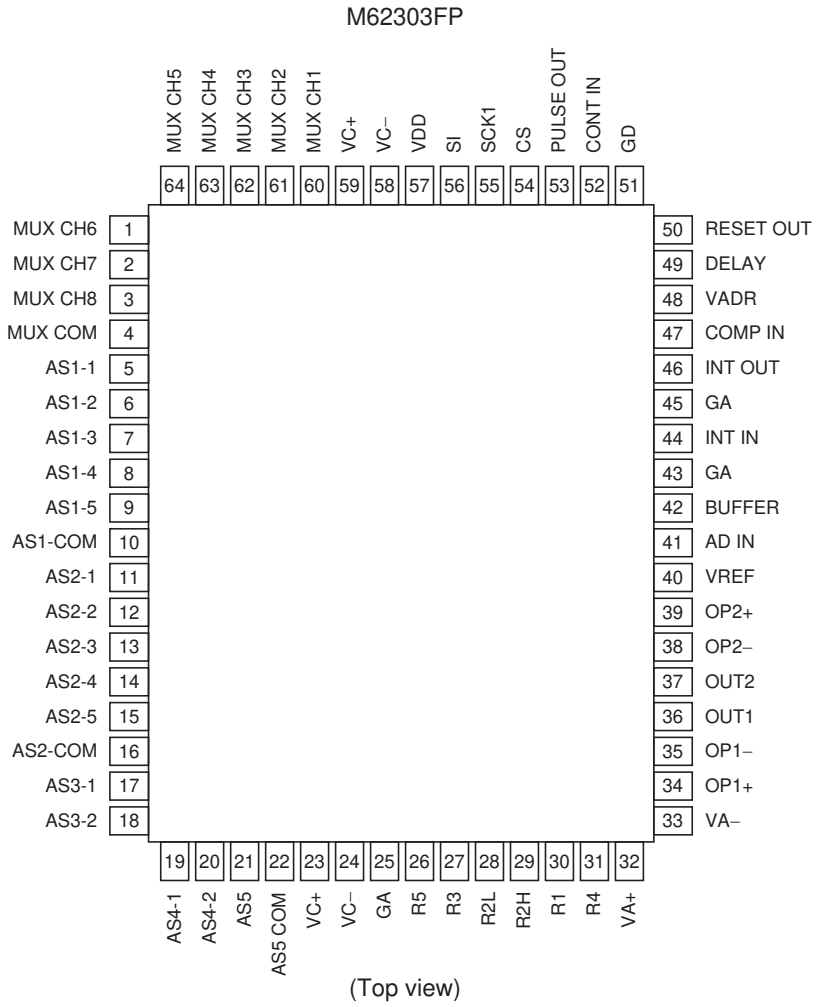
Application

High precision control systems, such as temperature control and speed control

Block Diagram



Pin Arrangement



Outline: PRQP0064JA-A (64P6S-A)

Pin Description

Pin No.	Pin Name	Function
56	SI	Serial data input terminal. Serial data of 15 bits data length is input.
55	SCK1	Shift clock input terminal. Signal from SI terminal is input into 15-bit shift register at the rise of a clock.
54	CS	"L" level of this terminal enables shift clock, and "H" level makes shift register contents stored into multiplexer control register (analog switches) and unenables clock input.
52	CONT IN	A pulse is input. Double integration type A/D converter is started synchronizing with this pulse. Moreover, the optimal full scale can be set up by setting up with C and R so that it may be set to TCONT ≤ 2.14 CR.
57	VDD	Digital part power supply terminal
51	GD	Digital part GND terminal. This terminal is externally connected to analog ground terminal when IC is operative.
50	RESET OUT	Output terminal of reset circuit supervising the fall of a digital part power supply.
49	DERAY	Reset output rise is delayed by adding capacitor.
60, 61, 62, 63, 64, 1, 2, 3	MUX1 to 8	Input side terminal of multiplexer (analog switch group) MUX.
4	MUXCOM	Output side COMMON terminal of multiplexer MUX.
5, 6, 7, 8, 9	AS1-1 to 5	Input side terminal of multiplexer (analog switch group) AS1.
10	AS1COM	Output side COMMON terminal of multiplexer AS1.
11, 12, 13, 14, 15	AS2-1 to 5	Input side terminal of multiplexer (analog switch group) AS2
16	AS2COM	Output side COMMON terminal of multiplexer AS2
17, 18	AS3-1 to 2	Source type constant current source output terminal
19, 20	AS4-1 to 2	Sink type constant current source output terminal
21	AS5	Analog switch AS5 input side terminal
22	AS5COM	Analog switch AS5 output side terminal
23, 59	VC+	Positive power supply output terminal for analog switch drive
24, 58	VC–	Negative power supply output terminal for analog switch drive
25	GA	Analog part GND terminal
26, 27, 28, 29	R5, R3, R2L, R2H	Reference current setting terminal for constant current source
30	R1	Source type output current setting terminal for constant current source
31	R4	Sink type output current setting terminal for constant current source
32	VA+	Analog part positive power supply terminal
33	VA–	Analog part negative power supply terminal
34	OP1+	Operational amplifier 1 non-inverting input terminal
35	OP1–	Operational amplifier 1 inverting input terminal
36	OUT1	Operational amplifier 1 output terminal
37	OUT2	Operational amplifier 2 output terminal
38	OP2–	Operational amplifier 2 inverting input terminal
39	OP2+	Operational amplifier 2 non-inverting input terminal
40	VREF	Standard voltage input for standard integration, and constant standard voltage input terminal for source current source setup
41	ADIN	A/D conversion input terminal. Analog signal into ADIN terminal is converted into pulse width proportional to the input voltage.
42	BUFFER	Output terminal of buffer amplifier which receives VREF, ADIN, and GA input. Internal analog switch for A/D conversion is switched by the CONTIN signal, and the voltage of three types of VREF, ADIN, and GA is output to BUFFER terminal through buffer amplifier.
43, 45	GA	Analog part GND terminal
44	INTIN	Input terminal of integration amplifier
46	INTOUT	Output terminal of integration amplifier
47	COMPIN	Input terminal of the comparator part of a double integration type A/D converter
48	VADR	Power supply output terminal used for reference terminal of comparator
53	PULSEOUT	A/D translation output terminal. Input analog signal is changed into pulse to be output.

Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Analog power supply voltage	VA+ VA–	22	V	
Switch part power supply voltage	Vc+ Vc–	13.2	V	
Digital section supply voltage	V_{DD}	–0.3 to +7	V	
A/D converter analog input voltage	V_{AIN}	–4 to +4	V	
PULSE OUT output current	Isink (PO)	10	mA	
Reset output current	Isink (RE)	10	mA	
Switch input voltage	V_{SWIN}	Vc– to Vc+	V	
		VA– to VA+ *1		At the line of fault voltage impression
Switch input current	I_{SWIN}	±20*1	mA	(Per one pin)
		±100*1		(All the switch sum totals)
Digital input voltage	V_{DIN}	–0.3 to V_{DD} + 0.3	V	
Power dissipation	Pd	740	mW	
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–40 to +125	°C	

Note: 1. Represents the protection level at the time of abnormalities.

Operating Conditions

(Ta = 25°C)

Block	Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Analog	Power supply voltage (positive side)	VA+	+8.1	+12	+13	V	
	Power supply voltage (negative side)	VA–	–9	–8	–7.2	V	
	Power supply current (positive side)	IA+	—	13	17	mA	
	Power supply current (negative side)	IA–	—	12	17	mA	
	A/D converter analog standard voltage	V_{REF}	1.0	2.5	3.0	V	
	A/D converter analog input voltage	V_{AIN}	$-V_{REF}$	—	V_{REF}	V	
	Switch input voltage	V_{SWIN}	–6	—	+6	V	
	Input integration time	T_{CONT}	2	—	20	ms	
Digital	Power supply voltage	V_{DD}	4.80*2	5.0	5.5	V	
	Power supply current	I_{DD}	—	1.8	3	mA	
	High-level input voltage	V_{IN}	2.4	—	—	V	
	Low-level input voltage	V_{IL}	—	—	0.8	V	
	Serial clock waiting time	t_{SCSK}	250	—	—	ns	CS↓→SCKI↓
	Serial input setup time	t_{SIK}	100	—	—	ns	SI→SCKI↑
	Serial input hold time	t_{HKI}	50	—	—	ns	SCKI↑→SI
	Serial clock low level time	t_{WLK}	200	—	—	ns	
	Serial clock high level time	t_{WHK}	200	—	—	ns	
	Chip selection hold time	t_{HKCS}	50	—	—	ns	SCKI↑→CS↑
External parts	Integration capacitance	C_{INT}*3	—	0.015	—	μF	
	Voltage current conversion resistor	R_{INT}	56	230	500	kΩ	

Notes: 2. Represents the reset release voltage.
3. Set up as in 2.14 R_{INT} – C_{INT} T_{CONT}.

Electrical Characteristics

(Ta = 25°C, unless otherwise noted)
VA+ = 12 V, VA– = –SV, V_{REF} = 2.5 V, V_{DD} = 5.0 V, T_{CONT} = 7.3 ms

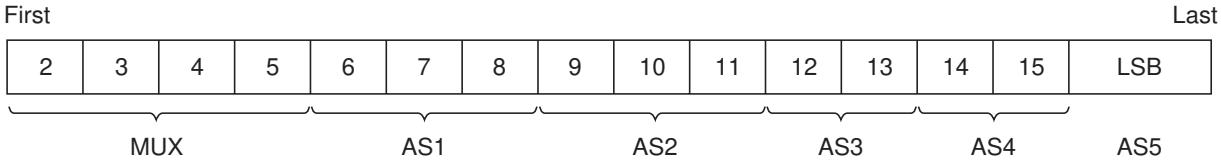
Block	Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
A/D Conversion Machine	Analog input current	I_I	—	20	80	nA		
	Resolution	ER	14	—	—	Bit		
	Linearity error*1	N, L	—	0.012	—	%FS		
	Conversion range of fluctuation*2	—	—	0.006	—	%FS		
	Conversion time	Tc	—	8.28	—	ms	C_{INT} = 0.015 µF, R_{INT} = 230 kΩ	V_{AIN} = 2.5 V
			—	15.58	—			V_{AIN} = 0 V
			—	22.88	—			V_{AIN} = –2.5 V
	Saturation voltage	Vpo (sat)	—	—	0.4	V	Isink (PO) = 6 mA	
Power Supply	Conversion standard voltage	V_{ADR}	–6.3	–6.0	–5.7	V		
	Output voltage for switch part power supplies	Vc+	+6.0	+6.3	+6.6	V		
	Output voltage for switch part power supplies	Vc–	–6.6	–6.3	–6.6	V		
	Input voltage fluctuation	ΔVc	—	—	100	mV	VA+: 8.1 to 13 V, VA–: –9 to –7.2 V	
Switch Part	ON resistance	R_{ON}	—	100	200	Ω	–6 V Vds 6 V, Id = 1 mA	Ta = 25°C
			—	—	200			Ta = –40°C
			—	—	300			Ta = 85°C
	RON match		—	10	30	%		
	RON drift	$\Delta R_{ON}/\Delta T$	—	0.5	—	%/°C		
	Input off-leak current	I_{Soff}	—	±0.1	±100	nA	Vd = –6 V, Vs = 6 V and Vs = –6 V, Vd = 6 V	Ta = 25°C
			—	—	±100			Ta = 0°C
			—	—	±100			Ta = 50°C
	Output off-leak current	I_{Doff}	—	±0.1	±100	nA	Vd = –6 V, Vs = 6 V and Vs = –6 V, Vd = 6 V	Ta = 25°C
			—	—	±100			Ta = 0°C
			—	—	±100			Ta = 50°C
	On-channel leak current	I_{Don}	—	±0.1	±100	nA	Vs = Vd = 6 V and Vs = Vd = –6 V	Ta = 25°C
			—	—	±100			Ta = 0°C
			—	—	±100			Ta = 50°C
	Off isolation	OIRR	70	80	—	dB	Vs = 2 Vp-p, f = 1 kHz, R_L = 100 Ω	
	Cross talk	CCRR	70	90	—	dB	Vs = 2 Vp-p, f = 1 kHz, R_L = 100 Ω	

Notes: 1. $-V_{REF}$ to 0 and 0 to V_{REF} is made into full scale.
2. Tolerance width at the time of repeated conversion.

Electrical Characteristics (cont.)

Block	Item	Symbol	Min	Typ	Max	Unit	Test Conditions
The Source of Current	Output source current	I_{CS1}	0.1	—	2	mA	RL1 = 0 to 3000 Ω
	Output source current accuracy	ΔI_{CS1}	—	—	±0.2	%	RL1 = 0 to 3000 Ω
	Output source current drift		—	±10	—	ppM/°C	
	Permissible load resistance	RL1	—	—	3000	Ω	With the sauce current maximum
	Output sink current	I_{CS2}	—	—	–0.2	mA	RL2 = 0 to 1000 Ω
	Output sink current accuracy	ΔI_{CS2}	—	—	±0.2	%	RL2 = 0 to 1000 Ω
	Output sink current drift		—	±10	—	ppM/°C	
	Permissible load resistance	RL2	—	—	1000	Ω	With the sink current maximum
Reset	Reset detection voltage	Vs	4.3	4.5	4.7	V	
	Hysteresis (upper side)	Vhys	40	70	100	mV	
	Delay time	t_D	0.6	1	1.5	ms	C_{DELAY} = 0.01 μF
	Saturation voltage	VR (sat)	—	—	0.4	V	Isink = 6 mA
Operational Amplifier	Input offset voltage	VI_O	—	1.0	6.0	mV	Rs = 10 kΩ
	Input offset voltage drift	$\Delta Vm/\Delta T$	—	3	—	μV/°C	Rs = 10 kΩ
	Input offset current	II_O	—	20	200	nA	
	Input offset current drift	$\Delta Im/\Delta T$	—	1	—	nA/°C	
	Input bias current	I_B	—	80	500	nA	
	Input bias current drift	$\Delta I_B/\Delta T$	—	2	—	nA/°C	
	Open loop gain	AV	20000	100000	—	Ω	R_L = 2 kΩ, V_O = +8 V, –4 V
	Open loop gain rejection ratio	CMR	70	90	—	dB	Rs = 10 kΩ
	Power supply change rejection ratio	SVR	—	30	150	μV/V	Rs = 10 kΩ
	Maximum output voltage	Vom	+9, –5	+11, –7	—	V	R_L = 10 kΩ
	Slew rate	S. R.	0.4	0.8	—	V/μs	AV = 1
	Maximum output current	Iop	5	10	—	mA	

Digital Format



1. Multiplexer (MUX)

	5th	4th	3rd	2nd
ALL OFF	0	0	0	0
CH1 ON	1	0	0	0
CH2 ON	0	1	0	0
CH3 ON	1	1	0	0
CH4 ON	0	0	1	0
CH5 ON	1	0	1	0
CH6 ON	0	1	1	0
CH7 ON	1	1	1	0
CH8 ON	0	0	0	1
ALL OFF	1	0	0	1
ALL OFF	0	1	0	1
ALL OFF	1	1	0	1
ALL OFF	0	0	1	1
ALL OFF	1	0	1	1
ALL OFF	0	1	1	1
ALL OFF	1	1	1	1

2. Analog switch 1 (AS1)

	8th	7th	6th
ALL OFF	0	0	0
AS1-1ON	1	0	0
1-2ON	0	1	0
1-3ON	1	1	0
1-4ON	0	0	1
1-5ON	1	0	1
ALL OFF	0	1	1
ALL OFF	1	1	1

3. Analog switch 2 (AS2)

	11th	10th	9th
ALL OFF	0	0	0
AS2-1ON	1	0	0
2-2ON	0	1	0
2-3ON	1	1	0
2-4ON	0	0	1
2-5ON	1	0	1
ALL OFF	0	1	1
ALL OFF	1	1	1

4. Analog switch 3 (AS3)

	13th	12th
ALL OFF	0	0
AS3-1ON	1	0
3-2ON	0	1
ALL OFF	1	1

5. Analog switch 4 (AS4)

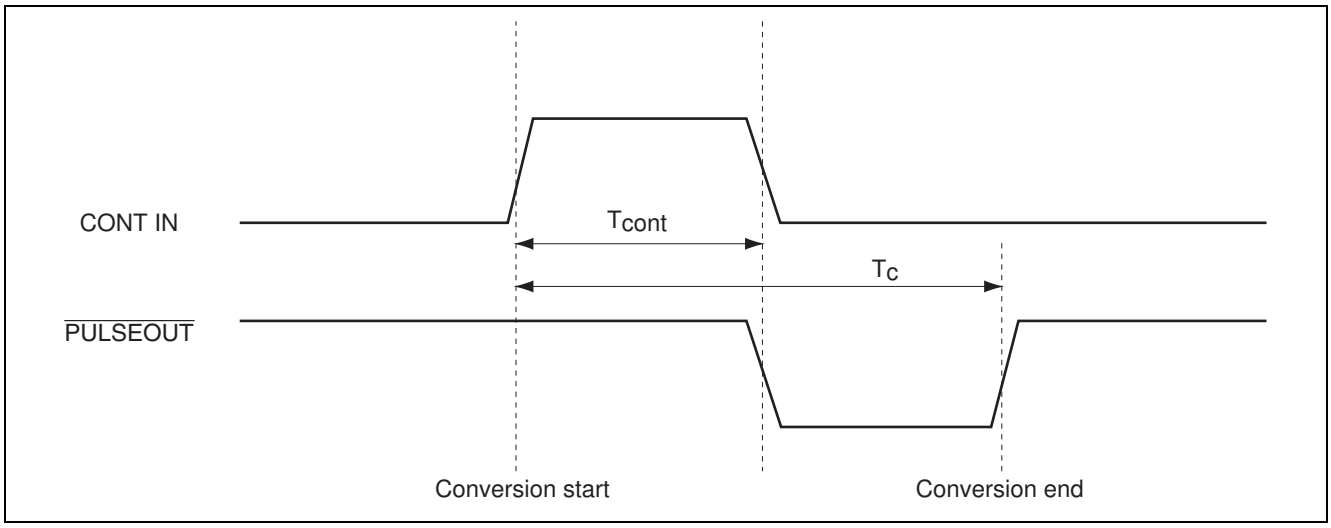
	15th	14th
ALL OFF	0	0
AS4-1ON	1	0
4-2ON	0	1
ALL OFF	1	1

6. Analog switch 5 (AS5)

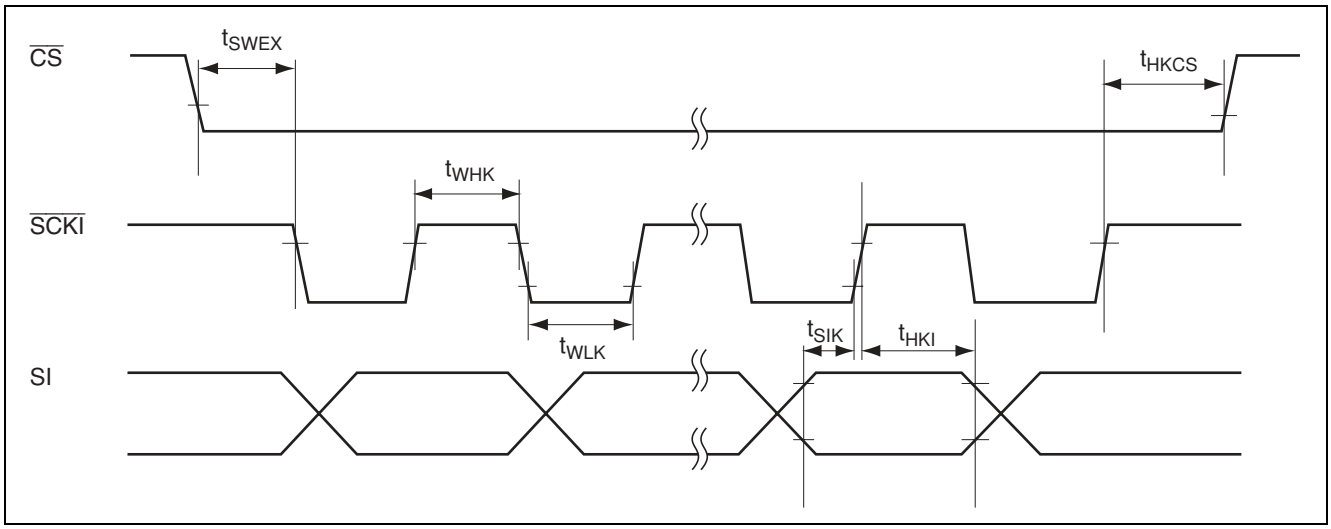
	LSB
OFF	0
AS5ON	1

Sequence Timing Chart

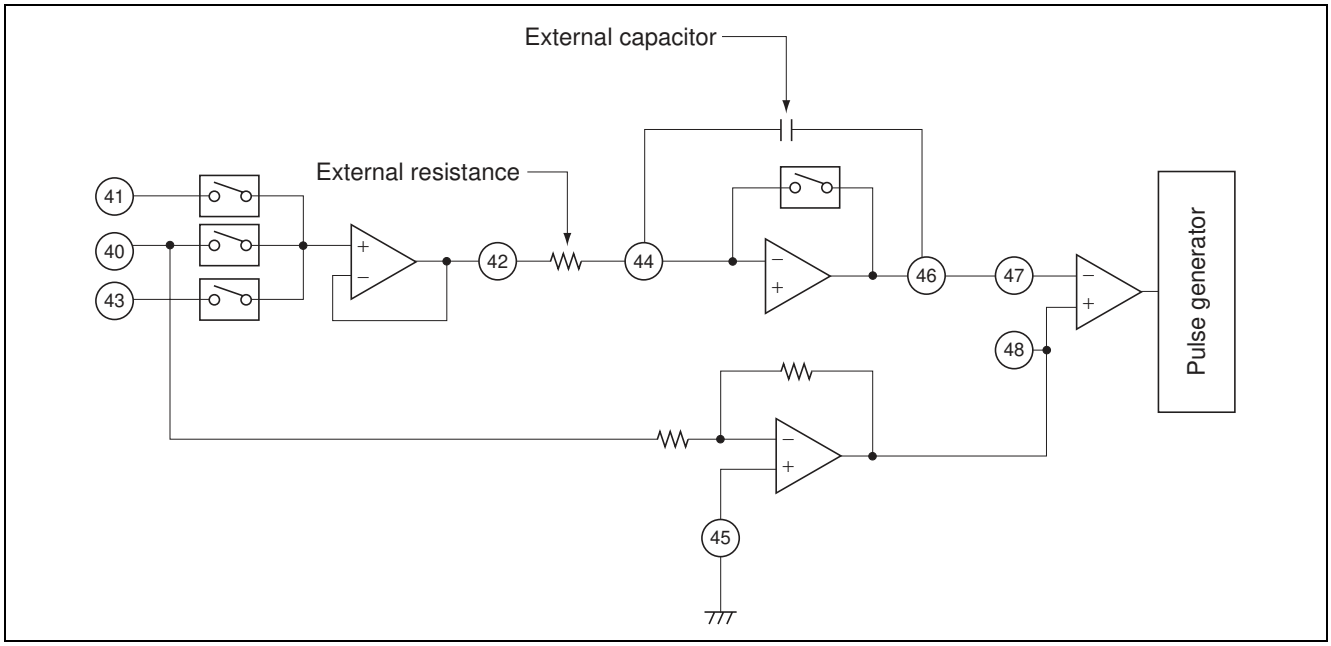
(1) A/D conversion



(2) DATA Input



About the Input Voltage VX



Given the applied voltage into 41 pin is VX in the diagram above,

$$VX = \frac{TGND - TX}{TGND - TR} \bullet VR \qquad T = \text{Pulse width}$$

TGND, TR, and TX can be respectively expressed with nGND/f, nR/f, and nX/f, (f is clock frequency; nGND, nR, nX is count values for clock frequency f.)

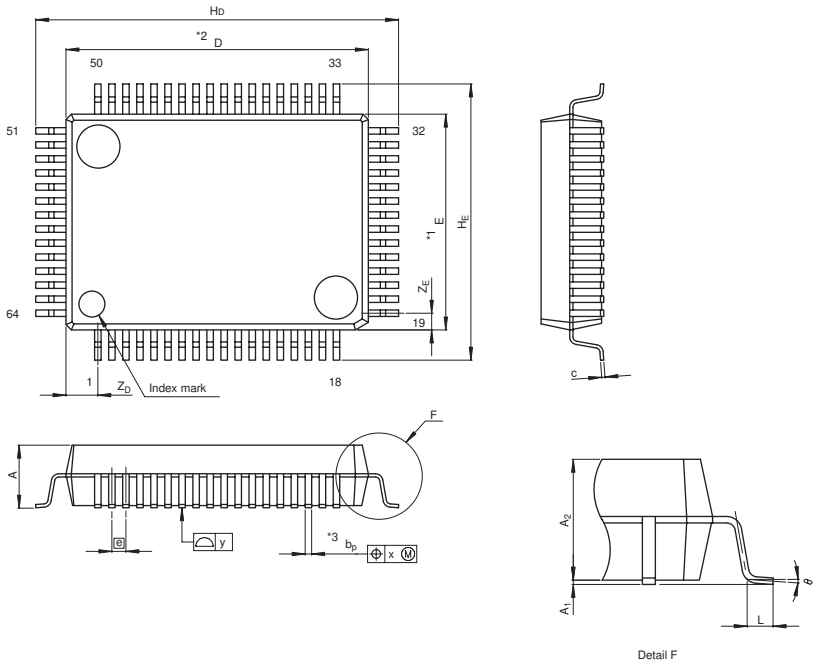
If these are substituted for an upper formula,

$$VX = \frac{nGND - nX}{nGND - nR} \bullet VR$$

VX can be expressed in this way for the number of counters.

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP64-10x14-0.65	PRQP0064JA-A	64P6S-A	0.8g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.8	14.0	14.2
E	9.8	10.0	10.2
A_2	—	2.8	—
H_D	16.5	16.8	17.1
H_E	12.5	12.8	13.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.475	—
Z_E	—	0.775	—
L	0.4	0.6	0.8

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