HA-2842

80MHz, High Slew Rate, High Output Current, Video Operational Amplifier

November 1996

Features

- Stable at Gains of 2 or Greater
- Low AC Variability Over Process and Temperature
- Gain Bandwidth 80MHz
- Gain Flatness to 10MHz. 0.035dB
- High Slew Rate. 400V/µs
- High Output Current (Min). 100mA
- Differential Gain/Phase . . . . 0.02%/0.03 Degrees
- Low Supply Current (Max) 15mA
- Enhanced Replacement for AD842

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- Coaxial Cable Drivers
- Fast Sample-Hold Circuits
- High Frequency Signal Conditioning Circuits

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA3B2842-5	0 to 75	14 Ld PDIP	E14.3
HA3-2842-5	0 to 75	8 Ld PDIP	E8.3
HA9P2842-5 (H2842F5)	0 to 75	8 Ld SOIC	M8.15
HA3-2842C-5	0 to 75	8 Ld PDIP	E8.3
HA9P2842C-5 (H2842C5)	0 to 75	8 Ld SOIC	M8.15
HA3B2842-9	-40 to 85	14 Ld PDIP	E14.3
HA3-2842-9	-40 to 85	8 Ld PDIP	E8.3

Description

The HA-2842 is a wideband, high slew rate, operational amplifier featuring an outstanding combination of speed, bandwidth, and output drive capability. This amplifier's performance is further enhanced through stable operation down to closed loop gains of +2, the inclusion of offset null controls, and by its excellent video performance.

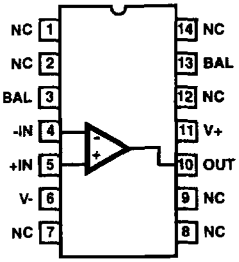
The capabilities of the HA-2842 are ideally suited for high speed cable driver circuits, where low closed loop gains and high output drive are required. With a 6MHz full power bandwidth, this amplifier is well suited for high frequency signal conditioning circuits and video amplifiers. Gain flatness of 0.035dB, combined with differential gain and phase specifications of 0.02%, and 0.03 degrees, respectively, make the HA-2842 ideal for component and composite video applications.

A zener/nichrome based reference circuit, coupled with advanced laser trimming techniques, yields a supply current with a low temperature coefficient and low lot-to-lot variability. For example, the average I_{CC} variation from 85°C to -40°C is <600µA (±2%), while the standard deviation of the I_{CC} distribution is <0.1mA (0.8%) at 25°C. Tighter I_{CC} control translates to more consistent AC parameters ensuring that units from each lot perform the same way, and easing the task of designing systems for wide temperature ranges. Critical AC parameters, Slew Rate and Bandwidth, each vary by less than ±5% over the industrial temperature range (see Typical Performance Curves).

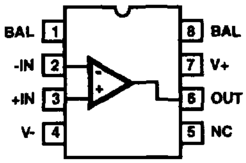
The HA-2842C is the same amplifier with a compensation pin available to the user. By connecting a capacitor from pin 8 to GND, the HA-2842C can be compensated for unity gain operation, or the bandwidth can be limited to reduce total noise.

Pinouts

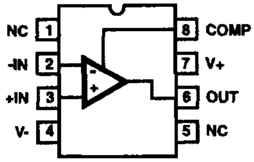
HA-2842 (PDIP) TOP VIEW



HA-2842 (PDIP, SOIC) TOP VIEW



HA-2842C (PDIP, SOIC) TOP VIEW



NOTE: No Connection (NC) pins may be tied to a ground plane for better isolation and heat dissipation.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage. 6V
Output Current (Notes 3, 4) 125mA
100mA (50% Duty Cycle)

Operating Conditions

Temperature Range
HA-2842-5. . . . . .0°C to 75°C
HA-2842-9. . . . . -40°C to 85°C
Recommended Supply Voltage Range. . . . . ±6.5V to ±15V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
14 Lead PDIP Package	89
8 Lead PDIP Package	92
8 Lead SOIC Package	157

Maximum Junction Temperature (Die). .175°C
Maximum Junction Temperature (Plastic Package, Note 1) . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below 150°C for plastic packages. By using Application Note AN556 on Safe Operating Area equations, along with the packaging thermal resistances listed in the Operating Conditions section, proper load conditions can be determined.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. V_O = ±5V, R_L Unconnected, Duty cycle ≤ 50%. For information about using high output current amplifiers, please refer to Application Note AN556 (Thermal Safe-Operating-Areas For High Current Op Amps), and the "Power Dissipation Considerations" section in the "Application Information" section of this datasheet.
4. Maximum continuous (100% Duty Cycle) output current is 50mA. For currents >50mA, Duty Cycle must be derated accordingly.

Electrical Specifications

V_{SUPPLY} = ±15V, R_L = 1kΩ, C_L ≤ 10pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-2842-5, -9 MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Offset Voltage (Note 10)		25	-	1	3	mV
		Full	-	-	6	mV
Average Offset Voltage Drift		Full	-	13	-	μV/°C
Bias Current (Note 10)		25	-	5	10	μA
		Full	-	-	15	μA
Average Bias Current Drift		Full	-	20	-	nA/°C
Offset Current		25	-	0.5	1.0	μA
		Full	-	-	1.5	μA
Average Offset Current Drift		Full	-	1.3	-	nA/°C
Input Resistance		25	-	170	-	kΩ
Input Capacitance		25	-	1	-	pF
Common Mode Range		Full	±10	-	-	V
Input Noise Voltage	10Hz to 1MHz	25	-	16	-	μV_{RMS}
Input Noise Voltage Density	f = 1kHz, R_{SOURCE} = 0Ω	25	-	16	-	$nV/\sqrt{Hz}$
Input Noise Current (Note 10)	f = 1kHz, R_{SOURCE} = 100kΩ	25	-	2	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	V_O = ±10V	25	50	100	-	kV/V
		Full	30	60	-	kV/V
Common-Mode Rejection Ratio (Note 10)	V_{CM} = ±10V	Full	80	110	-	dB
Minimum Stable Gain		25	2	-	-	V/V
Gain Bandwidth Product (Note 10)	A_{VCL} = 100	25	-	80	-	MHz
Gain Flatness to 10MHz (Note 10)	R_L ≥ 75Ω	25	-	±0.035	-	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note, 10)	V_O = ±10V	Full	±10	±11	-	V
Output Current (Note 10)	Note 3	Full	100	-	-	mA

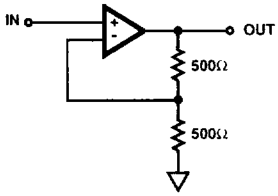
Electrical Specifications V_{SUPPLY} = ±15V, R_L = 1kΩ, C_L ≤ 10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-2842-5, -9			UNITS
			MIN	TYP	MAX	
Output Resistance		25	-	8.5	-	Ω
Full Power Bandwidth (Note 6)	V_O = ±10V	25	5.2	6	-	MHz
Differential Gain (Note 10)	Note 5	25	-	0.02	-	%
Differential Phase (Note 10)	Note 5	25	-	0.03	-	Degrees
Harmonic Distortion (Note 10)	V_O = 2V_{P-P}, f = 1MHz, A_V = 2	25	-	>81	-	dBc
TRANSIENT RESPONSE (Note 7)						
Rise Time		25	-	4	-	ns
Overshoot		25	-	25	-	%
Slew Rate (Notes 9, 10)	A_V = +2	25	325	400	-	V/µs
Settling Time	10V Step to 0.1%	25	-	100	-	ns
POWER REQUIREMENTS						
Supply Current (Note 10)		25	-	14.2	-	mA
		Full	-	14.3	15	mA
Power Supply Rejection Ratio (Note 10)	Note 8	Full	70	80	-	dB

NOTES:

5. Differential gain and phase are measured with a VM700A video tester, using a NTC-7 composite VITS. R_F = R_1 = 1kΩ, R_L = 700Ω.
6. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$, V_{PEAK} = 10V.
7. Refer to Test Circuits section of this data sheet.
8. V_{SUPPLY} = ±10V to ±20V.
9. This parameter is not tested. The limits are guaranteed based on lab characterization and reflect lot-to-lot variation.
10. See "Typical Performance Curves" for more information.

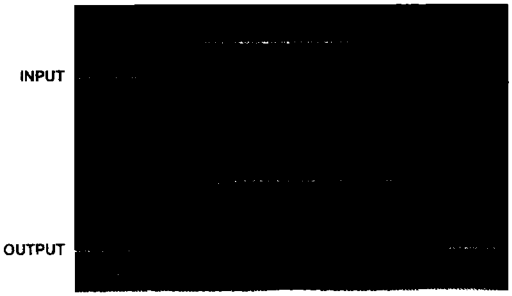
Test Circuits and Waveforms



NOTES:

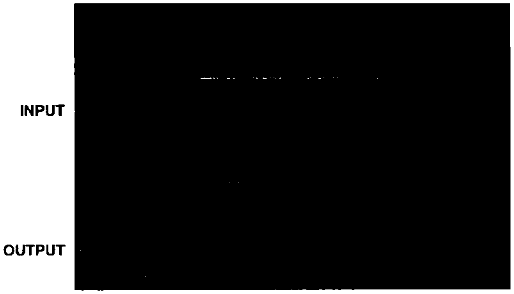
11. V_S = ±15V.
12. A_V = +2.
13. C_L ≤10pF

TEST CIRCUIT



Input = 5V/Div., Output = 5V/Div., 50ns/Div.

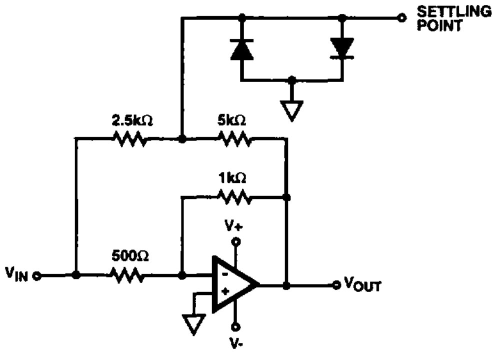
LARGE SIGNAL RESPONSE



Input = 100mV/Div., Output = 100mV/Div., 50ns/Div.

SMALL SIGNAL RESPONSE

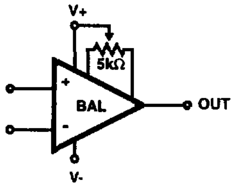
Test Circuits and Waveforms (Continued)



SETTLING TIME TEST CIRCUIT

NOTES:

14. A_V = -2.
15. Feedback and summing resistors must be matched (0.1%).
16. HP5082-2810 clipping diodes recommended.
17. Tektronix P6201 FET probe used at settling point.
18. For 0.01% settling time, heat sinking is suggested to reduce thermal effects and an analog ground plane with supply decoupling is suggested to minimize ground loop errors.



SUGESTED OFFSET VOLTAGE ADJUSTMENT

Application Information

The Harris HA-2842 is a state of the art monolithic device which also approaches the "ALL-IN-ONE" amplifier concept. This device features an outstanding set of AC parameters augmented by excellent output drive capability providing for suitable application in both high speed and high output drive circuits.

Primarily intended to be used in balanced 50Ω and 75Ω coaxial cable systems as a driver, the HA-2842 could also be used as a power booster in audio systems as well as a power amp in power supply circuits. This device would also be suitable as a small DC motor driver.

Prototyping Guidelines

For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include:

1. Mounting the device through a ground plane.
2. Connecting unused pins (NC) to the ground plane.
3. Mounting feedback components on Teflon standoffs and/or locating these components as close to the device as possible.
4. Placing power supply decoupling capacitors from device supply pins to ground.

Power Dissipation Considerations

At high output currents, especially with the 8 lead SOIC package, care must be taken to ensure that the Maximum Junction Temperature (T_J, see "Absolute Maximum Ratings" table) isn't exceeded. As an example consider the HA-2842 in the SOIC package, with a required output current of 50mA at V_{OUT} = 10V with ±15V supplies. The power dissipation is the quiescent power (450mW = 30V x 15mA) plus the power dissipated in the output stage (P_{OUT} = 250mW = 50mA x (15V - 10V)), or a total of 700mW. The thermal resistance (θ_{JA}) of the SOIC package is 157°C/W, which increases the junction temperature by 110°C over the ambient temperature (T_A). Remaining below T_{JMAX} requires that T_A be restricted to ≤ 40°C (150°C - 110°C). Heatsinking would be required for operation at ambient temperatures greater than 40°C.

Note that the problem isn't as severe with either of the PDIP packages due to their lower thermal resistances, however it is recommended that the above analysis be performed for any package if operating outside the conditions listed below:

MAX P_{OUT} WITHOUT HEATSINK (V_S = ±15V)

T_A	14 LEAD PDIP (θ_{JA} = 89°C/W)	8 LEAD PDIP (θ_{JA} = 92°C/W)	8 LEAD SOIC (θ_{JA} = 157°C/W)
85°C	280mW	260mW	Heatsink Required
70°C	450mW	420mW	60mW
25°C	950mW	910mW	350mW

Allowable output power can be increased by decreasing the quiescent dissipation via lower supply voltages.

For more information please refer to Application Note AN556, Thermal Safe Operating Areas for High Current Op Amps.

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified

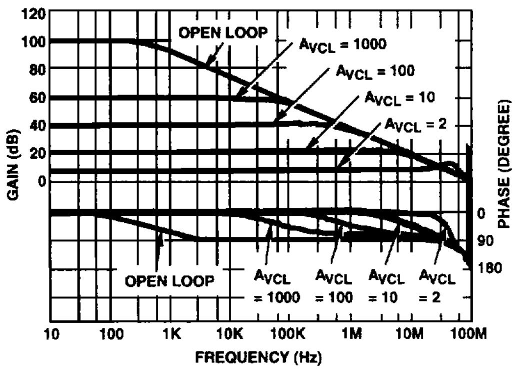


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS GAINS

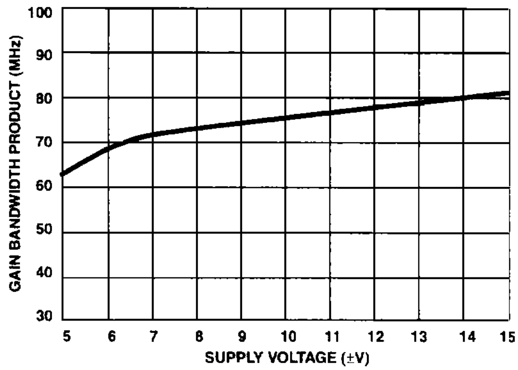


FIGURE 2. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

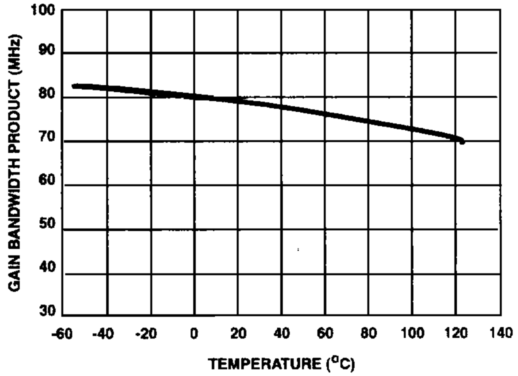


FIGURE 3. GAIN BANDWIDTH PRODUCT vs TEMPERATURE

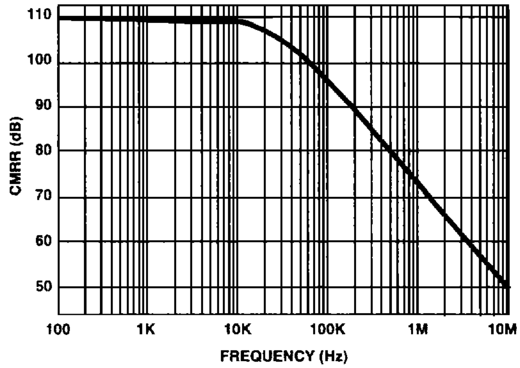


FIGURE 4. CMRR vs FREQUENCY

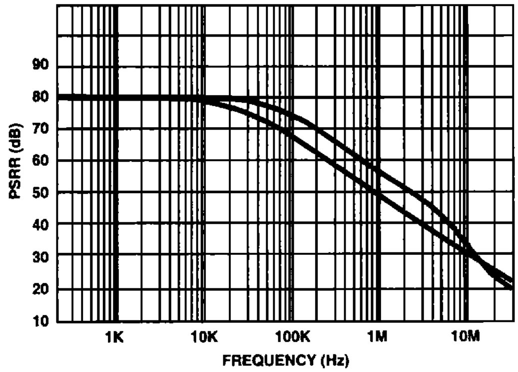


FIGURE 5. PSRR vs FREQUENCY

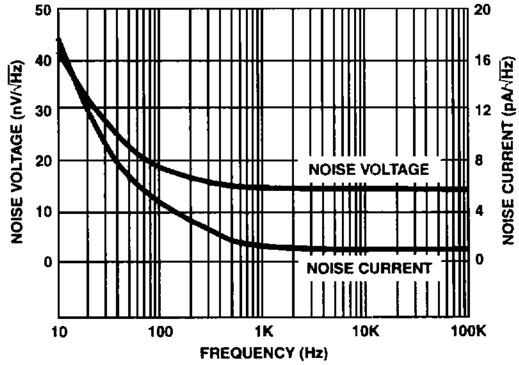


FIGURE 6. INPUT NOISE vs FREQUENCY

3

OPERATIONAL AMPLIFIERS

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified **(Continued)**

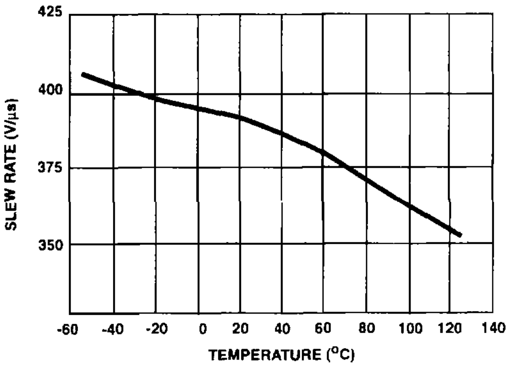


FIGURE 7. SLEW RATE vs TEMPERATURE

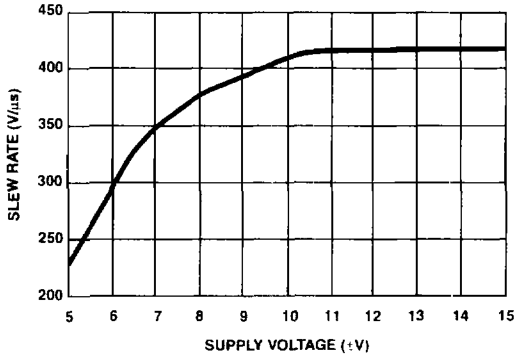


FIGURE 8. SLEW RATE vs SUPPLY VOLTAGE

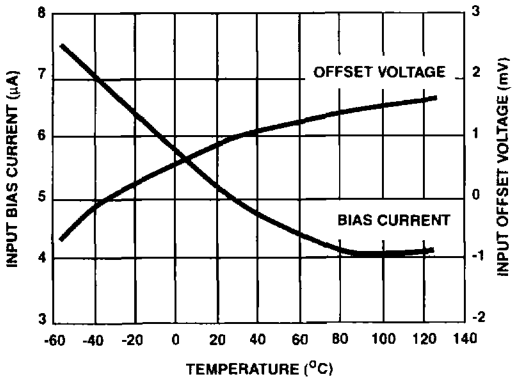


FIGURE 9. INPUT OFFSET VOLTAGE AND INPUT BIAS CURRENT vs TEMPERATURE

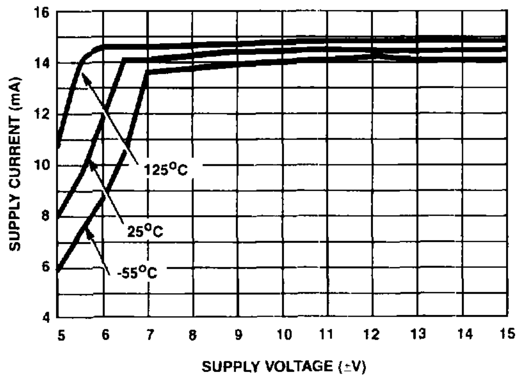


FIGURE 10. SUPPLY CURRENT vs SUPPLY VOLTAGE

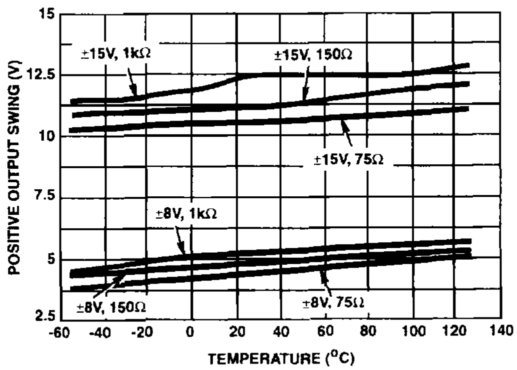


FIGURE 11. POSITIVE OUTPUT SWING vs TEMPERATURE

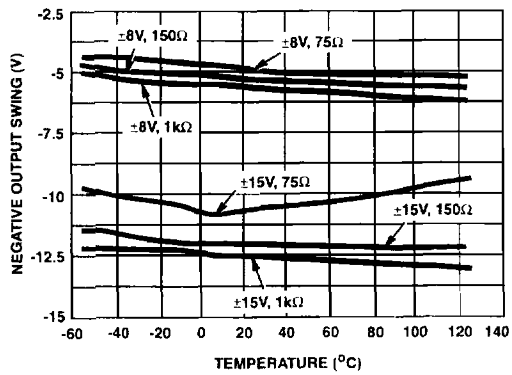


FIGURE 12. NEGATIVE OUTPUT SWING vs TEMPERATURE

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified **(Continued)**

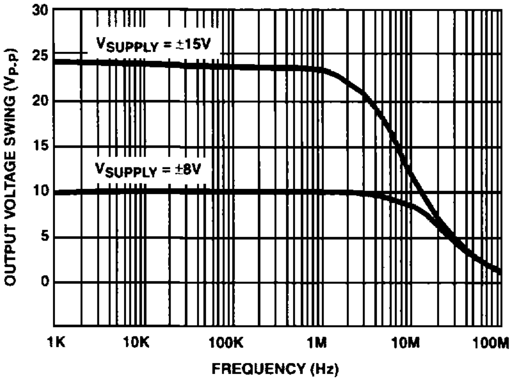


FIGURE 13. MAXIMUM UNDISTORTED OUTPUT SWING vs FREQUENCY

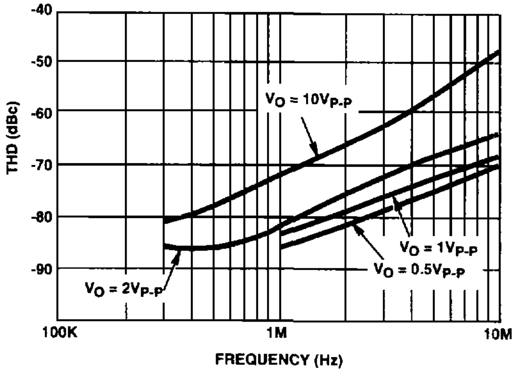


FIGURE 14. TOTAL HARMONIC DISTORTION vs FREQUENCY

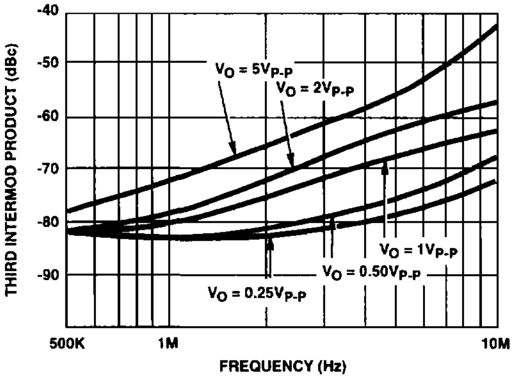


FIGURE 15. INTERMODULATION DISTORTION vs FREQUENCY (TWO TONE)

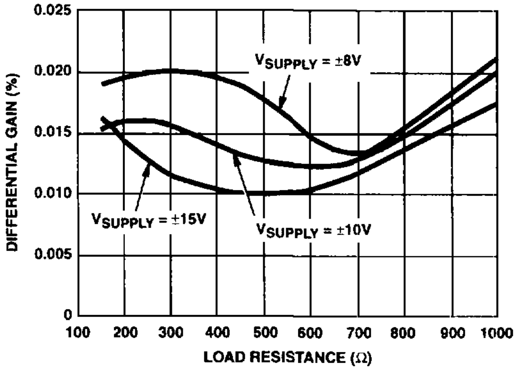


FIGURE 16. DIFFERENTIAL GAIN vs LOAD RESISTANCE

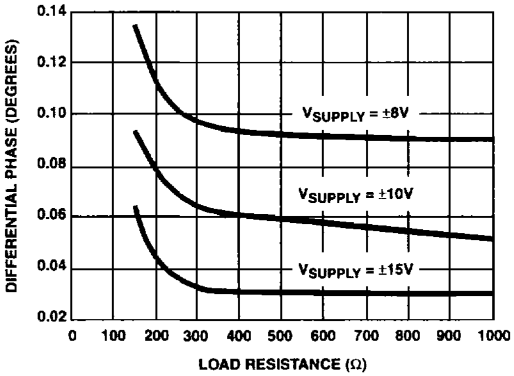


FIGURE 17. DIFFERENTIAL PHASE vs LOAD RESISTANCE

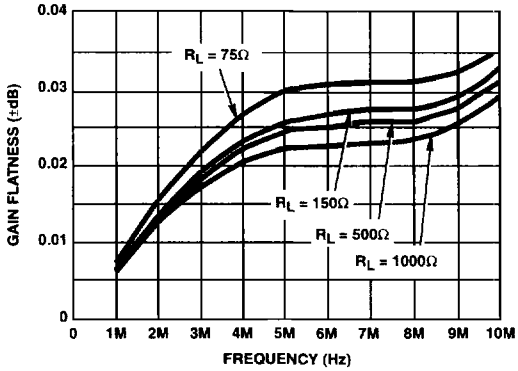


FIGURE 18. GAIN FLATNESS vs FREQUENCY ($A_{VCL} = 2$)

Typical Performance Curves $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L < 10pF$, Unless Otherwise Specified **(Continued)**

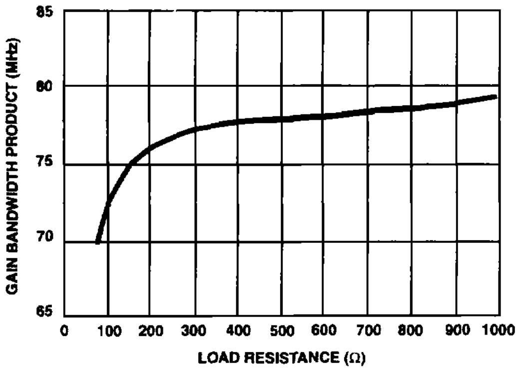


FIGURE 19. GAIN BANDWIDTH PRODUCT vs LOAD RESISTANCE

Metallization Topology

DIE DIMENSIONS:

77 mils x 81 mils x 19 mils
1960µm x 2060µm x 483µm

METALLIZATION:

Type: Aluminum, 1% Copper
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride over Silox
Silox Thickness: 12kÅ ±2kÅ
Nitride thickness: 3.5kÅ ±1kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

58

PROCESS:

High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2842