MAX9951/MAX9952

Dual Per-Pin Parametric Measurement Units

General Description

The MAX9951/MAX9952 dual parametric measurement units (PMUs) feature a small package size, wide force and measurement range, and high accuracy, making the devices ideal for automatic test equipment (ATE) and other instrumentation that requires a PMU per pin or per site.

The MAX9951/MAX9952 force or measure voltages in the -2V to +7V through -7V to +13V ranges, dependent upon the supply voltage (V_{CC} and V_{EE}). The devices handle supply voltages of up to +30V (V_{CC} to V_{EE}) and a 20V device-under-test (DUT) voltage swing at full current. The MAX9951/MAX9952 also force or measure currents up to ±64mA with a lowest full-scale range of ±2µA. Integrated support circuitry facilitates use of an external buffer amplifier for current ranges greater than ±64mA.

A voltage proportional to the measured output voltage or current is provided at the MSR_ output. Integrated comparators, with externally set voltage thresholds, provide detection for both voltage and current levels. The MSR_ and comparator outputs can be placed in a high-impedance state. Separate FORCE and SENSE connections are short-circuit protected for voltages from (V_{EE} - 0.3V) to (V_{CC} + 0.3V). The FORCE output also features a low-leakage, high-impedance state.

Integrated voltage clamps limit the force output to levels set externally. The force-current or the measure-current voltage can be offset -0.2V to +4.4V (IOS). This feature allows for the centering of the control or measured signal within the external DAC or ADC range.

The MAX9951D/MAX9952D feature an integrated 10kΩ force-sense resistor between FORCE_ and SENSE_. The MAX9951F/MAX9952F have no internal force-sense resistor. These devices are available in a 64-pin, 10mm x 10mm, 0.5mm pitch TQFP package with an exposed 8mm x 8mm die pad on the top (MAX9951) or the bottom (MAX9952) of the package for efficient heat removal. The exposed pad is internally connected to V_{EE}. The MAX9951/MAX9952 are specified over the commercial 0°C to +70°C temperature range.

Applications

Memory Testers

VLSI Testers

System-on-a-Chip Testers

Structural Testers

Pin Configurations and Selector Guide appear at end of data sheet.

Features

- **Force Voltage/Measure Current (FVMI)**
- **Force Current/Measure Voltage (FIMV)**
- **Force Voltage/Measure Voltage (FVMV)**
- **Force Current/Measure Current (FIMI)**
- **Force Nothing/Measure Voltage (FNMV)**
- **Force Nothing/Measure Current (FNMI, Range E Only)**
- **Termination/Measure Current**
- **Termination/Measure Voltage**
- **Five Programmable Current Ranges**
  - **±2µA**
  - **±20µA**
  - **±200µA**
  - **±2mA**
  - **±64mA**
- **-2V to +7V Through -7V to +13V Input-Voltage Range**
- **Force-Current/Measure-Current Adjustable-Voltage Offset (IOS)**
- **Programmable Voltage Clamps at Force Output**
- **Low-Leakage, High-Impedance Measure, and Force States**
- **3-Wire Serial Interface**
- **Low 6mA (max) Quiescent Current per PMU**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9951DCCB+D	0°C to +70°C	64 TQFP-EPR*
MAX9951DCCB+TD	0°C to +70°C	64 TQFP-EPR*
MAX9951DCCB-D	0°C to +70°C	64 TQFP-EPR*
MAX9951DCCB-TD	0°C to +70°C	64 TQFP-EPR*
MAX9951FCCB+	0°C to +70°C	64 TQFP-EPR*
MAX9951FCCB+T	0°C to +70°C	64 TQFP-EPR*
MAX9951FCCB-D	0°C to +70°C	64 TQFP-EPR*
MAX9951FCCB-TD	0°C to +70°C	64 TQFP-EPR*
MAX9952DCCB+	0°C to +70°C	64 TQFP-EP**
MAX9952DCCB+T	0°C to +70°C	64 TQFP-EP**
MAX9952DCCB-D	0°C to +70°C	64 TQFP-EP**
MAX9952DCCB-TD	0°C to +70°C	64 TQFP-EP**
MAX9952FCCB+	0°C to +70°C	64 TQFP-EP**
MAX9952FCCB+T	0°C to +70°C	64 TQFP-EP**
MAX9952FCCB-D	0°C to +70°C	64 TQFP-EP**
MAX9952FCCB-TD	0°C to +70°C	64 TQFP-EP**

+Denotes a lead(Pb)-free/RoHS-compliant package.
-Denotes a package containing lead(Pb).
D = Dry pack. **EPR = Top side exposed pad.*
T = Tape and reel. ***EP = Exposed pad.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-3247; Rev 6; 8/13

ABSOLUTE MAXIMUM RATINGS

V_{CC} to AGND .....+20V
V_{EE} to AGND .....-15V
V_{CC} to V_{EE} .....+32V
V_L to AGND .....+6V
AGND to DGND .....-0.5V to +0.5V
Digital Inputs/Outputs .....-0.3V to (V_L + 0.3V)
All Other Pins to AGND .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
MAX9951_CCB (derate 125mW/°C above +70°C) ...10,000mW
MAX9952_CCB (derate 43.5mW/°C above +70°C) 3478mW
θ_{JA} MAX9951_CCB (Note 1) .....+8°C/W
θ_{JC} MAX9951_CCB (Note 1) .....+2°C/W
θ_{JA} MAX9952_CCB (Note 1) .....+23°C/W
θ_{JC} MAX9952_CCB (Note 1) .....+2°C/W
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Operating Temperature Range (commercial) .....0°C to +70°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
Lead(Pb)-Free Packages .....+260°C
Packages Containing Lead(Pb) .....+240°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = T_{MIN} and T_A = T_{MAX} are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FORCE VOLTAGE							
Force Input Voltage Range	$V_{IN0\_}$, $V_{IN1\_}$			V_{EE} + 2.5		V_{CC} - 2.5	V
Forced Voltage	V_{DUT}	DUT current at full scale	V_{CC} = +12V, V_{EE} = -7V	-2		+7	V
			V_{CC} = +18V, V_{EE} = -12V	-7		+13	
		DUT current = 0A		V_{EE} + 2.5		V_{CC} - 2.5	
Input Bias Current					±1		µA
Forced-Voltage Offset	V_{FOS}			-25		+25	mV
Forced-Voltage-Offset Temperature Coefficient					±100		µV/°C
Forced-Voltage Gain Error	V_{FGE}	Nominal gain of +1		-1	0.005	+1	%
Forced-Voltage-Gain Temperature Coefficient					±10		ppm/°C
Forced-Voltage Linearity Error	V_{FLER}	Gain and offset errors calibrated out (Notes 3, 4)		-0.02		+0.02	%FSR
MEASURE CURRENT							
Measure-Current Offset	I_{MOS}	(Note 3)		-1		+1	%FSR
Measure-Current-Offset Temperature Coefficient					±20		ppm/°C
Measure-Current Gain Error	I_{MGE}	(Note 5)		-1		+1	%
Measure-Current-Gain Temperature Coefficient					±20		ppm/°C
Linearity Error	I_{MLER}	Gain and offset errors calibrated out (Notes 3, 4, 6)		-0.02		+0.02	%FSR

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = T_{MIN} and T_A = T_{MAX} are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Measure-Output-Voltage Range Over Full-Current Range	$V_{MSR\_}$	V_{IOS} = V_{DUTGND}	-4		+4	V
		V_{IOS} = 4V + V_{DUTGND}	0		+8	
Current-Sense Amp Offset-Voltage Input	V_{IOS}	Relative to V_{DUTGND}	-0.2		+4.4	V
Rejection of Output-Measure Error Due to Common-Mode Sense Voltage	$CMVR_{LER}$	(Notes 5 and 7)		+0.001	+0.007	%FSR/V
Measure-Current Range		Range E, R_E = 500kΩ	-2		+2	µA
		Range D, R_D = 50kΩ	-20		+20	
		Range C, R_C = 5kΩ	-200		+200	
		Range B, R_B = 500Ω	-2		+2	mA
		Range A, R_A = 15.6Ω	-64		+64	
FORCE CURRENT						
Input Voltage Range for Setting Forced Current Over Full Range	$V_{IN0\_}$, $V_{IN1\_}$	V_{IOS} = V_{DUTGND}	-4		+4	V
		V_{IOS} = 4V + V_{DUTGND}	0		+8	
Current-Sense Amp Offset-Voltage Input	V_{IOS}	Relative to V_{DUTGND}	-0.2		+4.4	V
IOS_ Input Bias Current				±1		µA
Forced-Current Offset		(Note 3)	-1		+1	%FSR
Forced-Current-Offset Temperature Coefficient				±20		ppm/°C
Forced-Current Gain Error		(Note 5)	-1		+1	%
Forced-Current-Gain Temperature Coefficient				±20		ppm/°C
Forced-Current Linearity Error	I_{FLER}	Gain and offset errors calibrated out (Notes 3, 4, 6)	-0.02		+0.02	%FSR
Rejection of Output Error Due to Common-Mode Load Voltage	$CMRI_{OER}$	(Notes 5 and 7)		+0.001	+0.007	%FSR/V
Forced-Current Range		Range E, R_E = 500kΩ	-2		+2	µA
		Range D, R_D = 50kΩ	-20		+20	
		Range C, R_C = 5kΩ	-200		+200	
		Range B, R_B = 500Ω	-2		+2	mA
		Range A, R_A = 15.6Ω	-64		+64	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = T_{MIN} and T_A = T_{MAX} are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MEASURE VOLTAGE							
Measure-Voltage-Offset	V_{MOS}			-25		+25	mV
Measure-Voltage-Offset Temperature Coefficient					±100		µV/°C
Gain Error	V_{MGER}	Nominal gain of +1		-1	±0.005	+1	%
Measure-Voltage-Gain Temperature Coefficient					±10		ppm/°C
Measure-Voltage Linearity Error	V_{MLER}	Gain and offset errors calibrated out (Notes 3, 4, 6)		-0.02		+0.02	%FSR
Measure-Output-Voltage Range Over Full DUT Voltage	V_{MSR}	DUT current at full scale	V_{CC} = +12V, V_{EE} = -7V	-2		+7	V
			V_{CC} = +18V, V_{EE} = -12V	-7		+13	
		DUT current = 0A		V_{EE} + 2.5		V_{CC} - 2.5	
FORCE OUTPUT							
Off-State Leakage Current				-1		+1	nA
Short-Circuit Current Limit	I_{LIM-}			-92		-65	mA
	I_{LIM+}			+65		+92	
Force-to-Sense Resistor	R_{FS}	D option only		8	10	12	kΩ
SENSE INPUT							
Input Voltage Range				V_{EE} + 2.5		V_{CC} - 2.5	V
Leakage Current		F option only		-1		+1	nA
COMPARATOR INPUTS							
Input Voltage Range				V_{EE} + 2.5		V_{CC} - 2.5	V
Offset Voltage				-25		+25	mV
Input Bias Current					±1		µA
VOLTAGE CLAMPS							
Input Control Voltage	$V_{CLLO\_}$, $V_{CLHI\_}$			V_{EE} + 2.4		V_{CC} - 2.4	V
Clamp Voltage Accuracy		(Note 8)		-100		+100	mV
DIGITAL INPUTS							
Input High Voltage (Note 9)	V_{IH}	V_L = 5V		+3.5			V
		V_L = 3.3V		+2.0			
		V_L = 2.5V		+1.7			
Input Low Voltage (Note 9)	V_{IL}	V_L = 5V or 3.3V				+0.8	V
		V_L = 2.5V				+0.7	
Input Current	I_{IN}				±1		µA
Input Capacitance	C_{IN}				3.0		pF

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = T_{MIN} and T_A = T_{MAX} are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMPARATOR OUTPUTS						
Output High Voltage	V_{OH}	V_L = +2.375V to +5.5V, R_{PUP} = 1kΩ	V_L - 0.2			V
Output Low Voltage	V_{OL}	V_L = +2.375V to +5.5V, R_{PUP} = 1kΩ			+0.4	V
High-Impedance-State Leakage Current				±1		µA
High-Impedance-State Output Capacitance				6.0		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{OUT} = 1mA, V_L = +2.375V to +5.5V, relative to DGND	V_L - 0.25			V
Output Low Voltage	V_{OL}	I_{OUT} = -1mA, V_L = +2.375V to +5.5V, relative to DGND			+0.2	V
POWER SUPPLY						
Positive Supply	V_{CC}	(Note 2)	+10	+12	+18	V
Negative Supply	V_{EE}	(Note 2)	-15	-7	-5	V
Total Supply Voltage	V_{CC} - V_{EE}	(Note 10)			+30	V
Logic Supply	V_L		+2.375		+5.5	V
Positive Supply Current	I_{CC}	No load, clamps enabled			10.0	mA
Negative Supply Current	I_{EE}	No load, clamps enabled			10.0	mA
Logic Supply Current	I_L	No load, all digital inputs at rails			1.2	mA
Analog Ground Current	I_{AGND}	No load, clamps enabled		0.9		mA
Digital Ground Current	I_{DGND}	No load, all digital inputs at rails		1.4		mA
Power-Supply Rejection Ratio	PSRR	1MHz, measured at force output		20		dB
		60Hz, measured at force output		85		

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, $C_{CM\_}$ = 120pF, C_L = 100pF, T_A = +25°C, unless otherwise noted. Specifications at T_A = T_{MIN} and T_A = T_{MAX} are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FORCE VOLTAGE (Notes 10, 11)						
Settling Time		Range E, R_E = 500kΩ		150		µs
		Range D, R_D = 50kΩ		50		
		Range C, R_C = 5kΩ		20	30	
		Range B, R_B = 500Ω		20		
		Range A, R_A = 15.6Ω		25		
FORCE VOLTAGE/MEASURE CURRENT (Notes 11, 12)						
Settling Time		Range E, R_E = 500kΩ		500		µs
		Range D, R_D = 50kΩ		100		
		Range C, R_C = 5kΩ		30	55	
		Range B, R_B = 500Ω		25		
		Range A, R_A = 15.6Ω		25		
Range Change Switching		In addition to force-voltage and measure-current settling times, range A to range B, R_A = 15.6Ω, R_B = 500Ω		12		µs
FORCE CURRENT/MEASURE VOLTAGE (Notes 11, 12)						
Settling Time		Range E, R_E = 500kΩ		2500		µs
		Range D, R_D = 50kΩ		350		
		Range C, R_C = 5kΩ		30	60	
		Range B, R_B = 500Ω		25		
		Range A, R_A = 15.6Ω		25		
Range Change Switching		In addition to force-current and measure-voltage settling times, range A to range B, R_A = 15.6Ω, R_B = 500Ω		12		µs
SENSE INPUT TO MEASURE OUTPUT PATH						
Propagation Delay		C_{LMSR} = 100pF		0.2		µs
MEASURE OUTPUT						
Maximum Stable Load Capacitance			1000			pF
COMPARATORS (C_{LCOMP} = 20pF, R_{PUP} = 1kΩ)						
Propagation Delay		50mV overdrive, $1V_{P-P}$, measured from input-threshold zero crossing to 50% of output voltage (Note 13)		75		ns
Rise Time		20% to 80%		60		ns
Fall Time		80% to 20%		5		ns
SERIAL PORT (V_L = +3.3V, C_{DOUT} = 10pF)						
Serial Clock Frequency	f_{SCLK}	(Note 14)			20	MHz
SCLK Pulse-Width High	t_{CH}		12			ns
SCLK Pulse-Width Low	t_{CL}		12			ns

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, V_{EE} = -7V, V_L = +3.3V, $C_{CM\_}$ = 120pF, C_L = 100pF, T_A = +25°C, unless otherwise noted. Specifications at T_A = T_{MIN} and T_A = T_{MAX} are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Fall to DOUT Valid	t_{DO}				22	ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		10			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		22			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}		0			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		5			ns
DIN to SCLK High Setup	t_{DS}		10			ns
DIN to SCLK High Hold	t_{DH}	(Note 13)	0			ns
$\overline{CS}$ Pulse-Width High	t_{CSWH}		10			ns
$\overline{CS}$ Pulse-Width Low	t_{CSWL}		10			ns
$\overline{LOAD}$ Pulse-Width Low	t_{LDW}		20			ns
V_{DD} High to $\overline{CS}$ Low (Power-Up)		(Note 13)			500	ns

Note 2: The device operates properly with different supply voltages with equally different voltage swings.

Note 3: Interpret errors expressed in terms of %FSR (percent of full-scale range) as a percentage of the end-point-to-end-point range, i.e., for the ±64mA range, the full-scale range = 128mA, and a 1% error = 1.28mA.

Note 4: Case must be maintained ±5°C for linearity specifications.

Note 5: Tested in range C.

Note 6: Current linearity specifications are maintained to within 700mV of the clamp voltages when the clamps are enabled.

Note 7: Specified as the percent of full-scale range change at the output per volt change in the DUT voltage.

Note 8: $V_{CLLO\_}$ and $V_{CLHI\_}$ should differ by at least 700mV.

Note 9: The digital interface accepts +5V, +3.3V, and +2.5V CMOS logic levels. The voltage at V_L adjusts the threshold.

Note 10: Guaranteed by design.

Note 11: Settling times are to 0.1% of FSR. $C_{X\_}$ = 60pF.

Note 12: All settling times are specified using a single compensation capacitor ($C_{X\_}$) across all current-sense resistors. Use an individual capacitor across each sense resistor for better performance across all current ranges, particularly the lower ranges.

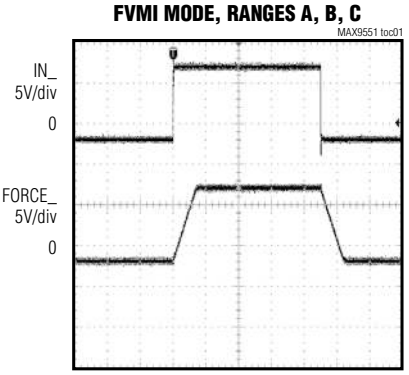
Note 13: The propagation delay time is only guaranteed over the force-voltage output range. Propagation delay is measured by holding $V_{SENSE\_}$ steady and transitioning THMAX_ or THMIN_.

Note 14: Maximum serial clock frequency may diminish at V_L < +3.3V.

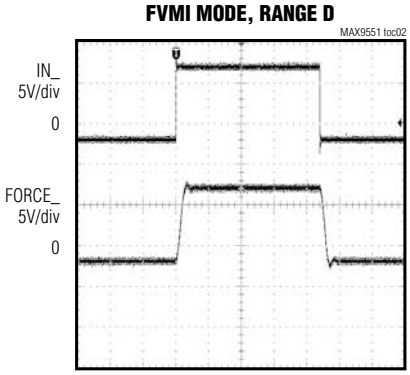
Typical Operating Characteristics

(V_{CC} = +12V, V_{EE} = -7V, C_L = 100pF, $C_{CM\_}$ = 120pF, $C_{CX\_}$ = 60pF, R_L to +2.5V, range A: R_A = 15.6Ω, R_L = 70.3Ω; range B: R_B = 500Ω, R_L = 2.25kΩ; range C: R_C = 5kΩ, R_L = 22.5kΩ; range D: R_D = 50kΩ, R_L = 225kΩ; range E: R_E = 500kΩ, R_L = 2.25MΩ, T_A = +25°C.)

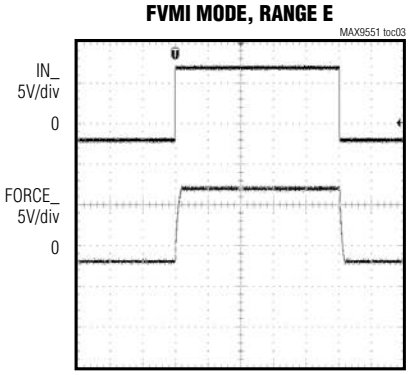
TRANSIENT RESPONSE FVMI MODE, RANGES A, B, C



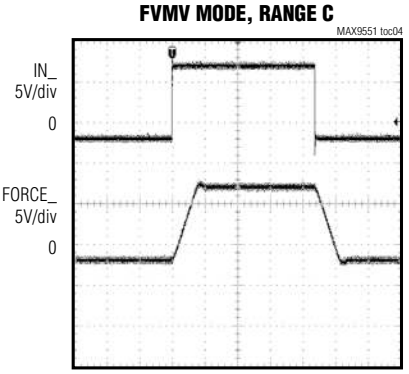
TRANSIENT RESPONSE FVMI MODE, RANGE D



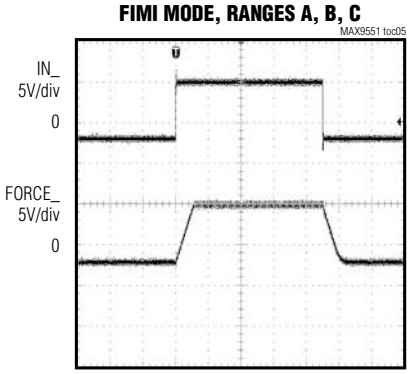
TRANSIENT RESPONSE FVMI MODE, RANGE E



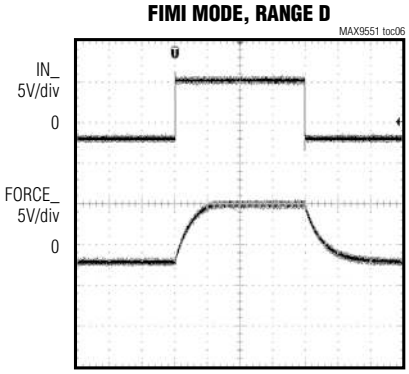
TRANSIENT RESPONSE FVMV MODE, RANGE C



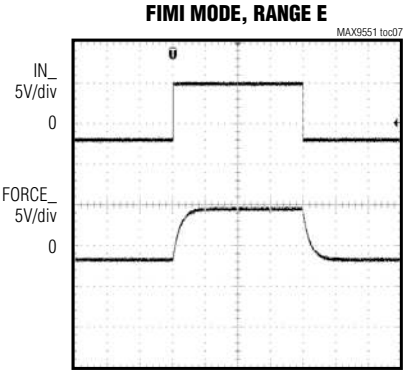
TRANSIENT RESPONSE FIMI MODE, RANGES A, B, C



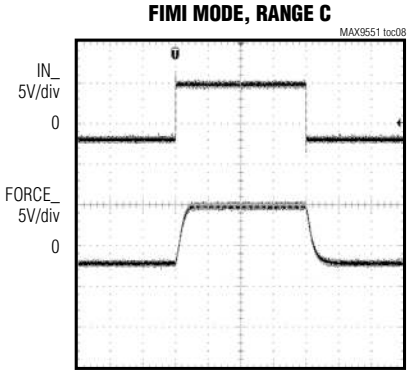
TRANSIENT RESPONSE FIMI MODE, RANGE D



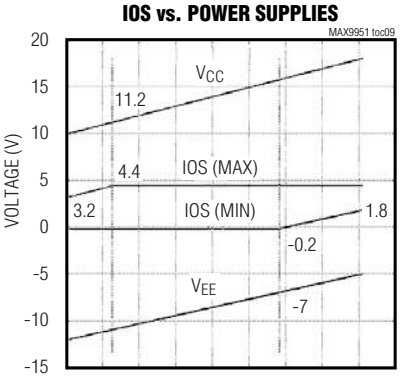
TRANSIENT RESPONSE FIMI MODE, RANGE E



TRANSIENT RESPONSE FIMI MODE, RANGE C



IOS vs. POWER SUPPLIES



Pin Description

PIN		NAME	FUNCTION
MAX9951	MAX9952		
1	48	SENSEA	PMU-A Sense Input. A Kelvin connection to the DUT. Provides the feedback signal in FVMI mode and the measured signal in FIMV mode for PMU-A.
2	47	FORCEA	PMU-A Driver Output. Forces a current or voltage to the DUT for PMU-A.
3	46	CCA	PMU-A Compensation Capacitor Connection. Provides compensation for the PMU-A main amplifier. Connect a 120pF capacitor from CCA to CCOMA.
5, 15, 34, 44	5, 15, 34, 44	V_{EE}	Negative Analog-Supply Input
4, 14, 35, 45	4, 14, 35, 45	V_{CC}	Positive Analog-Supply Input
6	43	CCOMA	Common Connection of CMA and CXA for PMU-A
7	42	RAAS	PMU-A Range Setting Resistor-Sense Connection
8	41	RAA	PMU-A Range A Setting Resistor Connection
9	40	RAB	PMU-A Range B Setting Resistor Connection
10	39	RAC	PMU-A Range C Setting Resistor Connection
11	38	RAD	PMU-A Range D Setting Resistor Connection
12	37	RAE	PMU-A Range E Setting Resistor Connection
13	36	RAX	PMU-A Current-Range Sense-Resistor Connection. Connects to the external current range sense resistor for PMU-A.
16	33	EXTSELA	PMU-A External Current-Range Selector. Selects the external current range for PMU-A.
17	32	$\overline{DUTLA}$	PMU-A Window Comparator Lower Comparator Output. A high output indicates that the sensed voltage at the window comparator is above V_{THMINA}. $\overline{DUTLA}$ is an open-drain output.
18	31	$\overline{DUTHA}$	PMU-A Window Comparator Higher Comparator Output. A high output indicates that the sensed voltage at the window comparator is below V_{THMAXA}. $\overline{DUTHA}$ is an open-drain output.
19	30	$\overline{HI\text{-}ZA}$	MSRA Tri-State Control Input. A logic-low places MSRA in a high-impedance state.
20	29	INSELA	Input Select PMU-A. INSELA is a logic input that selects between IN0A and IN1A. Force INSELA low to select IN0A. INSELA is OR'ed with control register bit INMODEA.
21	28	TEMP	Temperature Output. V_{TEMP} = 10mV/°C. T_{DIE}(°C) = (100)V_{TEMP} - 273.
22	27	DGND	Digital Ground
23	26	V_L	Logic-Supply Voltage Input. The voltage applied at V_L sets the upper logic-voltage level.
24	25	DOUT	Serial-Data Output. A standard SPI™-compatible output.
25	24	DIN	Serial-Data Input
26	23	$\overline{LOAD}$	Serial-Port Load Input. A logic-low asynchronously loads data from the input registers into the PMU registers.

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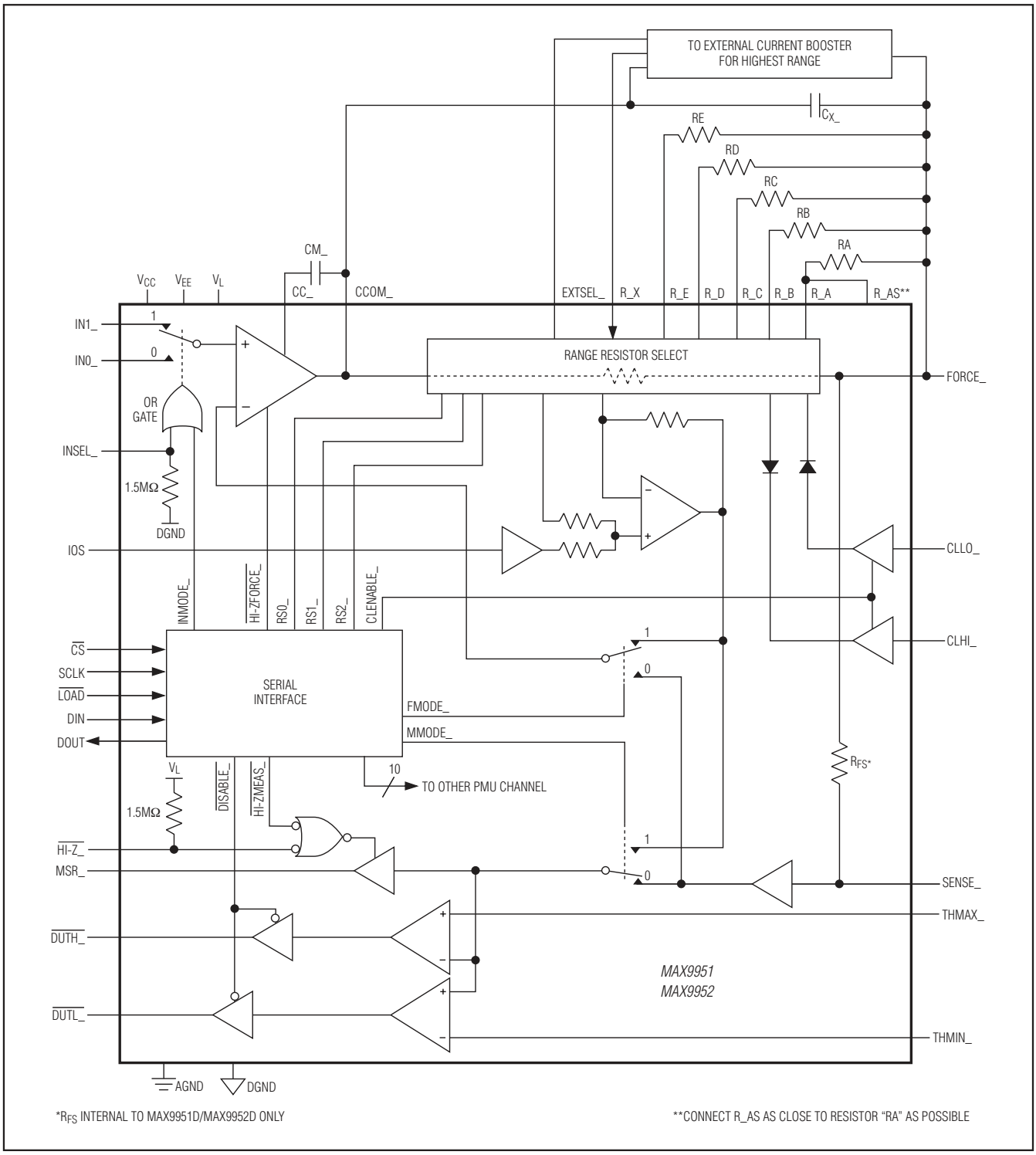
Pin Description (continued)

PIN		NAME	FUNCTION
MAX9951	MAX9952		
27	22	SCLK	Serial-Clock Input. SCLK accepts external clock frequencies up to 20MHz.
28	21	$\overline{CS}$	Chip-Select Input. Force $\overline{CS}$ low to enable the serial interface.
29	20	INSELB	Input Select PMU-B. INSELB is a logic input that selects between IN0B and IN1B. Force INSELB low to select IN0B. INSELB is OR'ed with control register bit INMODEB.
30	19	$\overline{HI\text{-}ZB}$	MSRB Tri-State Control Input. A logic-low places MSRB in a high-impedance state.
31	18	$\overline{DUTHB}$	PMU-B Window Comparator Higher Comparator Output. A high output indicates that the sensed voltage at the window comparator is below V_{THMAXB}. $\overline{DUTHB}$ is an open-drain output.
32	17	$\overline{DUTLB}$	PMU-B Window Comparator Lower Comparator Output. A high output indicates that the sensed voltage at the window comparator is above V_{THMINB}. $\overline{DUTLB}$ is an open-drain output.
33	16	EXTSELB	PMU-B External Current-Range Selector. Selects the external current range for PMU-B.
36	13	RBX	PMU-B Current-Range Sense-Resistor Connection. Connects to the external current-range sense resistor for PMU-B.
37	12	RBE	PMU-B Range E Setting Resistor Connection
38	11	RBD	PMU-B Range D Setting Resistor Connection
39	10	RBC	PMU-B Range C Setting Resistor Connection
40	9	RBB	PMU-B Range B Setting Resistor Connection
41	8	RBA	PMU-B Range A Setting Resistor Connection
42	7	RBAS	PMU-B Range A Setting Resistor-Sense Connection
43	6	CCOMB	Common Connection of CMB and CXB for PMU-B
46	3	CCB	PMU-B Compensation Capacitor Connection. Provides compensation for the PMU-B main amplifier. Connect a 120pF capacitor from CCB to CCOMB.
47	2	FORCEB	PMU-B Driver Output. Forces a current or voltage to the DUT for PMU-B.
48	1	SENSEB	PMU-B Sense Input. A Kelvin connection to the DUT. Provides the feedback signal in FVMI mode and the measured signal in FIMV mode for PMU-B.
49	64	THMAXB	PMU-B Window Comparator Upper Threshold Voltage Input. Sets the upper voltage threshold for the PMU-B window comparator.
50	63	THMINB	PMU-B Window Comparator Lower Threshold Voltage Input. Sets the lower voltage threshold for the PMU-B window comparator.
51	62	CLHIB	PMU-B Upper-Clamp Voltage Input. Sets the upper-clamp voltage level.
52	61	CLLOB	PMU-B Lower-Clamp Voltage Input. Sets the lower-clamp voltage level.
53	60	IN0B	Force-Threshold Current Input for PMU-B. Sets the forced voltage in FV mode or the forced current in FI mode.
54	59	IN1B	Force-Threshold Voltage Input for PMU-B. Sets the forced voltage in FV mode or the forced current in FI mode

Pin Description (continued)

PIN		NAME	FUNCTION
MAX9951	MAX9952		
55	58	MSRB	PMU-B Measurement Output. Provides a voltage equal to the SENSE voltage in FIMV mode, and provides a voltage proportional to the DUT current in FVMI mode for PMU-B. Force $\overline{HI\text{-}ZB}$ low to place MSRB in a high-impedance state.
56	57	AGND	Analog Ground
57	56	IOS	Offset-Voltage Input. Sets an offset voltage for the internal current-sense amplifiers of both channels.
58	55	MSRA	PMU-A Measurement Output. Provides a voltage equal to the SENSE voltage in FIMV mode, and provides a voltage proportional to the DUT current in FVMI mode for PMU-A. Force $\overline{HI\text{-}ZA}$ low to place MSRA in a high-impedance state.
59	54	IN1A	Force-Threshold Voltage Input for PMU-A. Sets the forced voltage in FV mode or the forced current in FI mode.
60	53	IN0A	Force-Threshold Current Input for PMU-A. Sets the forced voltage in FV mode or the forced current in FI mode.
61	52	CLLOA	PMU-A Lower-Clamp Voltage Input. Sets the lower-clamp voltage level.
62	51	CLHIA	PMU-A Upper-Clamp Voltage Input. Sets the upper-clamp voltage level.
63	50	THMINA	PMU-A Window Comparator Lower Threshold Voltage Input. Sets the lower voltage threshold for the PMU-A window comparator.
64	49	THMAXA	PMU-A Window Comparator Upper Threshold Voltage Input. Sets the upper voltage threshold for the PMU-A window comparator.
—	—	EP	Exposed Pad. Internally biased to V_{EE}. Connect to a large ground plane or heatsink to maximize thermal performance. Not intended as an electrical connection point.

Functional Diagram



Detailed Description

The MAX9951/MAX9952 force or measure voltages in the -2V to +7V through -7V to +13V ranges, dependent upon the supply voltage range (V_{CC} and V_{EE}). These devices also force or measure currents up to ±64mA, with a lowest full-scale range of ±2µA. Use an external buffer amplifier for current ranges greater than ±64mA.

MSR_ presents a voltage proportional to the measured voltage or current. Place MSR_ in a low-leakage, high-impedance state by forcing $\overline{HI\text{-}Z\_}$ low. Integrated comparators with externally programmable voltage thresholds provide "too low" ($\overline{DUTL\_}$) and "too high" ($\overline{DUTH\_}$) voltage-monitoring outputs. Each comparator output features a selectable high-impedance state. The devices feature separate FORCE_ and SENSE_ connections and are fully protected against short circuits. The FORCE_ output has two voltage clamps, negative (CLLO_) and positive (CLHI_), to limit the voltage to externally provided levels. Two control-voltage inputs, selected independently of the PMU mode, allow for greater flexibility.

Serial Interface

The MAX9951/MAX9952 use a standard 3-wire SPI/QSPI™/MICROWIRE™-compatible serial port. Once the input data register fills, the data becomes available at DOUT. This data output allows for daisy-chaining multiple devices. Figures 1, 2, and 3 show the serial interface timing diagrams.

Serial Port Operation

The serial interface has two ranks (Figure 4). Each PMU has an input register that loads from the serial port shift register. Each PMU also has a PMU register that loads from the input register. Data does not affect the PMU until it reaches the PMU register. This register configuration permits loading of the PMU data into the input register at one time and then latching the input register data into the PMU register later, at which time the PMU function changes accordingly. The register configuration also provides the ability to change the state of the PMU asynchronously, with respect to the loading of that PMU's data into the serial port. Thus, the PMU easily updates simultaneously with other PMUs or other devices.

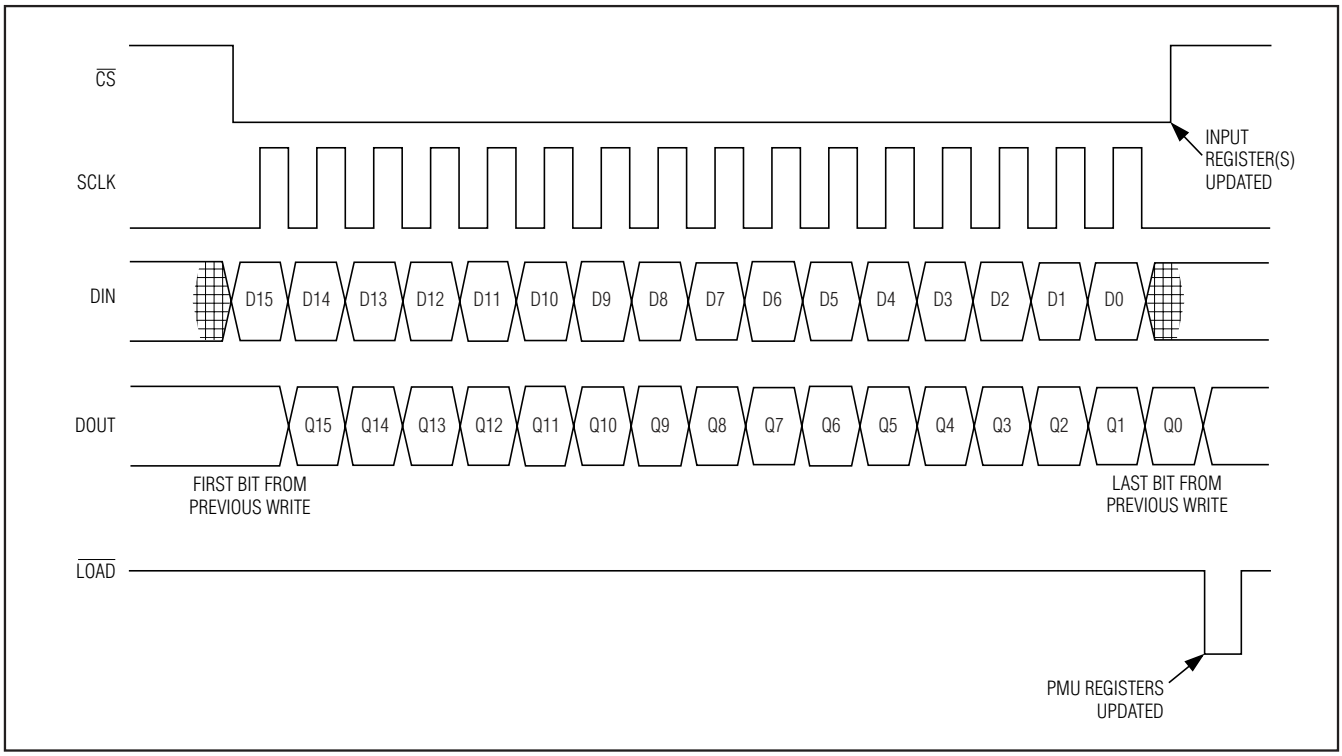


Figure 1. Serial Port Timing with Asynchronous Load

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MICROWIRE is a trademark of National Semiconductor Corp.

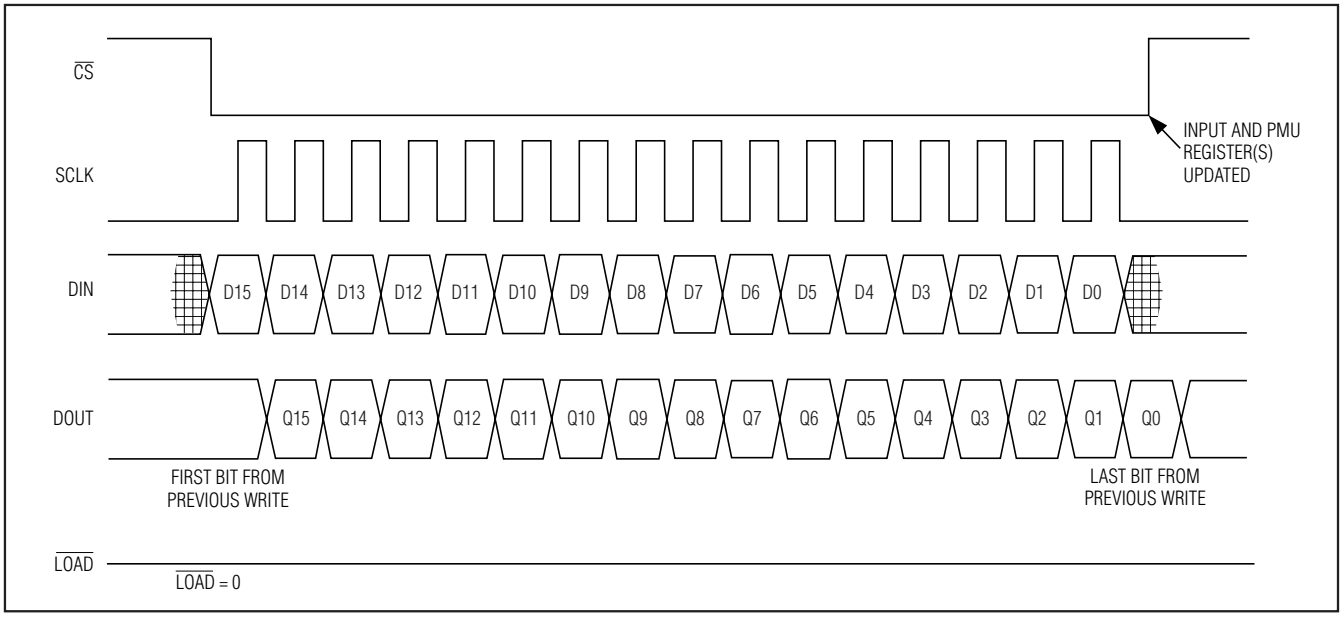


Figure 2. Serial Port Timing with Synchronous Load

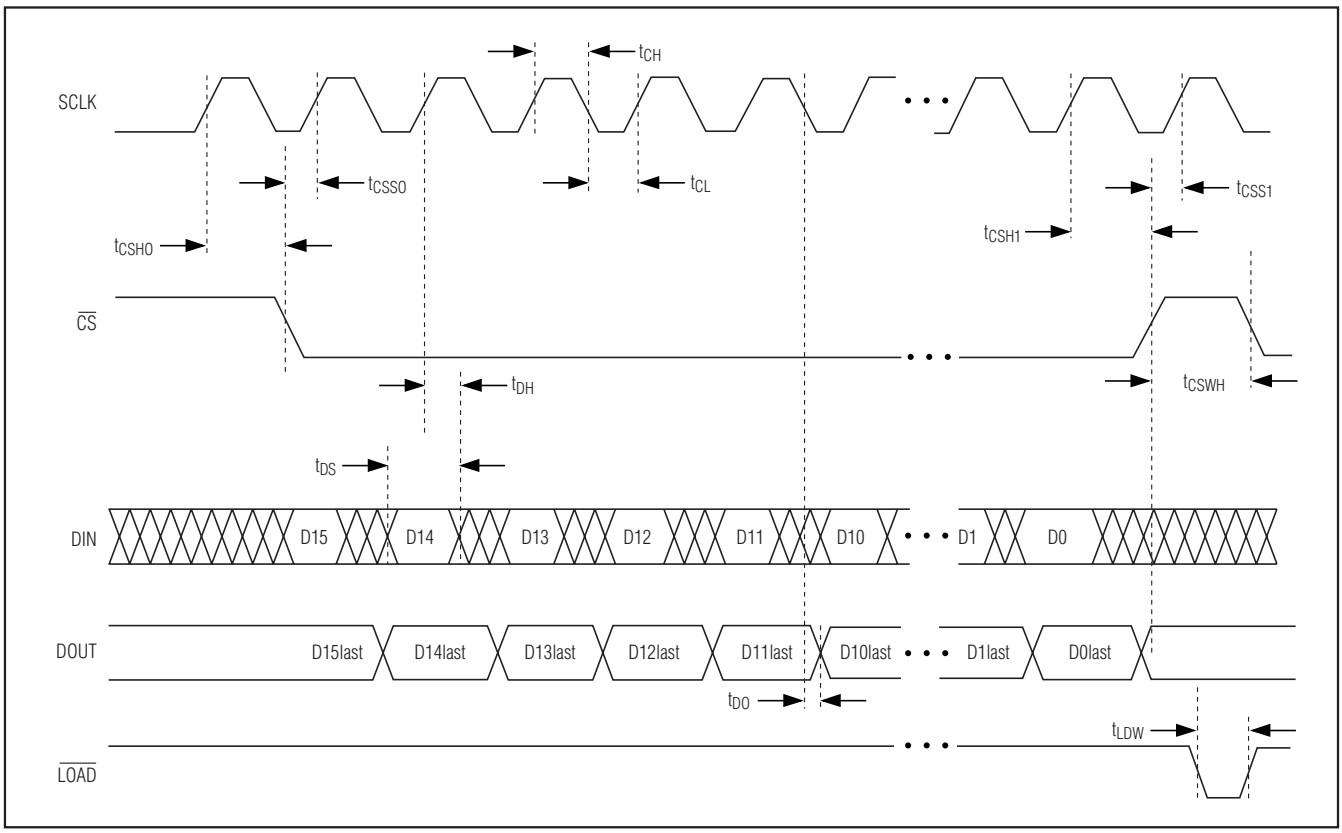


Figure 3. Detailed Serial Port Timing Diagram

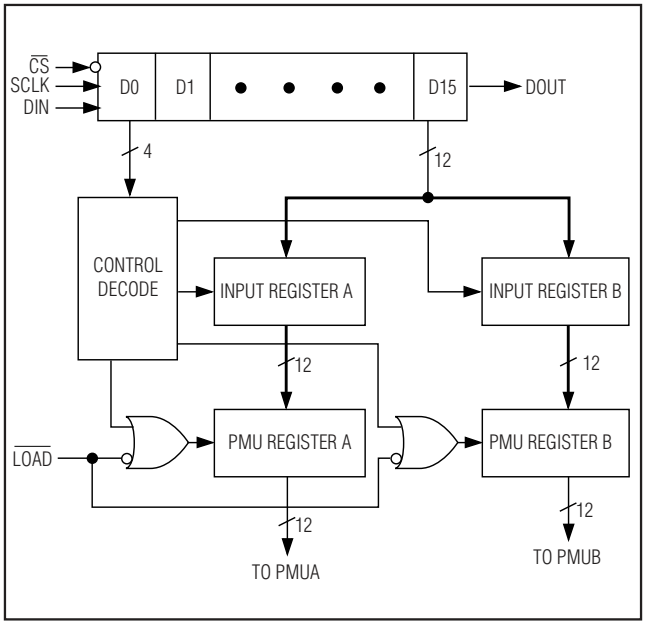


Figure 4. Dual PMU Serial Port Block Diagram

Use $\overline{\text{LOAD}}$ to asynchronously load all input registers into the PMU registers. If $\overline{\text{LOAD}}$ remains low when data latches into an input register, the data also transfers to the PMU register.

PMU Control

Programming both PMUs with the same data requires a 16-bit word. Programming each PMU with separate data requires two 16-bit words.

The address bits specify which input registers the shift-register loads. Table 2 describes the function of the address bits.

Bits C1 and C2 specify how the data loads into the second rank PMU registers. These 2 control bits serve a similar function as the $\overline{\text{LOAD}}$ input. The specified actions occur when $\overline{\text{CS}}$ goes high, whereas the $\overline{\text{LOAD}}$ input loads the PMU register at anytime. When either C1 or C2 is low, the corresponding PMU register is transparent. Table 3 describes the function of the 2 control bits.

The NOP operation requires A1 = A2 = C1 = C2 = 0. In this case, the data transfers through the shift register without changing the state of the device.

Table 1. Bit Assignments

BIT	BIT NAME
15	INMODE
14	FMODE
13	MMODE
12	RS2
11	RS1
10	RS0
9	CLENABLE
8	$\overline{\text{HI-ZFORCE}}$
7	$\overline{\text{HI-ZMSR}}$
6	$\overline{\text{DISABLE}}$
5	B2
4	B1
3	A2
2	A1
1	C2
0	C1

Table 2. Address Bit

A2	A1	OPERATION
0	0	Do not update any input register (NOP).
0	1	Only update input register A.
1	0	Only update input register B.
1	1	Update both input registers with the same data.

Table 3. Control Bit

C2	C1	OPERATION
0	0	Data stays in input register.
0	1	Transfer PMU-A input register to PMU register.
1	0	Transfer PMU-B input register to PMU register.
1	1	Transfer both input registers to the PMU registers.

C1 = C2 = 0 allows for data transfer from the shift register to the input register without transferring data to the PMU register (unless $\overline{LOAD}$ is low). This permits the latching of data into the PMU register at a later time by $\overline{LOAD}$ or subsequent command. Table 4 summarizes the possible control and address bit combinations. When asynchronously latching only one PMU's data, the input register of the other PMU maintains the same data. Therefore, loading both PMU registers would update the one PMU with new data while the other PMU remains in its current state.

Mode Selection

Four bits from the control word select between the various force-measure modes of operation. INMODE selects between the two input analog control voltages. FMODE selects whether the PMU forces a voltage or a current. MMODE selects whether the DUT current or DUT voltage is directed to MSR_. $\overline{HI\text{-}ZFORCE}$ places the driver amplifier in a high-output-impedance state. Table 5 describes the various force and measure modes of operation.

Table 4. PMU Operation Using Control and Address Bits

A2	A1	C2	C1	PMU-A OPERATION	PMU-B OPERATION
0	0	0	0	NOP: data just passes through	
0	0	0	1	Transfer PMU register A from input register A.	NOP.
0	0	1	0	NOP.	Transfer PMU register B from input register B.
0	0	1	1	Transfer PMU register A from input register A.	Transfer PMU register B from input register B.
0	1	0	0	Transfer input register A from shift register.	NOP.
0	1	0	1	Transfer input register A and PMU register A from shift register.	NOP.
0	1	1	0	Transfer input register A from shift register.	Transfer PMU register B from input register B.
0	1	1	1	Transfer input register A and PMU register A from shift register.	Transfer PMU register B from input register B.
1	0	0	0	NOP.	Transfer input register B from shift register.
1	0	0	1	Transfer PMU register A from input register A.	Transfer input register B from shift register.
1	0	1	0	NOP.	Transfer input register B and PMU register B from shift register.
1	0	1	1	Transfer PMU register A from input register A.	Transfer input register B and PMU register B from shift register.
1	1	0	0	Transfer input register A from shift register.	Transfer input register B from shift register.
1	1	0	1	Transfer input register A and PMU register A from shift register.	Transfer input register B from shift register.
1	1	1	0	Transfer input register A from shift register.	Transfer input register B and PMU register B from shift register.
1	1	1	1	Transfer input register A and PMU register A from shift register.	Transfer input register B and PMU register B from shift register.

Table 5. PMU Force-Measure Mode Selection

INMODE*	FMODE	MMODE	$\overline{\text{HI-ZFORCE}}$	PMU MODE	FORCE OUTPUT	MEASURE OUTPUT	ACTIVE INPUT
0	0	1	1	FVMI	Voltage	I_{DUT}	V_{IN0}
1	0	1	1	FVMI	Voltage	I_{DUT}	V_{IN1}
0	0	0	1	FVMV	Voltage	V_{DUT}	V_{IN0}
1	0	0	1	FVMV	Voltage	V_{DUT}	V_{IN1}
0	1	1	1	FIMI	Current	I_{DUT}	V_{IN0}
1	1	1	1	FIMI	Current	I_{DUT}	V_{IN1}
0	1	0	1	FIMV	Current	V_{DUT}	V_{IN0}
1	1	0	1	FIMV	Current	V_{DUT}	V_{IN1}
X	0	1	0	FNMI (range E only)	High-Impedance	I_{DUT}	X
X	0	0	0	FNMV	High-Impedance	V_{DUT}	X
0	1	0	0	Termination	Voltage	V_{DUT}	V_{IN0}
1	1	0	0	Termination	Voltage	V_{DUT}	V_{IN1}
0	1	1	0	Termination	Voltage	I_{DUT}	V_{IN0}
1	1	1	0	Termination	Voltage	I_{DUT}	V_{IN1}

**INSEL_ = 0*

Table 6. Current-Range Selection

RS2	RS1	RS0	RANGE	NOMINAL RESISTOR VALUE (Ω)
0	0	X	±2µA	R_E = 500k
0	1	0	±20µA	R_D = 50k
0	1	1	±200µA	R_C = 5k
1	0	0	±2mA	R_B = 500
1	X	1	±64mA	R_A = 15.6
1	1	0	External	—

Table 7. MSR_ Output Truth Table

$\overline{\text{HI-ZMSR}}$	$\overline{\text{HI-Z\_}}$	MSR_
1	1	Measure output enabled
0	1	High impedance
1	0	High impedance
0	0	High impedance

Current-Range Selection

Three bits from the control word, RS0, RS1, and RS2, control the full-scale current range for either FI (force current) or MI (measure current). Table 6 describes the full-scale current-range control.

Clamp Enable

The CLENABLE bit enables the force-output-voltage clamps when high and disables the clamps when low. There is hysteresis equal to approximately 5% of the current range for clamp when serial bit B1 is 1. For bit B1 = 0, no hysteresis, but clamp voltage is less accurate.

Measure Output High-Impedance Control

MSR_ attains a low-leakage, high-impedance state by using the $\overline{\text{HI-ZMSR}}$ control bit, or the $\overline{\text{HI-Z\_}}$ input. $\overline{\text{HI-Z\_}}$ is internally pulled up to V_L with a 1.5MΩ resistor. The 2 bits are logically ANDed together to control the MSR_ output. $\overline{\text{HI-Z\_}}$ allows external multiplexing among several PMU MSR_ outputs without using the serial interface. Table 7 explains the various output modes for the MSR_ output.

Digital Output (DOUT)

The digital output follows the last output of the serial-shift register and clocks out on the falling edge of SCLK. DOUT serially shifts the first bit of the incoming serial data word 16.5 clock cycles later. This allows for daisy-chaining additional devices using DOUT and the same clock.

"Quick Load" Using Chip Select

If $\overline{CS}$ goes low and then returns high without any clock activity, the data from the input registers latch into the PMU registers. This extra function is not standard for SPI/QSPI/MICROWIRE interfaces. The quick load mimics the function of $\overline{LOAD}$ without forcing $\overline{LOAD}$ low.

Comparators

Two comparators configured as a window comparator monitor MSR_. THMAX_ and THMIN_ set the high and low thresholds that determine the window. Both outputs are open drain and share a single disable control that places the outputs in a high-impedance, low-leakage state. Table 8 describes the comparator output states of the MAX9951/MAX9952.

Applications Information

In force-voltage (FV) mode, the voltage at FORCE_ is directly proportional to the input control voltage. In force-current (FI) mode, the current flowing out of FORCE_ is proportional to the input control voltage. Positive current flows out of the PMU.

In force-nothing (FN) mode, FORCE_ is high impedance.

In measure-current (MI) mode, the voltage at MSR_ is directly proportional to the current exiting FORCE_. Positive current flows out of the PMU.

In measure-voltage (MV) mode, the voltage at MSR_ is directly proportional to the voltage at SENSE_.

Current-Sense-Amplifier Offset-Voltage Input

IOS is a buffered input to the current-sense amplifiers. The current-sense amplifiers convert the input control voltage (IN0_ or IN1_) to the forced DUT current (FI), and convert the sensed DUT current to the MSR_ output voltage (MI). When IOS equals zero relative to DUTGND (the GND voltage at the DUT, which the level-setting DACs and the ADC are presumed to use as a ground reference), the nominal voltage range that corresponds to ±full-scale current is -4V to +4V. Any voltage applied to IOS adds directly to this control input/measure output voltage range, i.e., applying +4V to IOS forces the voltage range that corresponds to ±full-scale current from 0 to +8V.

The following equations determine the minimum and maximum currents for each current range corresponding to the input voltage or measure voltage:

$$V_{MAXCURRENT} = V_{IOS} + 4V$$

$$V_{MINCURRENT} = V_{IOS} - 4V$$

Choose IOS so the limits of MSR_ do not go closer than 2.8V to either V_{EE} or V_{CC}. For example, with supplies of +10V and -5V, limit the MSR_ output to -2.2V and +7.2V. Therefore, set IOS between +1.8V and +3.2V. MSR_ could clip if IOS is not within this range. Use these general equations for the limits on IOS:

$$\text{Minimum } V_{IOS} = V_{EE} + 6.8V$$

$$\text{Maximum } V_{IOS} = V_{CC} - 6.8V$$

Current Booster for Highest Current Range

An external buffer amplifier can be used to provide a current range greater than the MAX9951/MAX9952 maximum ±64mA output current (Figure 5). This function operates as follows:

Table 8. Comparator Truth Table

$\overline{DISABLE}$	CONDITION	$\overline{DUTH\_}$	$\overline{DUTL\_}$
0	X	High-Z	High-Z
1	$V_{MSR\_} > V_{THMAX\_}$ and $V_{THMIN\_}$	0	1
1	$V_{THMAX\_} > V_{MSR\_} > V_{THMIN\_}$	1	1
1	$V_{THMAX\_}$ and $V_{THMIN\_} > V_{MSR\_}$	1	0
1	$V_{THMIN\_} > V_{MSR\_} > V_{THMAX\_}$*	0	0

**$V_{THMAX\_} > V_{THMIN\_}$ constitutes normal operation. This condition, however, has $V_{THMIN\_} > V_{THMAX\_}$ and does not cause any problems with the operation of the comparators.*

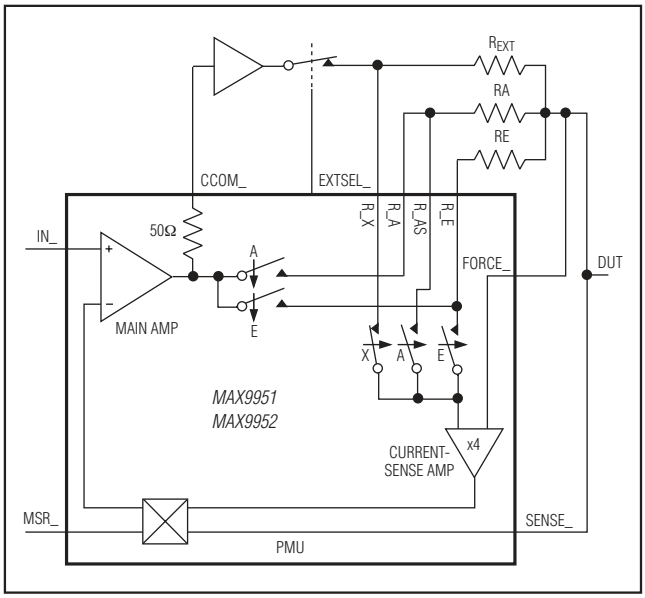


Figure 5. External Current Boost

A digital output decoded from the range select bits, EXTSEL_, indicates when to activate the booster. CCOM_ serves as an input to an external buffer through an internal 50Ω current-limit series resistor. Connect the external buffer output to the external current-sense resistor, R_{EXT}, and to R_X. Connect the other side of R_{EXT} to FORCE_. Ensure that the external switch is low leakage.

Voltage Clamps

The voltage clamps limit FORCE_ and operate over the entire specified current range. Set the clamp voltages externally at CLHI_ and CLLO_. The voltage at FORCE_ triggers the clamps independent of the voltage at SENSE_. When enabled, the clamps function in FI mode only. Use clamp voltages of 0.7V above and below the FORCE_ voltage range to ensure proper operation of the PMU.

Current Limit

The FORCE_ current-limiting circuitry, 92mA (maximum), ensures a well-behaved MSR_ output for currents between the full current range and the current limits. For currents greater than the full-scale current, the MSR_ voltage is greater than +4V, and for currents less than the full-scale current, the MSR_ voltage is less than -4V. Additionally, serial interface bit B2 enables a range-sensitive current limit of 2.5 times the nominal current range. Table 9 shows the current-limit operation.

Independent Control of the Feedback Switch and the Measure Switch

Two single-pole-double-throw (SPDT) switches determine the mode of operation of the PMU. One switch determines whether the sensed DUT current or DUT voltage feeds back to the input, and thus determines whether the MAX9951/MAX9952 force current or voltage. The other switch determines whether MSR_ senses the DUT current or DUT voltage.

Table 9. Current Limit

FMODE	RANGE	B2	CURRENT LIMIT
X	Any	0	65mA to 92mA
0	A	1	65mA to 92mA
0	B	1	5mA
0	C	1	500µA
0	D	1	50µA
0	E	1	5µA

Independent control of these switches and the HI-ZFORCE state permits flexible modes of operation beyond the traditional force-voltage/measure-current (FVMI) and force-current/measure-voltage (FIMV) modes. The MAX9951/MAX9952 support the following eight modes:

- FVMI
- FIMV
- FVMV
- FIMI
- FNMV
- FNMI (range E only)
- Terminate/Measure V
- Terminate/Measure I

Figure 6 shows the internal path structure for force-voltage/measure-current mode. In force-voltage/measure-current mode, the current across the appropriate external sense resistor (R_A to R_E) provides a voltage at MSR_. SENSE_ samples the voltage at the DUT and feeds the buffered result back to the negative input of the voltage amplifier. The voltage at MSR_ is proportional to the FORCE_ current in accordance with the following formula:

$$V_{MSR\_} = I_{FORCE\_} \times R_{SENSE} \times 4$$

Figure 7 shows the internal path structure for the force-current/measure-voltage mode. In force-current/measure-voltage mode, the appropriate external sense resistor (R_A to R_E) provides a feedback voltage to

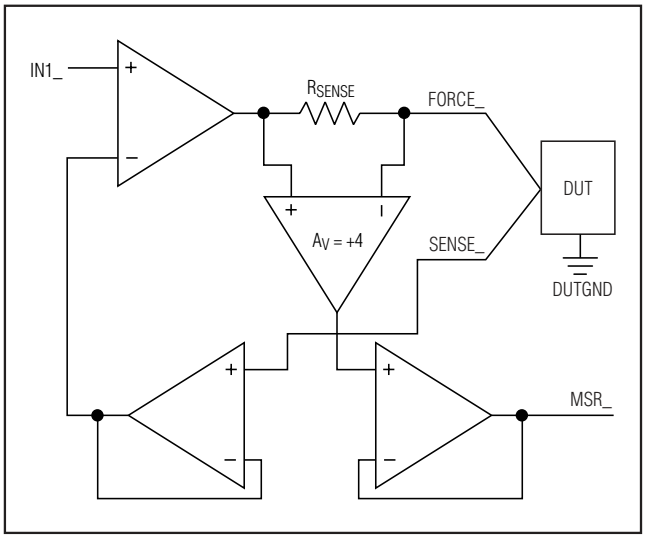


Figure 6. Force-Voltage/Measure-Current Functional Diagram

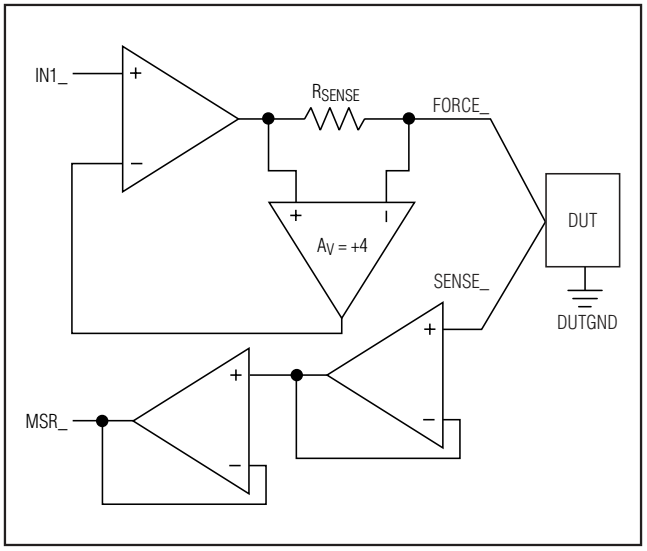


Figure 7. Force-Current/Measure-Voltage Functional Diagram

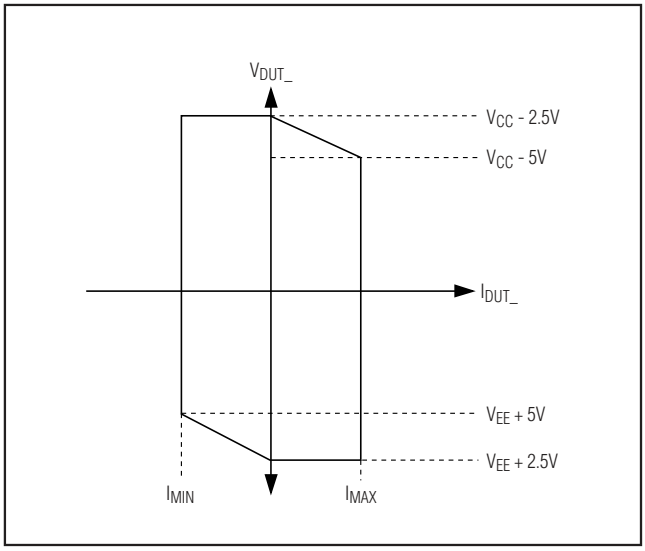


Figure 8. PMU Force-Output Capability

the inverting input of the voltage amplifier. SENSE_ samples the voltage at the DUT and provides a buffered result at MSR_.

High-Impedance States

The FORCE_, MSR_, and comparator outputs feature individual high-impedance control that places them into a high-impedance, low-leakage state. The high-impedance state allows busing of MSR_ and comparator outputs with other PMU measure and comparator outputs. The FORCE_ output high-impedance state allows for additional modes of operation as described in Table 5 and can eliminate the need for a series relay in some applications.

The FORCE_, MSR_, and comparator outputs power up in the high-impedance state.

Input Source Selection

Either one of two input signals, IN0_ or IN1_, can control both the forced voltage and the forced current. In this case, the two input signals represent alternate forcing values that can be selected either with the serial interface or INSEL_. Alternatively, each input signal can be dedicated to control a single forcing function (i.e., voltage or current).

Short-Circuit Protection

FORCE_ and SENSE_ input can withstand a short to any voltage between the supply rails.

Mode and Range Change Transients

The MAX9951/MAX9952 feature make-before-break switching to minimize glitches. The integrated voltage clamps also reduce glitching at the output.

DUT Voltage Swing vs. DUT Current and Power-Supply Voltages

Several factors limit the actual DUT voltage that the PMU delivers:

- The overhead required by the device amplifiers and other integrated circuitry; this is typically 2.5V from each rail independent of load.
- The voltage drop across the current-range select resistor and internal circuitry in series with the sense resistor. At full current, the combined voltage drop is typically 2.5V.
- Variations in the power supplies.
- Variation of DUT ground vs. PMU ground.

Neglecting the effects of the third and fourth items, Figure 8 demonstrates the force-output capabilities of the PMU. For zero DUT current, the DUT voltage swings from (V_{EE} + 2.5V) to (V_{CC} - 2.5V). For larger positive DUT currents, the positive swing drops off linearly until it reaches (V_{CC} - 5V) at full current. Similarly, for larger negative DUT currents, the negative voltage swing drops off linearly until it reaches (V_{EE} + 5V) at full current.

Ground, DUT Ground, and IOS

The MAX9951/MAX9952 utilize two local grounds, AGND (analog ground) and DGND (digital ground). Connect AGND and DGND together on the PC board. In a typical ATE system, the PMU force voltage is relative to DUT ground. In this case, reference the input voltages IN0_ and IN1_ to DUT ground. Similarly, reference IOS to DUT ground. If it is not desired to offset the current control and measure voltages, connect IOS to DUT ground potential.

Reference the MSR_ output to DUT ground.

Settling Times and Compensation Capacitors

The data in the *Electrical Characteristics* table reflects the circuit shown in the *Functional Diagram* that includes a single compensation capacitor ($C_{X\_}$) effectively across all the sense resistors. Placing individual capacitors, CRA, CRB, CRC, CRD, and CRE directly across the sense resistors, R_A, R_B, R_C, R_D, and R_E, independently optimizes each range.

The combination of the capacitance across the sense resistors, along with the main amplifier compensation comparator, CM_, ensures stability into the maximum expected load capacitance while optimizing settling time for a given load.

Digital Inputs (SCLK, DIN, $\overline{CS}$, and $\overline{LOAD}$)

The digital inputs incorporate hysteresis to mitigate issues with noise, as well as provide for compatibility with opto-isolators that can have slow edges.

Temperature Monitor

Each device supplies a single temperature output signal, TEMP, that asserts a nominal output voltage of 2.98V at a die temperature of +25°C (298K). The output voltage increases proportionately with temperature at a rate of 10mV/°C. The temperature sensor output impedance is 15kΩ (typ). Determine the die temperature using:

$$T_{DIE} = (100) \times V_{TEMP} - 273\ [°C]$$

Exposed Pad

The exposed pad is internally biased to V_{EE}. Connect to a large ground plane or heatsink to maximize thermal performance. Not intended as an electrical connection point. Leave EP electrically unconnected, or connect to V_{EE}. Do not connect EP to ground.

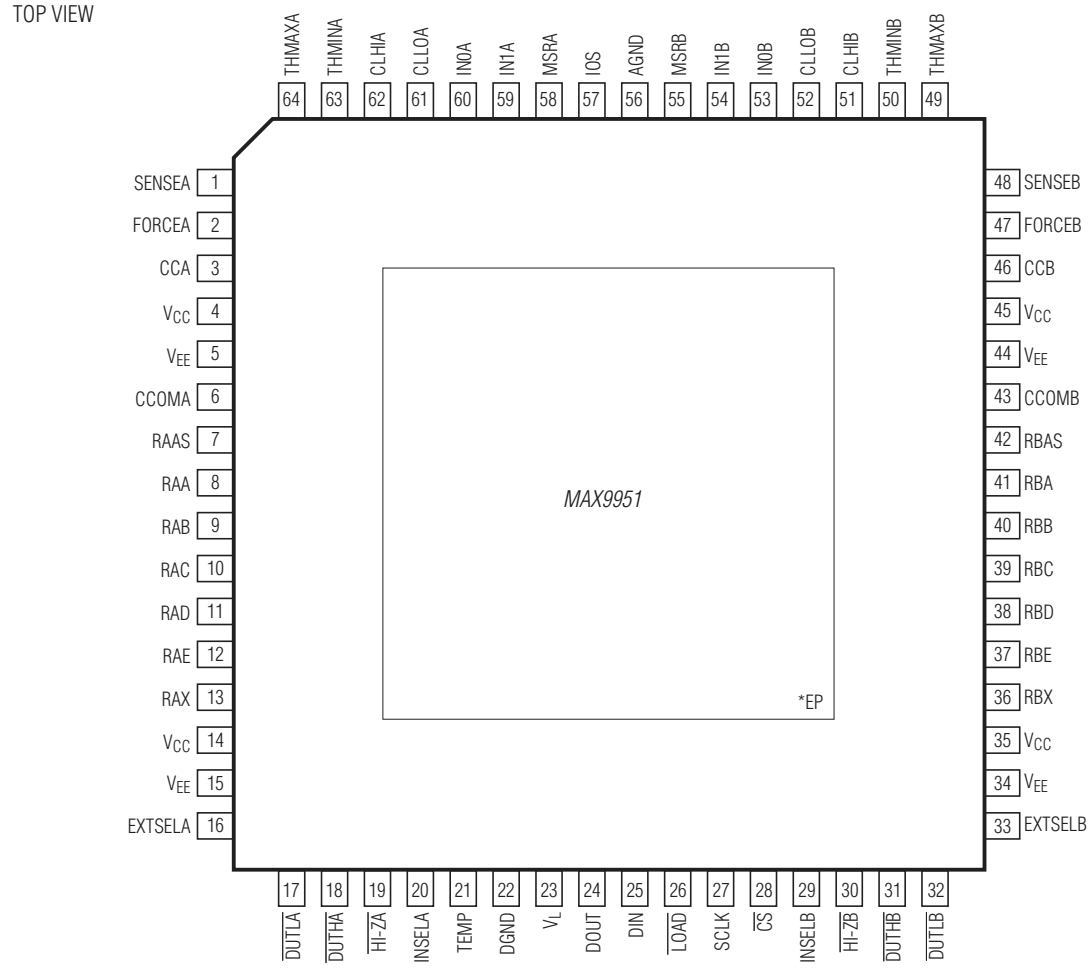
Selector Guide

PART	DESCRIPTION
MAX9951DCCB	Internal 10kΩ force-sense resistor
MAX9951FCCB	External force-sense resistor
MAX9952DCCB	Internal 10kΩ force-sense resistor
MAX9952FCCB	External force-sense resistor

Chip Information

PROCESS: BiCMOS

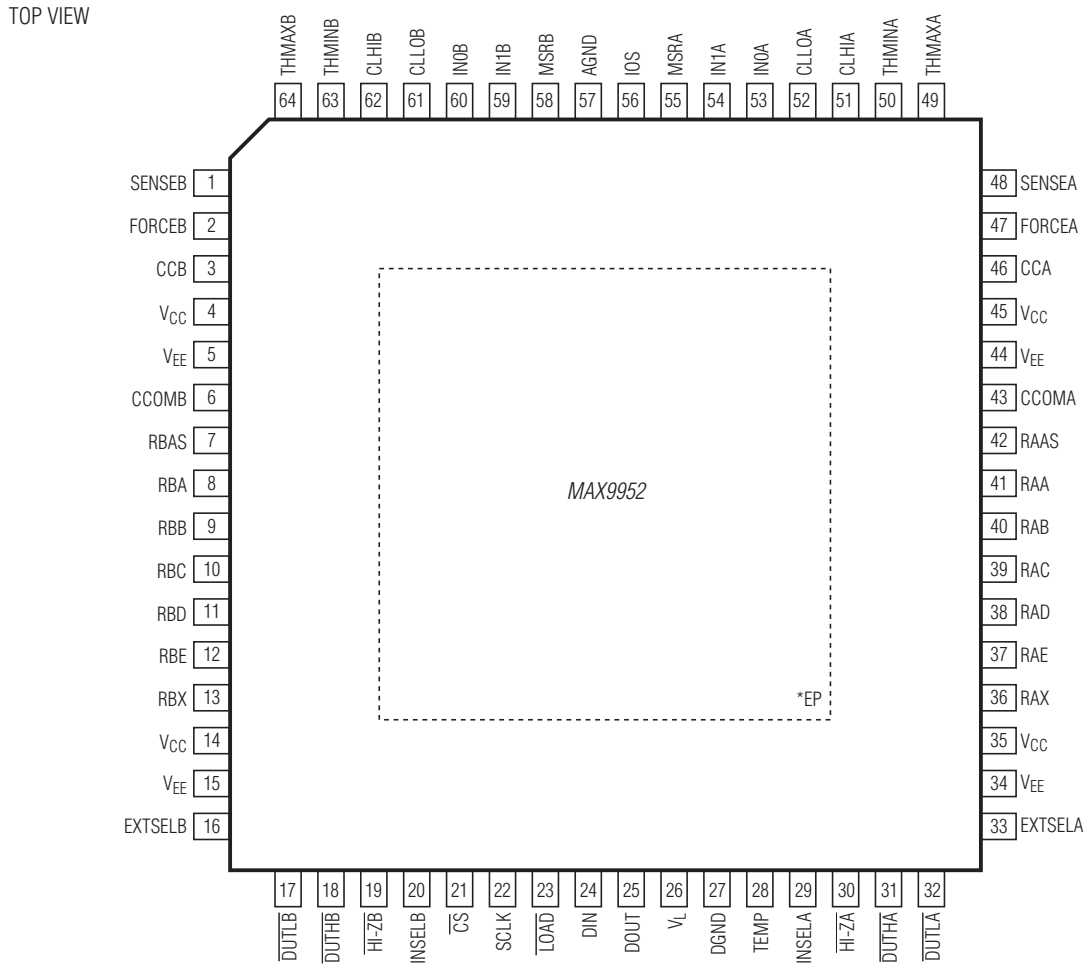
Pin Configurations



TQFP-EPR

*EP = EXPOSED PAD.

Pin Configurations (continued)



TQFP-EP

*EP = EXPOSED PAD.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
64 TQFP-EPR	C64E-6	21-0162
64 TQFP-EP	C64E-9R	21-0084

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	11/09	Corrected bit ordering in Figures 1, 2, and 3; updated *Ordering Information*; added exposed pad information	1, 11, 13, 14, 21, 22, 23
5	5/10	Updated *Absolute Maximum Ratings* section. Corrected timing diagrams and written descriptions so operation is more clearly understood. Bit names rather than bit numbers adopted.	2, 9, 13, 15–19
6	9/13	Corrected Package Information	23