ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

# NTE74HC161 & NTE74HC163
# Integrated Circuit
# TTL – High Speed CMOS,
# Synchronous 4–Bit Binary Counters

**Description:**

The NTE74HC161 (Asynchronous Clear) and NTE74HC163 (Synchronous Clear) are synchronous presettable counters in a 16–Lead DIP type package that utilize advanced silicon–gate CMOS technology and internal look–ahead carry logic for use in high speed counting applications. They offer the high noise immunity and low power consumption inherent to CMOS with speeds similar to low power Schottky TTL. All flip–flops are clocked simultaneously on the low to high to transition (positive–edge) of the CLOCK input waveform.

These counters may be preset using the LOAD input. Presetting of all four flip–flops is synchronous to the rising edge of CLOCK. When LOAD is held low, counting is disabled and the data on the A, B, C, and D inputs is loaded into the counter on the rising edge of CLOCK. If the load input is taken high before the positive edge of CLOCK, the count operation will be unaffected.

Both of these counters may be cleared by utilizing the CLEAR input. The clear function on the NTE74HC163 counter is synchronous to the clock. That is, the counter is cleared on the positive edge of CLOCK while the clear input is held low.

The NTE74HC161 counter is cleared asynchronously. When the CLEAR is taken low, the counter is cleared immediately, regardless of the CLOCK.

Two active high enable inputs (ENP and ENT) and a RIPPLE CARRY (RC) output are provided to enable easy cascading of counters. Both ENABLE inputs must be high to count. The ENT input also enables the RC output. When enabled, the RC outputs a positive pulse when the counter overflows. This pulse is approximately equal in duration to the high level portion of th $Q_A$ output. The RC output is fed to successive cascaded stages to facilitate easy implementation of N–bit counters.

All inputs are protected from damage due to static discharge by diodes to $V_{CC}$ and GND.

**Features:**

- Typical Operating Frequency: 40MHz
- Typical Propagation Delay: Clock to Q: 18ns
- Low Quiescent Current: 80μA (max)
- Low Input Current: 1μA (max)
- Wide Power Supply Range: 2V to 6V

**Absolute Maximum Ratings:** (Note 1, Note 2)

Supply Voltage, $V_{CC}$ ..... −0.5 to +7.0V
DC Input Voltage, $V_{IN}$ ..... −1.5 to $V_{CC}$ +1.5V
DC Output Voltage, $V_{OUT}$ ..... −0.5 to $V_{CC}$ + 0.5V
Clamp Diode Current, $I_{IK}$, $I_{OK}$ ..... ±20mA
DC Output Current (Per Pin), $I_{OUT}$ ..... ±25mA
DC $V_{CC}$ or GND Current (Per Pin), $I_{CC}$ ..... ±50mA
Power Dissipation (Note 3), $P_D$ ..... 600mW
Storage Temperature Range, $T_{stg}$ ..... −65°C to +150°C
Lead Temperature (During Soldering, 10sec), $T_L$ ..... +260°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.
Note 3. Power Dissipation temperature derating: 12mW/°C from +65°C to +85°C.

**Recommended Operating Conditions:**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 2.0 | – | 6.0 | V |
| DC Input or Output Voltage | $V_{IN}$, $V_{OUT}$ | 0 | – | $V_{CC}$ | V |
| Operating Temperature Range | $T_A$ | −55 | – | +85 | °C |
| Input Rise or Fall Times<br>$V_{CC}$ = 2.0V | $t_r$, $t_f$ | – | – | 1000 | ns |
| $V_{CC}$ = 4.5V | | – | – | 500 | ns |
| $V_{CC}$ = 6.0V | | – | – | 400 | ns |

**DC Electrical Characteristics:** (Note 4 unless otherwise specified)

| Parameter | Symbol | Test Conditions | | $V_{CC}$ | $T_A$ = +25°C | $T_A$ = −40° to +85°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Typ | Guaranteed Limits | | |
| Minimum High Level Input Voltage | $V_{IH}$ | | | 2.0 | – | 1.5 | 1.5 | V |
| | | | | 4.5 | – | 3.15 | 3.15 | V |
| | | | | 6.0 | – | 4.2 | 4.2 | V |
| Maximum Low Level Input Voltage | $V_{IL}$ | | | 2.0 | – | 0.5 | 0.5 | V |
| | | | | 4.5 | – | 1.35 | 1.35 | V |
| | | | | 6.0 | – | 1.8 | 1.8 | V |
| Minimum High Level Output Voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $\|I_{OUT}\| \le 20\mu A$ | – | $V_{CC}$ | $V_{CC}$ −0.1 | $V_{CC}$ −0.1 | V |
| | | | $\|I_{OUT}\| \le 4.0mA$ | 4.5 | 4.2 | 3.98 | 3.84 | V |
| | | | $\|I_{OUT}\| \le 5.2mA$ | 6.0 | 5.7 | 4.98 | 4.84 | V |
| Minimum Low Level Output Voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ | $\|I_{OUT}\| \le 20\mu A$ | – | 0 | 0.1 | 0.1 | V |
| | | | $\|I_{OUT}\| \le 4.0mA$ | 4.5 | 0.2 | 0.26 | 0.33 | V |
| | | | $\|I_{OUT}\| \le 5.2mA$ | 6.0 | 0.2 | 0.26 | 0.33 | V |
| Maximum Input Current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | 6.0 | – | ±0.1 | ±1.0 | μA |
| Maximum Quiescent Supply Current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0μA | | 6.0 | – | 8.0 | 80 | μA |

Note 4. For a power supply of 5V ±10% the worst case output voltages ($V_{OH}$ and $V_{OL}$) occur at 4.5V. Thus, the 4.5V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5V and 4.5V respectively (The $V_{IH}$ value at 5.5v is 3.85V). The worst case leakage current ($I_{IN}$, $I_{CC}$ and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0V vaules should be used.

**AC Electrical Characteristics:** ($V_{CC}$ = 5V, $t_r = t_f$ = 6ns, $C_L$ = 15pF, $T_A$ = +25°C unless otherwise specified)

| Parameter | Symbol | Test Conditions | Typ | Guaranteed Limits | Unit |
|---|---|---|---|---|---|
| Maximum Operating Frequency | $f_{MAX}$ | | 43 | 30 | ns |
| Maximum Propagation Delay (Clock to RC) | $t_{PHL}$, $t_{PLH}$ | | 30 | 36 | ns |
| Maximum Propagation Delay (Clock to Q) | $t_{PHL}$, $t_{PLH}$ | | 29 | 34 | ns |
| Maximum Propagation Delay (ENT to RC) | $t_{PHL}$, $t_{PLH}$ | | 18 | 32 | ns |
| Maximum Propagation Delay (Clear to Q or RC) | $t_{PHL}$ | | 27 | 38 | ns |
| Maximum Removal Time (Clear to Clock) | $t_{REM}$ | | 10 | 20 | ns |
| Minimum Set Up Time (Clear, Load, Enable or Data to Clock) | $t_S$ | | – | 30 | ns |
| Minimum Hold Time (Data from Clock) | $t_H$ | | – | 5 | ns |
| Minimum Pulse Width (Clock, Clear, or Load) | $t_W$ | | – | 16 | ns |

**AC Electrical Characteristics:** ($t_r = t_f$ = 6ns, $C_L$ = 50pF unless otherwise specified)

| Parameter | Symbol | Test Conditions | $V_{CC}$ | $T_A$ = +25°C | $T_A$ = −40° to +85°C | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| Maximum Operating Frequency | $f_{MAX}$ | | 2.0 | 10 | 5 | 4 | MHz |
| | | | 4.5 | 40 | 27 | 21 | MHz |
| | | | 6.0 | 45 | 32 | 25 | MHz |
| Maximum Propagation Delay (Clock to RC) | $t_{PHL}$ | | 2.0 | 100 | 215 | 271 | ns |
| | | | 4.5 | 32 | 43 | 54 | ns |
| | | | 6.0 | 28 | 37 | 46 | ns |
| | $t_{PLH}$ | | 2.0 | 88 | 175 | 220 | ns |
| | | | 4.5 | 18 | 35 | 44 | ns |
| | | | 6.0 | 15 | 30 | 37 | ns |
| Maximum Propagation Delay (Clock to Q) | $t_{PHL}$ | | 2.0 | 95 | 205 | 258 | ns |
| | | | 4.5 | 30 | 41 | 52 | ns |
| | | | 6.0 | 26 | 35 | 44 | ns |
| | $t_{PLH}$ | | 2.0 | 85 | 170 | 214 | ns |
| | | | 4.5 | 17 | 34 | 43 | ns |
| | | | 6.0 | 14 | 29 | 36 | ns |
| Maximum Propagation Delay (ENT to RC) | $t_{PHL}$ | | 2.0 | 90 | 195 | 246 | ns |
| | | | 4.5 | 28 | 39 | 49 | ns |
| | | | 6.0 | 24 | 33 | 42 | ns |
| | $t_{PLH}$ | | 2.0 | 80 | 160 | 202 | ns |
| | | | 4.5 | 16 | 32 | 40 | ns |
| | | | 6.0 | 14 | 27 | 34 | ns |
| Maximum Propagation Delay (Clear to RC) | $t_{PHL}$ | | 2.0 | 100 | 220 | 275 | ns |
| | | | 4.5 | 32 | 44 | 55 | ns |
| | | | 6.0 | 28 | 37 | 47 | ns |

**AC Electrical Characteristics (Cont'd):** ($t_r = t_f = 6ns$, $C_L = 50pF$ unless otherwise specified)

| Parameter | Symbol | Test Conditions | $V_{CC}$ | $T_A = +25°C$ | $T_A = -40°$ to $+85°C$ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| Maximum Propagation Delay (Clear to RC) | $t_{PHL}$ | | 2.0 | 100 | 220 | 275 | ns |
| | | | 4.5 | 32 | 44 | 55 | ns |
| | | | 6.0 | 28 | 37 | 47 | ns |
| Maximum Propagation Delay (Clear to Q) | $t_{PHL}$ | | 2.0 | 100 | 210 | 260 | ns |
| | | | 4.5 | 32 | 42 | 52 | ns |
| | | | 6.0 | 28 | 36 | 45 | ns |
| Minimum Removal Time (Clear to Clock) | $t_{REM}$ | | 2.0 | – | 125 | 158 | ns |
| | | | 4.5 | – | 25 | 32 | ns |
| | | | 6.0 | – | 21 | 27 | ns |
| Minimum Setup Time (Clear or Data to Clock) | $t_S$ | | 2.0 | – | 150 | 190 | ns |
| | | | 4.5 | – | 30 | 38 | ns |
| | | | 6.0 | – | 26 | 32 | ns |
| Minimum Setup Time (Load to Clock) | $t_S$ | | 2.0 | – | 135 | 170 | ns |
| | | | 4.5 | – | 27 | 34 | ns |
| | | | 6.0 | – | 23 | 29 | ns |
| Minimum Setup Time (Enable to Clock) | $t_S$ | | 2.0 | – | 175 | 220 | ns |
| | | | 4.5 | – | 35 | 44 | ns |
| | | | 6.0 | – | 30 | 37 | ns |
| Minimum Hold Time (Data from Clock) | $t_H$ | | 2.0 | – | 50 | 63 | ns |
| | | | 4.5 | – | 10 | 13 | ns |
| | | | 6.0 | – | 9 | 11 | ns |
| Minimum Hold Time (Enable, Load or Clear to Clock) | $t_H$ | | 2.0 | – | 0 | 0 | ns |
| | | | 4.5 | – | 0 | 0 | ns |
| | | | 6.0 | – | 0 | 0 | ns |
| Minimum Pulse Width (Clock, Clear or Load) | $t_W$ | | 2.0 | – | 80 | 100 | ns |
| | | | 4.5 | – | 16 | 20 | ns |
| | | | 6.0 | – | 14 | 17 | ns |
| Maximum Output Rise and Fall Time | $t_{THL}$, $t_{TLH}$ | | 2.0 | 40 | 75 | 95 | ns |
| | | | 4.5 | 8 | 15 | 19 | ns |
| | | | 6.0 | 7 | 13 | 16 | ns |
| Maximum Input Rise and Fall Time | $t_{THL}$, $t_{TLH}$ | | 2.0 | – | 1000 | 1000 | ns |
| | | | 4.5 | – | 500 | 500 | ns |
| | | | 6.0 | – | 400 | 400 | ns |
| Power Dissipation Capacitance | $C_{PD}$ | Per Package, Note 5 | – | 90 | – | – | pF |
| Maximum Input Capacitance | $C_{IN}$ | | – | 5 | 10 | 10 | pF |

Note 5. $C_{PD}$ determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

**Truth Tables:**

**NTE74HC161:**

| CLK | CLR | ENP | ENT | Load | Function |
|---|---|---|---|---|---|
| X | L | X | X | X | Clear |
| X | H | H | L | H | Count & RC Disabled |
| X | H | L | H | H | Count Disabled |
| X | H | L | L | H | Count & RC Disabled |
| ↑ | H | X | X | L | Load |
| ↑ | H | H | H | H | Increment Counter |

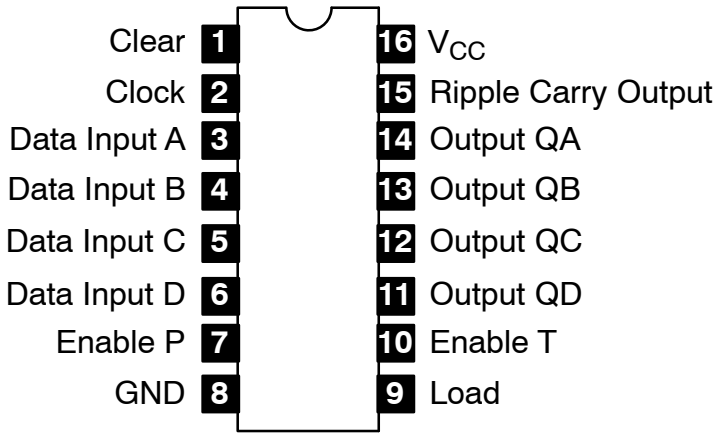
H = HIGH Level
L = LOW Level
X = Don't Care
↑ = LOW to HIGH Transition

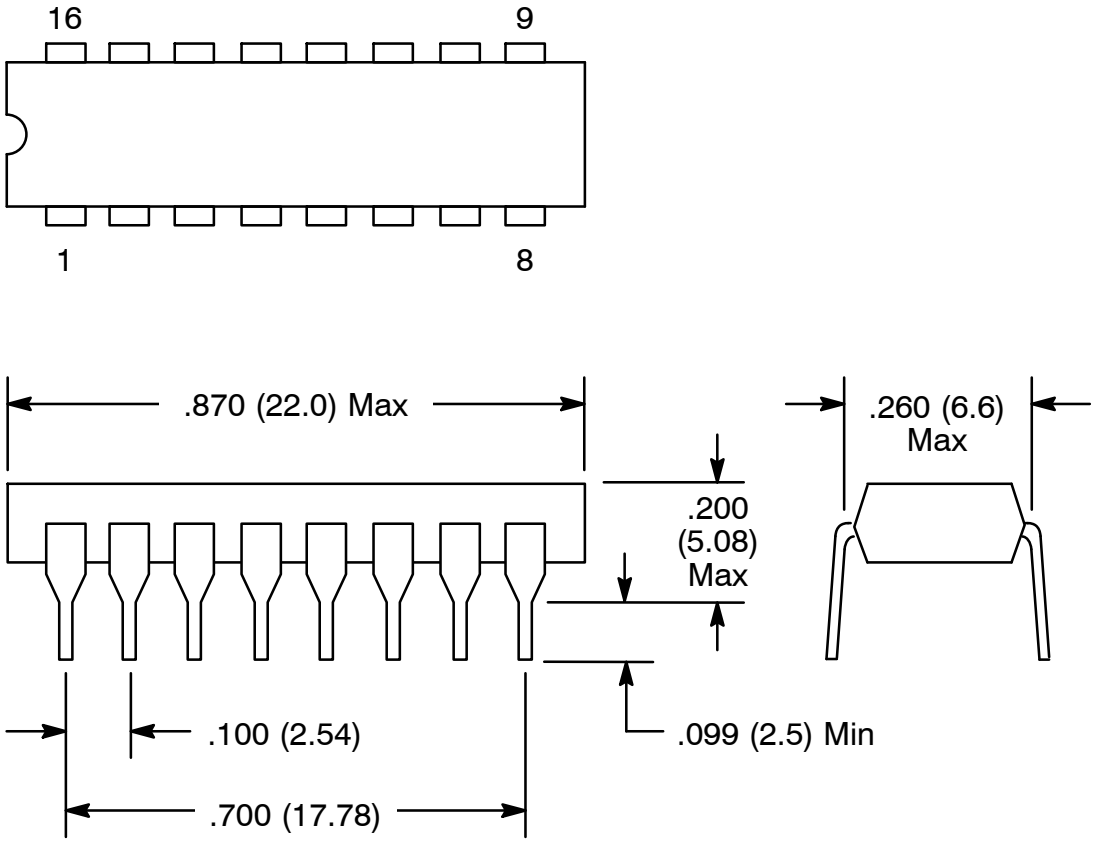
**NTE74HC163:**

| CLK | CLR | ENP | ENT | Load | Function |
|---|---|---|---|---|---|
| ↑ | L | X | X | X | Clear |
| X | H | H | L | H | Count & RC Disabled |
| X | H | L | H | H | Count Disabled |
| X | H | L | L | H | Count & RC Disabled |
| ↑ | H | X | X | L | Load |
| ↑ | H | H | H | H | Increment Counter |

H = HIGH Level
L = LOW Level
X = Don't Care
↑ = LOW to HIGH Transition

**Pin Connection Diagram**




16
9
1
8
.870 (22.0) Max
.260 (6.6)
Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)