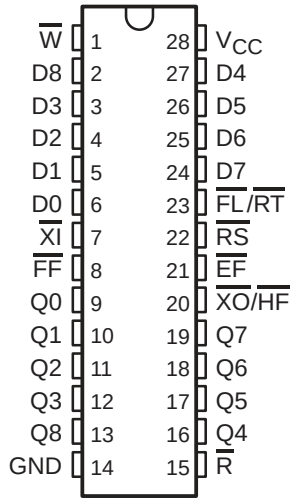
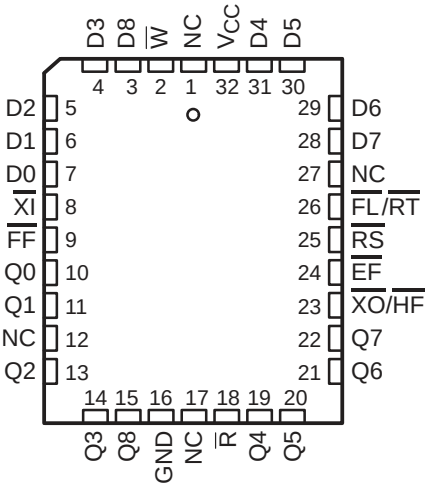
- **Reads and Writes Can Be Asynchronous or Coincident**
- **Organization:**
  - **SN74ACT7200L – 256 × 9**
  - **SN74ACT7201LA – 512 × 9**
  - **SN74ACT7202LA – 1024 × 9**
- **Fast Data Access Times of 15 ns**
- **Read and Write Frequencies up to 40 MHz**
- **Bit-Width and Word-Depth Expansion**
- **Fully Compatible With the IDT7200/7201/7202**
- **Retransmit Capability**
- **Empty, Full, and Half-Full Flags**
- **TTL-Compatible Inputs**
- **Available in 28-Pin Plastic DIP (NP), Small-Outline (DV), and 32-Pin Plastic J-Leaded Chip-Carrier (RJ) Packages**

DV OR NP PACKAGE
(TOP VIEW)



RJ PACKAGE
(TOP VIEW)



NC – No internal connection

description

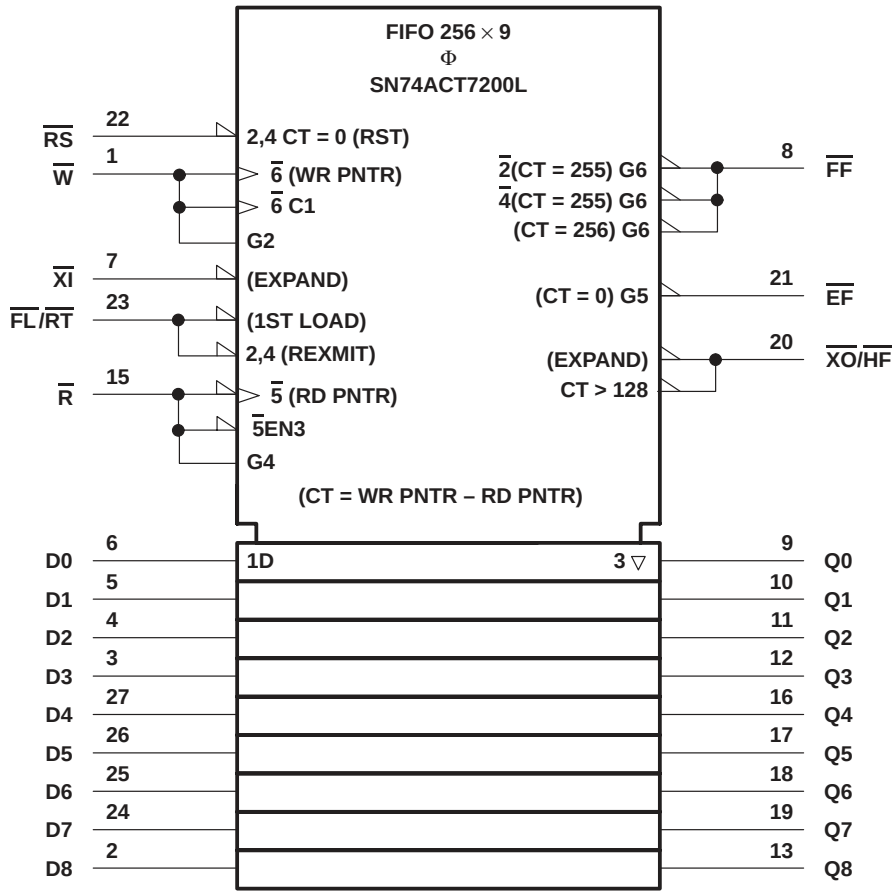
The SN74ACT7200L, SN74ACT7201LA, and SN74ACT7202LA are constructed with dual-port SRAM and have internal write and read address counters to provide data throughput on a first-in, first-out (FIFO) basis. Write and read operations are independent and can be asynchronous or coincident. Empty and full status flags prevent underflow and overflow of memory, and depth-expansion logic allows combining the storage cells of two or more devices into one FIFO. Word-width expansion is also possible.

Data is loaded into memory by the write-enable ($\overline{W}$) input and unloaded by the read-enable ($\overline{R}$) input. Read and write cycle times of 25 ns (40 MHz) are possible with data access times of 15 ns.

These devices are particularly suited for providing a data channel between two buses operating at asynchronous rates. Applications include use as rate buffers from analog-to-digital converters in data-acquisition systems, temporary storage elements between buses and magnetic or optical memories, and queues for communication systems. A 9-bit-wide data path is provided for the transmission of byte data plus a parity bit or packet-framing information. The read pointer can be reset independently of the write pointer for retransmitting previously read data when a device is not used in depth expansion.

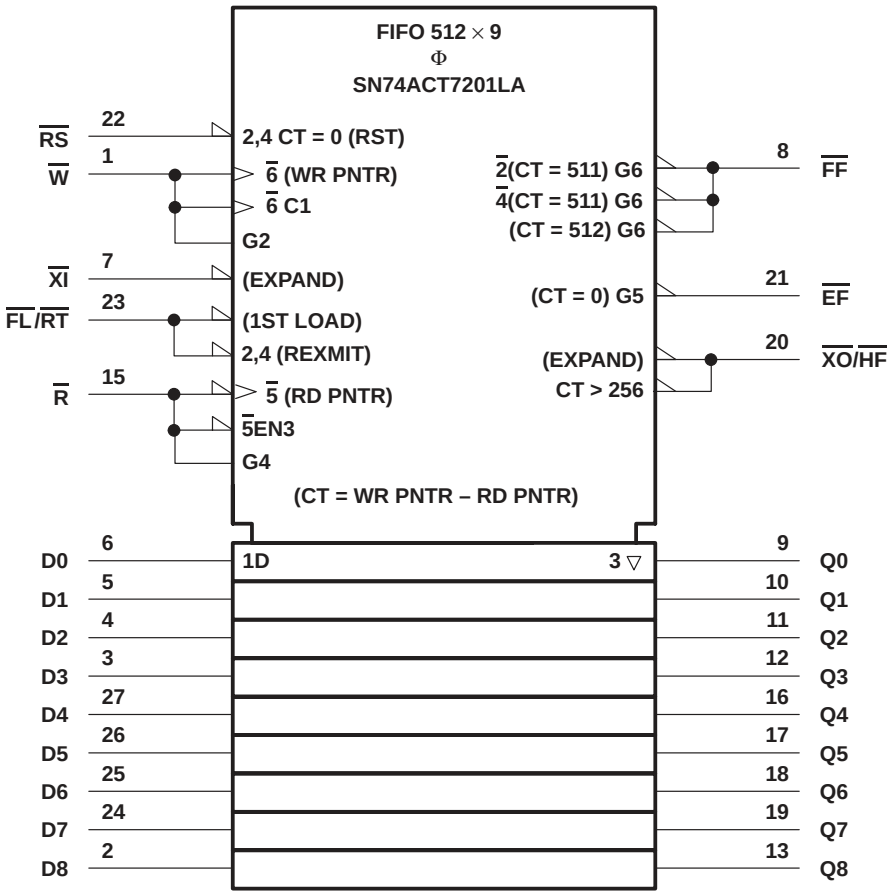
The SN74ACT7200L, SN74ACT7201LA, and SN74ACT7202LA are characterized for operation from 0°C to 70°C.

SN74ACT7200L logic symbol†



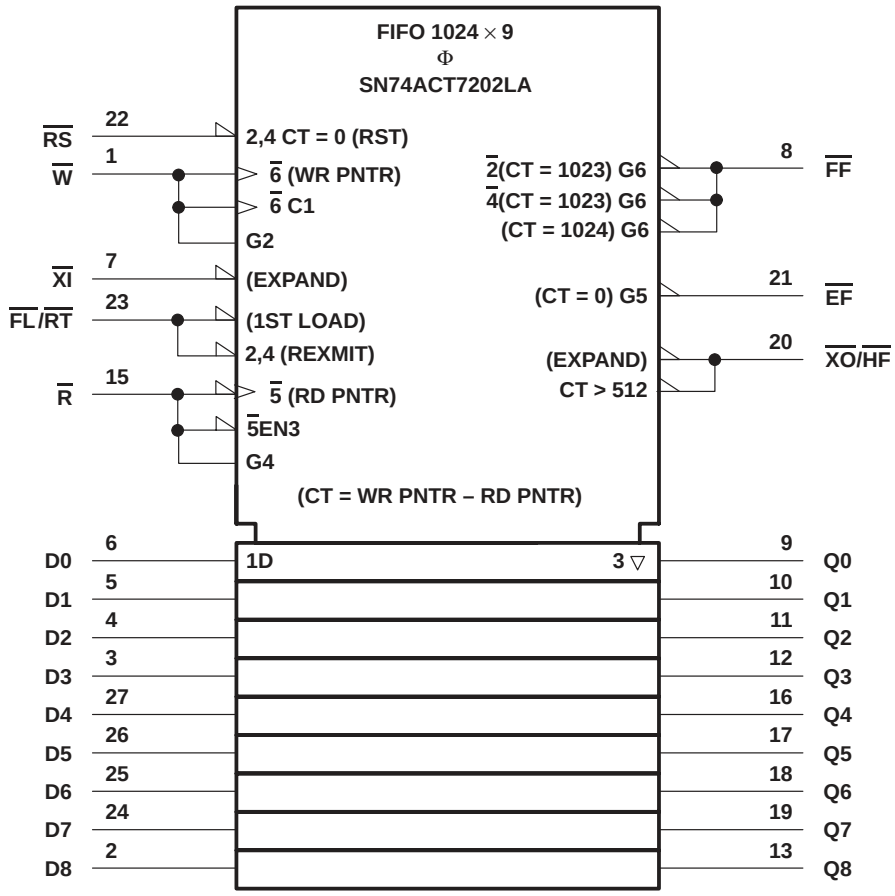
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DV and NP packages.

SN74ACT7201LA logic symbol†



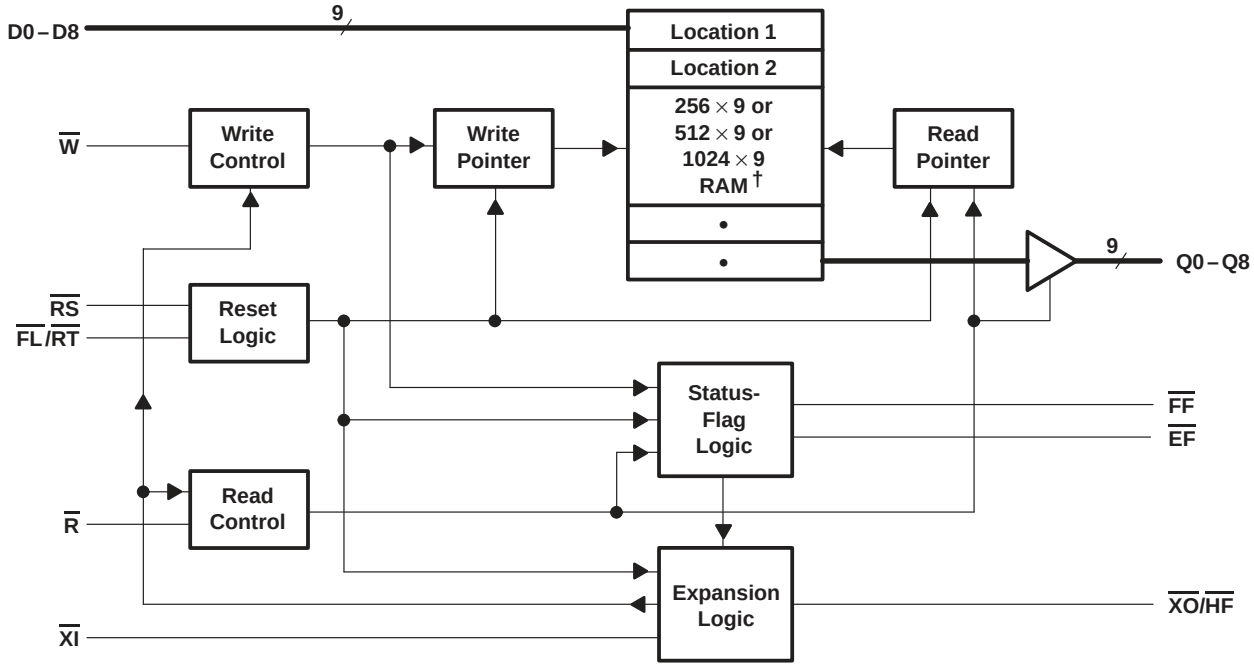
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DV and NP packages.

SN74ACT7202LA logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DV and NP packages.

functional block diagram



† 256 × 9 for SN74ACT7200L; 512 × 9 for SN74ACT7201LA; 1024 × 9 for SN74ACT7202LA

RESET AND RETRANSMIT FUNCTION TABLE
(single-device depth; single-or multiple-device width)

INPUTS			INTERNAL TO DEVICE		OUTPUTS			FUNCTION
$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{FF}$	$\overline{XO}/\overline{HF}$	
L	X	L	Location zero	Location zero	L	H	H	Reset device
H	L	L	Location zero	Unchanged	X	X	X	Retransmit
H	H	L	Increment if $\overline{EF}$ high	Increment if $\overline{FF}$ high	X	X	X	Read/write

RESET AND FIRST-LOAD FUNCTION TABLE
(multiple-device depth; single-or multiple-device width)

INPUTS			INTERNAL TO DEVICE		OUTPUTS		FUNCTION
$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{FF}$	
L	L	‡	Location zero	Location zero	L	H	Reset first device
L	H	‡	Location zero	Location zero	L	H	Reset all other devices
H	X	‡	X	X	X	X	Read/write

‡ $\overline{XI}$ is connected to $\overline{XO}/\overline{HF}$ of the previous device in the daisy chain (see Figure 15).

Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
D0–D8	I	Data inputs
$\overline{EF}$	O	Empty-flag output. $\overline{EF}$ is low when the read pointer is equal to the write pointer, inhibiting any operation initiated by a read cycle. When the FIFO is empty, a data word can be read automatically at Q0–Q8 by holding $\overline{R}$ low when loading the data word with a low-level pulse on $\overline{W}$.
$\overline{FF}$	O	Full-flag output. $\overline{FF}$ is low when the write pointer is one location less than the read pointer, indicating that the device is full and inhibiting any operation initiated by a write cycle. $\overline{FF}$ goes low when the number of writes after reset exceeds the number of reads by 256 for the SN74ACT7200L, 512 for the SN74ACT7201LA, and 1024 for the SN74ACT7202LA. When the FIFO is full, a data word can be written automatically into memory by holding $\overline{W}$ low while reading out another data word with a low-level pulse on $\overline{R}$.
$\overline{FL}/\overline{RT}$	I	First-load/retransmit input. $\overline{FL}/\overline{RT}$ performs two separate functions. When cascading two or more devices for word-depth expansion, $\overline{FL}/\overline{RT}$ is tied to ground on the first device in the daisy chain to indicate that it is the first device loaded and unloaded; it is tied high on all other devices in the depth-expansion chain. A device is not used in depth expansion when its expansion ($\overline{XI}$) input is tied to ground. In that case, $\overline{FL}/\overline{RT}$ acts as a retransmit enable. A retransmit operation is initiated when $\overline{FL}/\overline{RT}$ is pulsed low. This sets the internal read pointer to the first location and does not affect the write pointer. $\overline{R}$ and $\overline{W}$ must be at a high logic level during the low-level $\overline{FL}/\overline{RT}$ retransmit pulse. Retransmit should be used only when less than 256/512/1024 writes are performed between resets; otherwise, an attempt to retransmit can cause the loss of unread data. The retransmit function can affect $\overline{XO}/\overline{HF}$ depending on the relative locations of the read and write pointers.
GND		Ground
Q0–Q8	O	Data outputs. Q0–Q8 are in the high-impedance state when $\overline{R}$ is high or the FIFO is empty.
$\overline{R}$	I	Read-enable input. A read cycle begins on the falling edge of $\overline{R}$ if $\overline{EF}$ is high. This activates Q0–Q8 and shifts the next data value to this bus. The data outputs return to the high-impedance state as $\overline{R}$ goes high. As the last stored word is read by the falling edge of $\overline{R}$, $\overline{EF}$ transitions low but Q0–Q8 remain active until $\overline{R}$ returns high. When the FIFO is empty, the internal read pointer is unchanged by a pulse on $\overline{R}$.
$\overline{RS}$	I	Reset input. A reset is performed by taking $\overline{RS}$ low. This initializes the internal read and write pointers to the first location and sets $\overline{EF}$ low, $\overline{FF}$ high, and $\overline{HF}$ high. Both $\overline{R}$ and $\overline{W}$ must be held high for a reset during the window shown in Figure 7. A reset is required after power up before a write operation can take place.
V_{CC}		Supply voltage
$\overline{W}$	I	Write-enable input. A write cycle begins on the falling edge of $\overline{W}$ if $\overline{FF}$ is high. The value on D0–D8 is stored in memory as $\overline{W}$ returns high. When the FIFO is full, $\overline{FF}$ is low, inhibiting $\overline{W}$ from performing any operation on the device.
$\overline{XI}$	I	Expansion-in input. $\overline{XI}$ performs two functions. $\overline{XI}$ is tied to ground to indicate that the device is not used in depth expansion. When the device is used in depth expansion, $\overline{XI}$ is connected to the expansion-out ($\overline{XO}$) output of the previous device in the depth-expansion chain.
$\overline{XO}/\overline{HF}$	O	Expansion-out/half-full-flag output. $\overline{XO}/\overline{HF}$ performs two functions. When the device is not used in depth expansion (i.e., when $\overline{XI}$ is tied to ground), $\overline{XO}/\overline{HF}$ indicates when half the memory locations are filled. After half of the memory is filled, the falling edge on $\overline{W}$ for the next write operation drives $\overline{XO}/\overline{HF}$ low. $\overline{XO}/\overline{HF}$ remains low until a rising edge of $\overline{R}$ reduces the number of words stored to exactly half of the total memory. When the device is used in depth expansion, $\overline{XO}/\overline{HF}$ is connected to $\overline{XI}$ of the next device in the daisy chain. $\overline{XO}/\overline{HF}$ drives the daisy chain by sending a pulse to the next device when the previous device reaches the last memory location.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range (any input), V_I . . . . . –0.5 V to 7 V
Continuous output current, I_O . . . . . 50 mA
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{XI}$	2.6			V
		Other inputs	2			
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–2	mA
I_{OL}	Low-level output current				8	mA
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 2 mA		2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.4	V
I_{OZH}	$V_O = V_{CC}$,	$\overline{R} \geq V_{IH}$				±10	µA
I_{OZL}	V_O = 0.4 V,	$\overline{R} \geq V_{IH}$				±10	µA
I_I	V_I = 0 to 5.5 V			–1		1	µA
I_{CC1}‡	t_a = 15 and 25 ns					125¶	mA
	t_a = 35 and 50 ns				50	80	
I_{CC2}‡	t_a = 15 and 25 ns	$\overline{R}$, $\overline{W}$, $\overline{RS}$, and $\overline{FL}/\overline{RT}$ at V_{IH}				15	mA
	t_a = 35 and 50 ns				5	8	
I_{CC3}‡	t_a = 15 and 25 ns	$V_I = V_{CC}$ – 0.2 V				0.5	mA
	t_a = 35 and 50 ns					0.5	
C_i§	V_I = 0,	T_A = 25°C,	f = 1 MHz			8	pF
C_o§	V_O = 0,	T_A = 25°C,	f = 1 MHz			8	pF

‡ I_{CC1} = supply current; I_{CC2} = standby current; I_{CC3} = power-down current. I_{CC} measurements are made with outputs open (only capacitive loading).

§ This parameter is sampled and not 100% tested.

¶ Tested at f_{clock} = 20 MHz

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		FIGURE	′ACT7200L-15 ′ACT7201LA-15 ′ACT7202LA-15		′ACT7200L-25 ′ACT7201LA-25 ′ACT7202LA-25		′ACT7201LA-35† ′ACT7202LA-35†		′ACT7200L-50 ′ACT7201LA-50 ′ACT7202LA-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, $\overline{R}$ or $\overline{W}$			40		28.5		22.2		15	MHz
$t_{c(R)}$	Cycle time, read	1(a)	25		35		45		65		ns
$t_{c(W)}$	Cycle time, write	1(b)	25		35		45		65		ns
$t_{c(RS)}$	Cycle time, reset	7	25		35		45		65		ns
$t_{c(RT)}$	Cycle time, retransmit	4	25		35		45		65		ns
$t_{w(RL)}$	Pulse duration, $\overline{R}$ low	1(a)	15		25		35		50		ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	1(b)	15		25		35		50		ns
$t_{w(RH)}$	Pulse duration, $\overline{R}$ high	1(a)	10		10		10		15		ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	1(b)	10		10		10		15		ns
$t_{w(RT)}$	Pulse duration, $\overline{FL}/\overline{RT}$ low	4	15		25		35		50		ns
$t_{w(RS)}$	Pulse duration, $\overline{RS}$ low	7	15		25		35		50		ns
$t_{w(XIL)}$	Pulse duration, $\overline{XI}$ low	10	15		25		35		50		ns
$t_{w(XIH)}$	Pulse duration, $\overline{XI}$ high	10	10		10		10		10		ns
$t_{su(D)}$	Setup time, data before $\overline{W}\uparrow$	1(b), 6	11		15		18		30		ns
$t_{su(RT)}$	Setup time, $\overline{R}$ and $\overline{W}$ high before $\overline{FL}/\overline{RT}\uparrow$‡	4	15		25		35		50		ns
$t_{su(RS)}$	Setup time, $\overline{R}$ and $\overline{W}$ high before $\overline{RS}\uparrow$‡	7	15		25		35		50		ns
$t_{su(XI-R)}$	Setup time, $\overline{XI}$ low before $\overline{R}\downarrow$	10	10		10		10		15		ns
$t_{su(XI-W)}$	Setup time, $\overline{XI}$ low before $\overline{W}\downarrow$	10	10		10		10		15		ns
$t_{h(D)}$	Hold time, data after $\overline{W}\uparrow$	1(b), 6	0		0		0		5		ns
$t_{h(E-R)}$	Hold time, $\overline{R}$ low after $\overline{EF}\uparrow$	5, 11	15		25		35		50		ns
$t_{h(F-W)}$	Hold time, $\overline{W}$ low after $\overline{FF}\uparrow$	6, 12	15		25		35		50		ns
$t_{h(RT)}$	Hold time, $\overline{R}$ and $\overline{W}$ high after $\overline{FL}/\overline{RT}\uparrow$	4	10		10		10		15		ns
$t_{h(RS)}$	Hold time, $\overline{R}$ and $\overline{W}$ high after $\overline{RS}\uparrow$	7	10		10		10		15		ns

† Released in RJ package only
‡ These values are characterized but not currently tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 13)

PARAMETER		FIGURE	′ACT7200L-15 ′ACT7201LA-15 ′ACT7202LA-15		′ACT7200L-25 ′ACT7201LA-25 ′ACT7202LA-25		′ACT7201LA-35† ′ACT7202LA-35†		′ACT7200L-50 ′ACT7201LA-50 ′ACT7202LA-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_a	Access time, $\overline{R}\downarrow$ or $\overline{EF}\uparrow$ to data out valid	1(a), 3, 5		15		25		35		50	ns
$t_{v(RH)}$	Valid time, data out valid after $\overline{R}\uparrow$	1(a)	5		5		5		5		ns
$t_{en(R\text{-}QX)}$	Enable time, $\overline{R}\downarrow$ to Q outputs at low impedance‡	1(a)	5		5		10		10		ns
$t_{en(W\text{-}QX)}$	Enable time, $\overline{W}\uparrow$ to Q outputs at low impedance‡§	5	5		5		5		15		ns
$t_{dis(R)}$	Disable time, $\overline{R}\uparrow$ to Q outputs at high impedance‡	1(a)		15		18		20		30	ns
$t_{w(FH)}$	Pulse duration, $\overline{FF}$ high in automatic write mode	6		15		25		30		45	ns
$t_{w(EH)}$	Pulse duration, $\overline{EF}$ high in automatic read mode	5		15		25		30		45	ns
$t_{pd(W\text{-}F)}$	Propagation delay time, $\overline{W}\downarrow$ to $\overline{FF}$ low	2		15		25		30		45	ns
$t_{pd(R\text{-}F)}$	Propagation delay time, $\overline{R}\uparrow$ to $\overline{FF}$ high	2, 6, 12		15		25		30		45	ns
$t_{pd(RS\text{-}F)}$	Propagation delay time, $\overline{RS}\downarrow$ to $\overline{FF}$ high	7		25		35		45		65	ns
$t_{pd(RS\text{-}HF)}$	Propagation delay time, $\overline{RS}\downarrow$ to $\overline{XO}/\overline{HF}$ high	7		25		35		45		65	ns
$t_{pd(W\text{-}E)}$	Propagation delay time, $\overline{W}\uparrow$ to $\overline{EF}$ high	3, 5, 11		15		25		30		45	ns
$t_{pd(R\text{-}E)}$	Propagation delay time, $\overline{R}\downarrow$ to $\overline{EF}$ low	3		15		25		30		45	ns
$t_{pd(RS\text{-}E)}$	Propagation delay time, $\overline{RS}\downarrow$ to $\overline{EF}$ low	7		25		35		45		65	ns
$t_{pd(W\text{-}HF)}$	Propagation delay time, $\overline{W}\downarrow$ to $\overline{XO}/\overline{HF}$ low	8		25		35		45		65	ns
$t_{pd(R\text{-}HF)}$	Propagation delay time, $\overline{R}\uparrow$ to $\overline{XO}/\overline{HF}$ high	8		25		35		45		65	ns
$t_{pd(R\text{-}XOL)}$	Propagation delay time, $\overline{R}\downarrow$ to $\overline{XO}/\overline{HF}$ low	9		15		25		35		50	ns
$t_{pd(W\text{-}XOL)}$	Propagation delay time, $\overline{W}\downarrow$ to $\overline{XO}/\overline{HF}$ low	9		15		25		35		50	ns
$t_{pd(R\text{-}XOH)}$	Propagation delay time, $\overline{R}\uparrow$ to $\overline{XO}/\overline{HF}$ high	9		15		25		35		50	ns
$t_{pd(W\text{-}XOH)}$	Propagation delay time, $\overline{W}\uparrow$ to $\overline{XO}/\overline{HF}$ high	9		15		25		35		50	ns
$t_{pd(RT\text{-}FL)}$	Propagation delay time, $\overline{FL}/\overline{RT}\downarrow$ to $\overline{HF}$, $\overline{EF}$, $\overline{FF}$ valid	4		25		35		45		65	ns

† Released in RJ package only
‡ These values are characterized but not currently tested.
§ Only applies when data is automatically read (see Figure 5)

PARAMETER MEASUREMENT INFORMATION

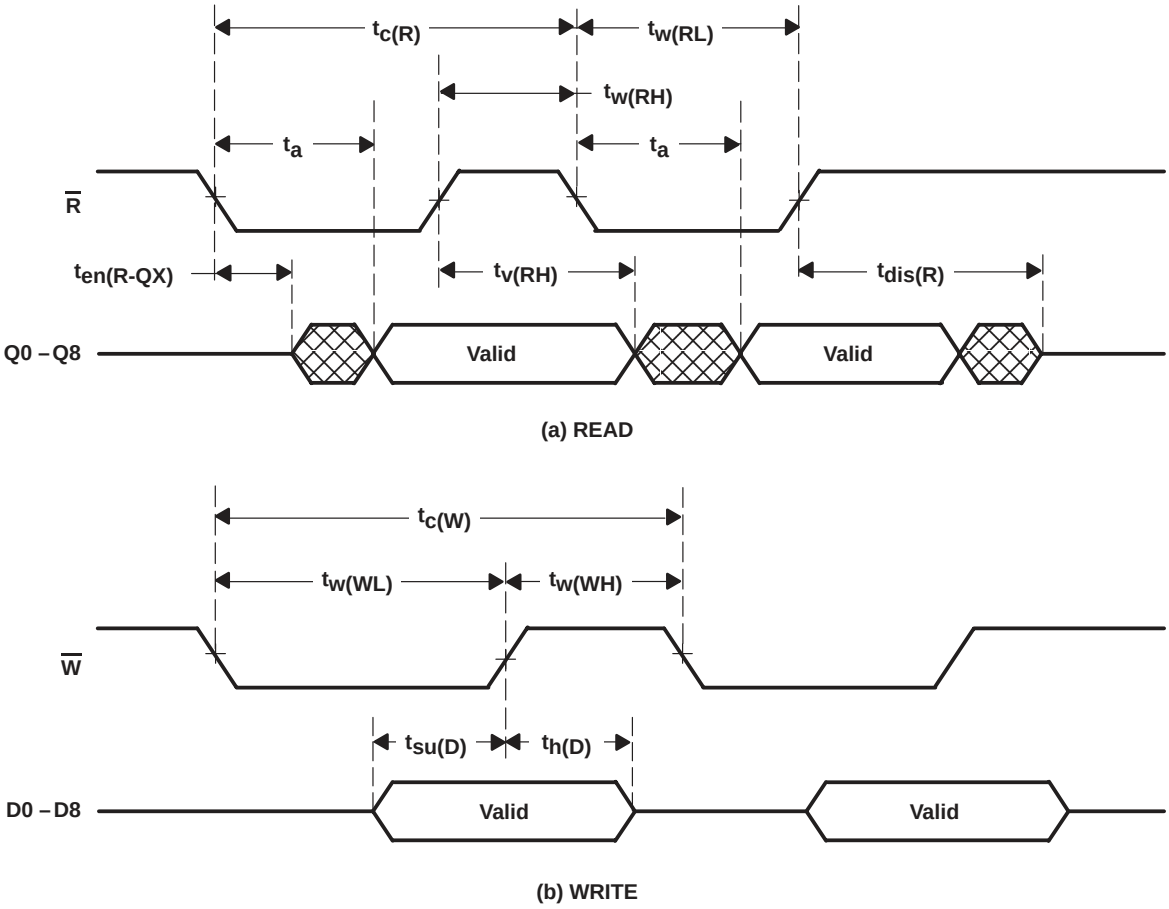


Figure 1. Asynchronous Waveforms

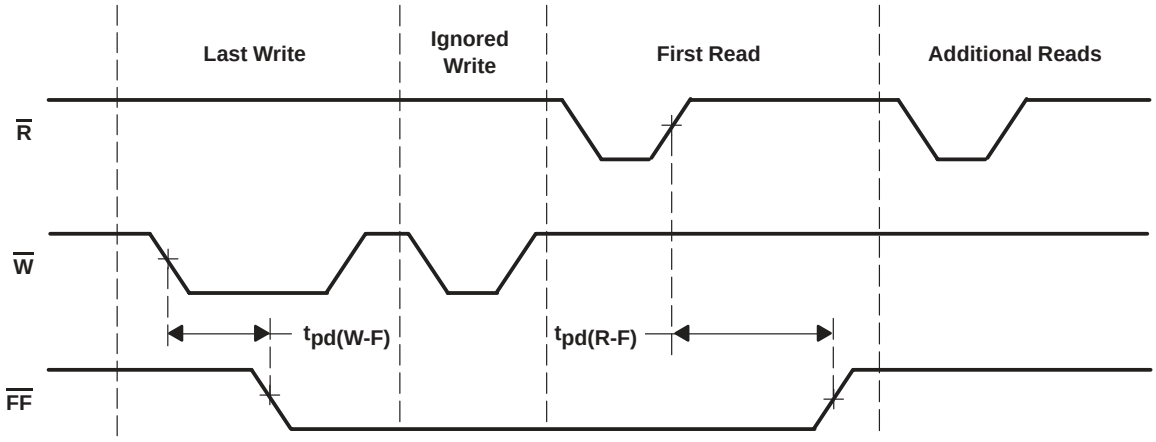


Figure 2. Full-Flag Waveforms

PARAMETER MEASUREMENT INFORMATION

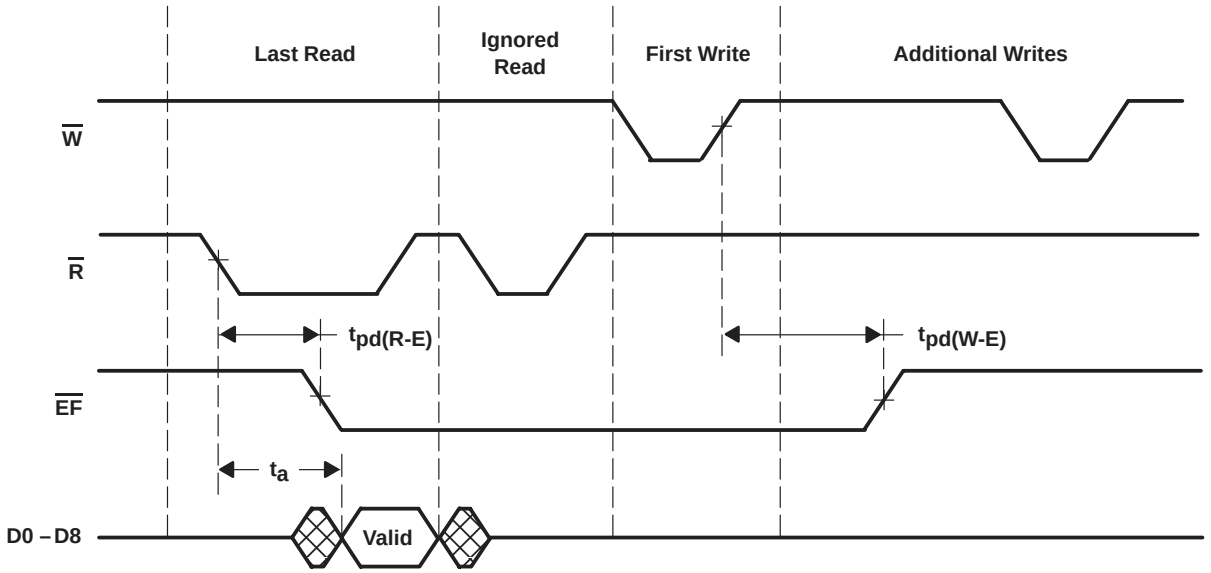
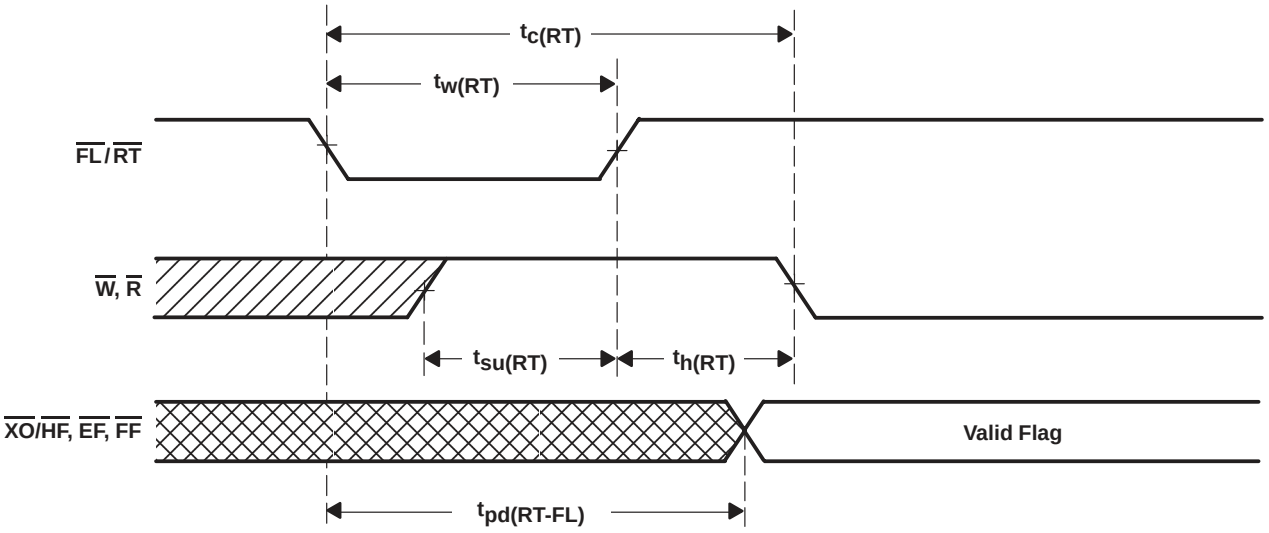


Figure 3. Empty-Flag Waveforms



NOTE A: The EF, FF, and XO/HF status flags are valid after completion of the retransmit cycle.

Figure 4. Retransmit Waveforms

PARAMETER MEASUREMENT INFORMATION

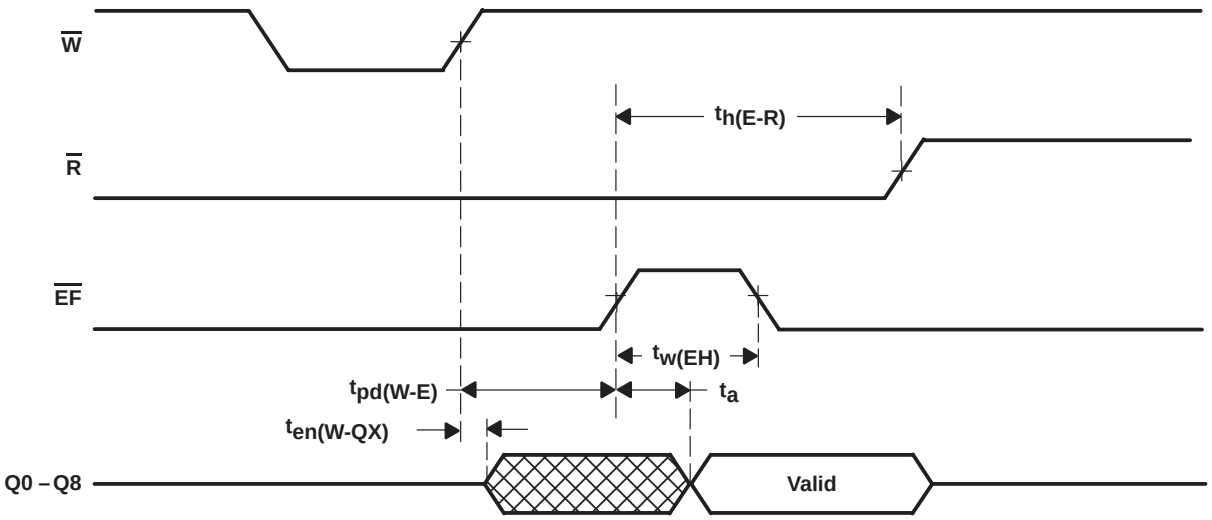


Figure 5. Automatic-Read Waveforms

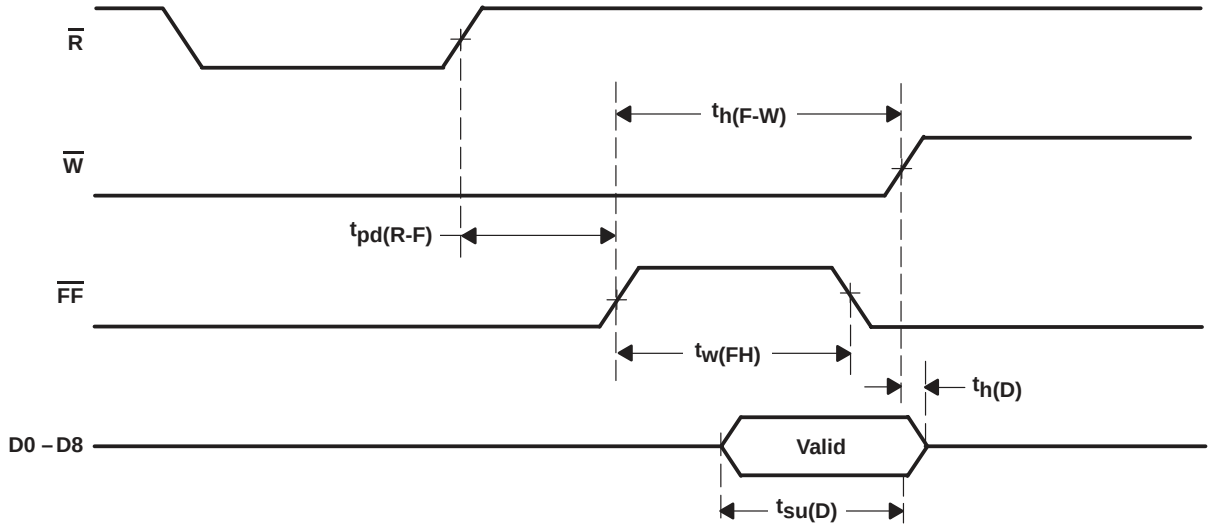


Figure 6. Automatic-Write Waveforms

PARAMETER MEASUREMENT INFORMATION

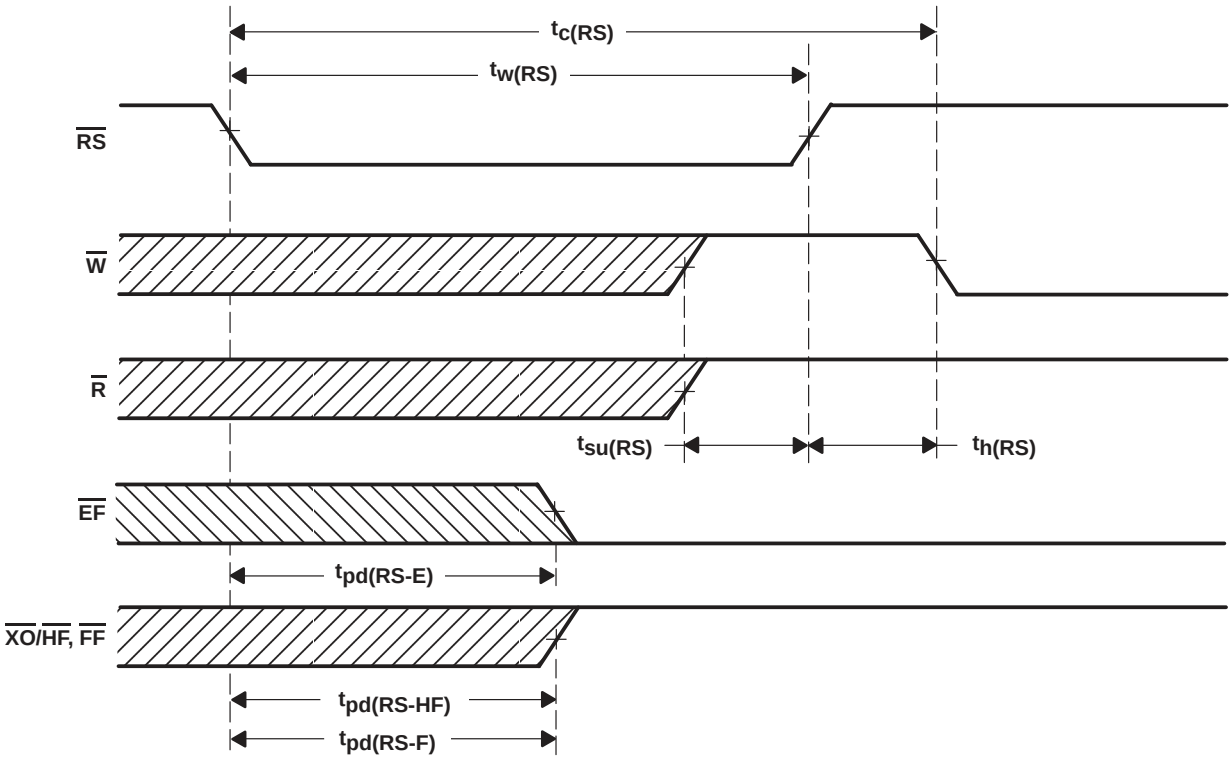


Figure 7. Master-Reset Waveforms

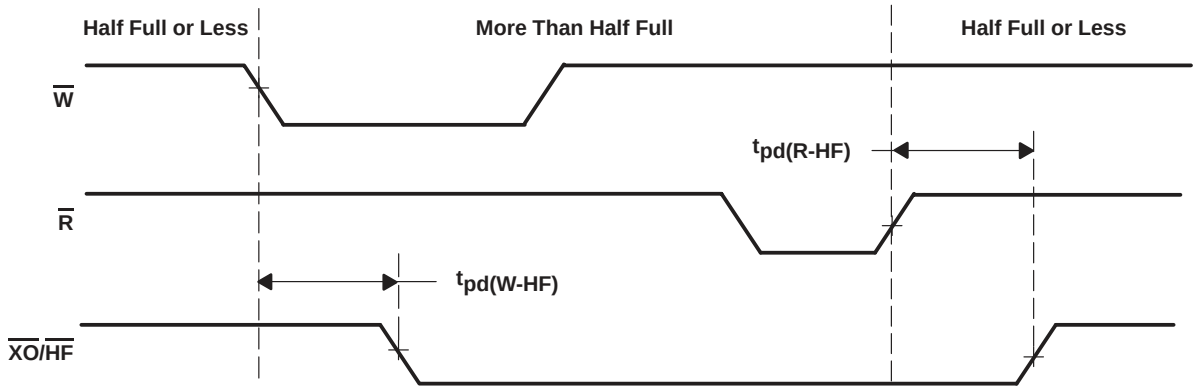


Figure 8. Half-Full Flag Waveforms

PARAMETER MEASUREMENT INFORMATION

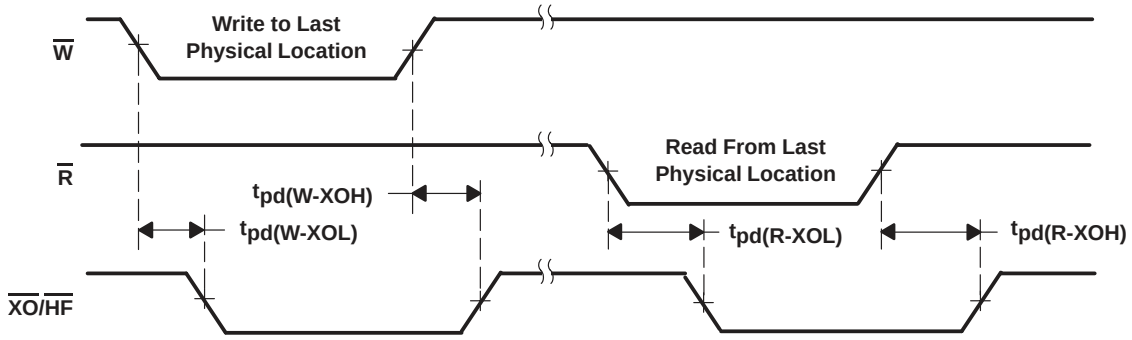


Figure 9. Expansion-Out Waveforms

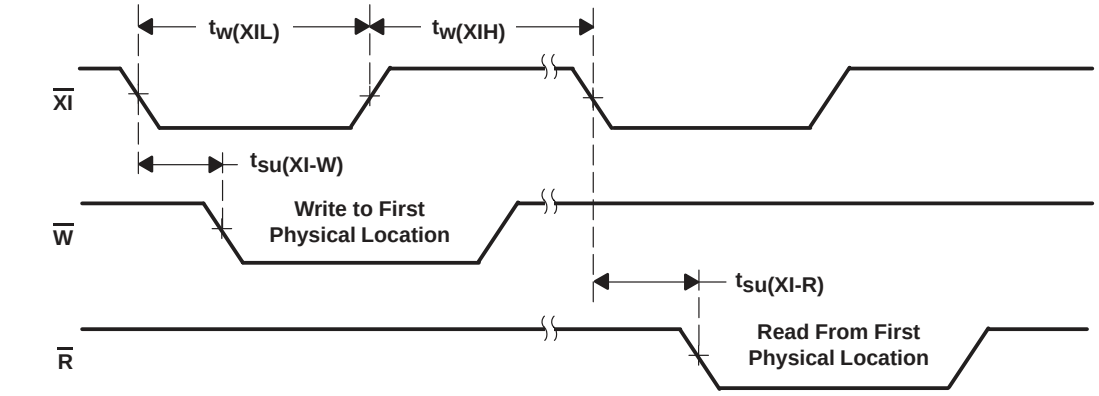


Figure 10. Expansion-In Waveforms

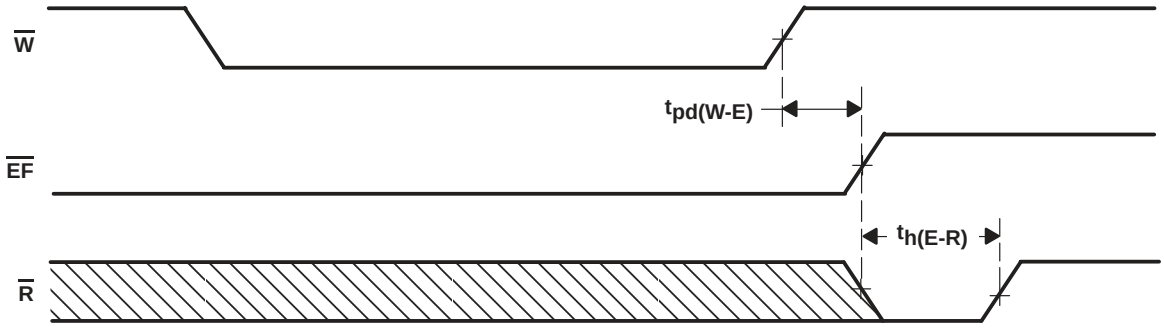


Figure 11. Minimum Timing for an Empty-Flag Coincident-Read Pulse

PARAMETER MEASUREMENT INFORMATION

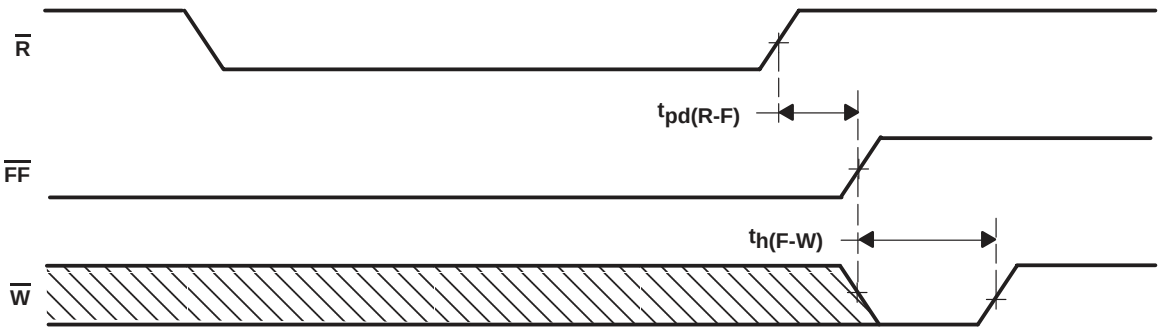
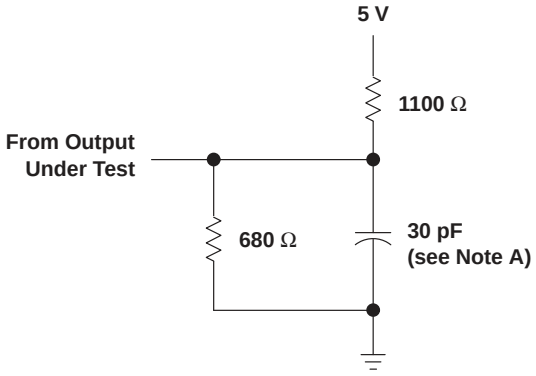
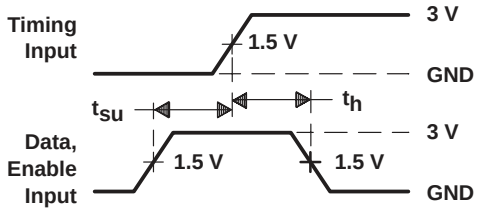


Figure 12. Minimum Timing for a Full-Flag Coincident-Write Pulse

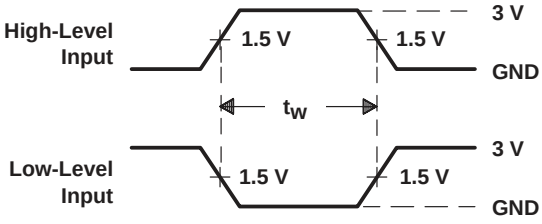
PARAMETER MEASUREMENT INFORMATION



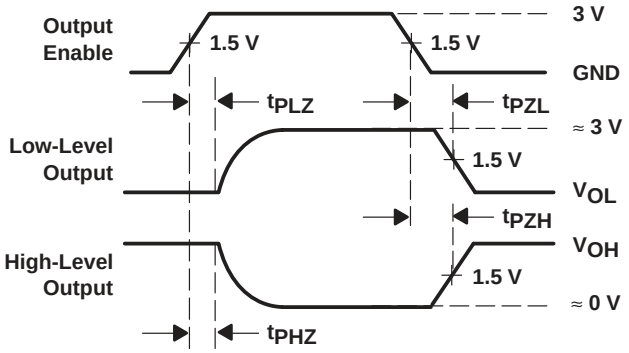
LOAD CIRCUIT



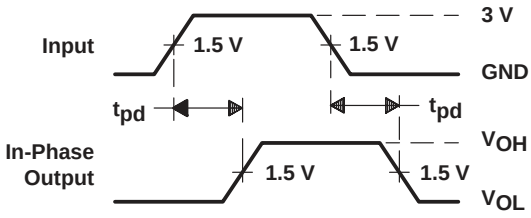
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE A: Includes probe and jig capacitance

Figure 13. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Combining two or more devices to create one FIFO with a greater number of memory bits is accomplished in two different ways. Width expansion increases the number of bits in each word by connecting FIFOs with the same depth in parallel. Depth expansion uses the built-in expansion logic to daisy-chain two or more devices for applications requiring more than 256, 512, or 1024 words of storage. Width expansion and depth expansion can be used together.

width expansion

Word-width expansion is achieved by connecting the corresponding input control to multiple devices with the same depth. Status flags ($\overline{EF}$, $\overline{FF}$, and $\overline{HF}$) can be monitored from any one device. Figure 14 shows two FIFOs in a width-expansion configuration. Both devices have their expansion-in ($\overline{XI}$) inputs tied to ground. This disables the depth-expansion function of the device, allowing the first-load/retransmit ($\overline{FL}/\overline{RT}$) input to function as a retransmit ($\overline{RT}$) input and the expansion-out/half-full ($\overline{XO}/\overline{HF}$) output to function as a half-full ($\overline{HF}$) flag.

depth expansion

The SN74ACT7200L/7201LA/7202LA is easily expanded in depth. Figure 15 shows the connections used to depth expand three SN74ACT7200L/7201LA/7202LA devices. Any depth can be attained by adding additional devices to the chain. The SN74ACT7200L/7201LA/7202LA operates in depth expansion under the following conditions:

- The first device in the chain is designated by tying $\overline{FL}$ to ground.
- All other devices must have their $\overline{FL}$ inputs at a high logic level.
- $\overline{XO}$ of each device must be tied to $\overline{XI}$ of the next device.
- External logic is needed to generate a composite $\overline{FF}$ and $\overline{EF}$. All $\overline{FF}$ outputs must be ORed together and all $\overline{EF}$ outputs must be ORed together.
- $\overline{RT}$ and $\overline{HF}$ functions are not available in the depth-expanded configuration.

combined depth and width expansion

Both expansion techniques can be used together to increase depth and width. This is done by first creating depth-expanded units and then connecting them in a width-expanded configuration (see Figure 16).

APPLICATION INFORMATION

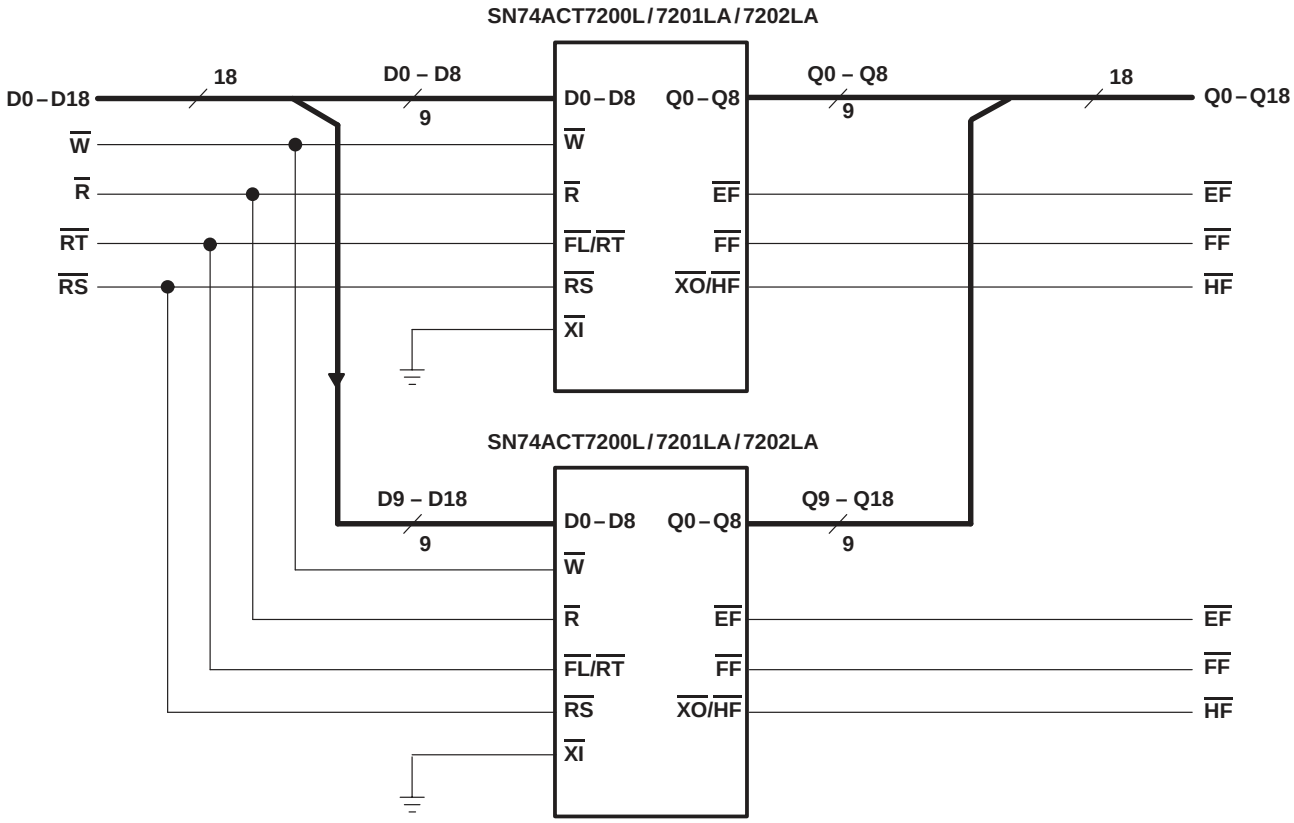


Figure 14. Word-Width Expansion: 256/512/1024 Words × 18 Bits

APPLICATION INFORMATION

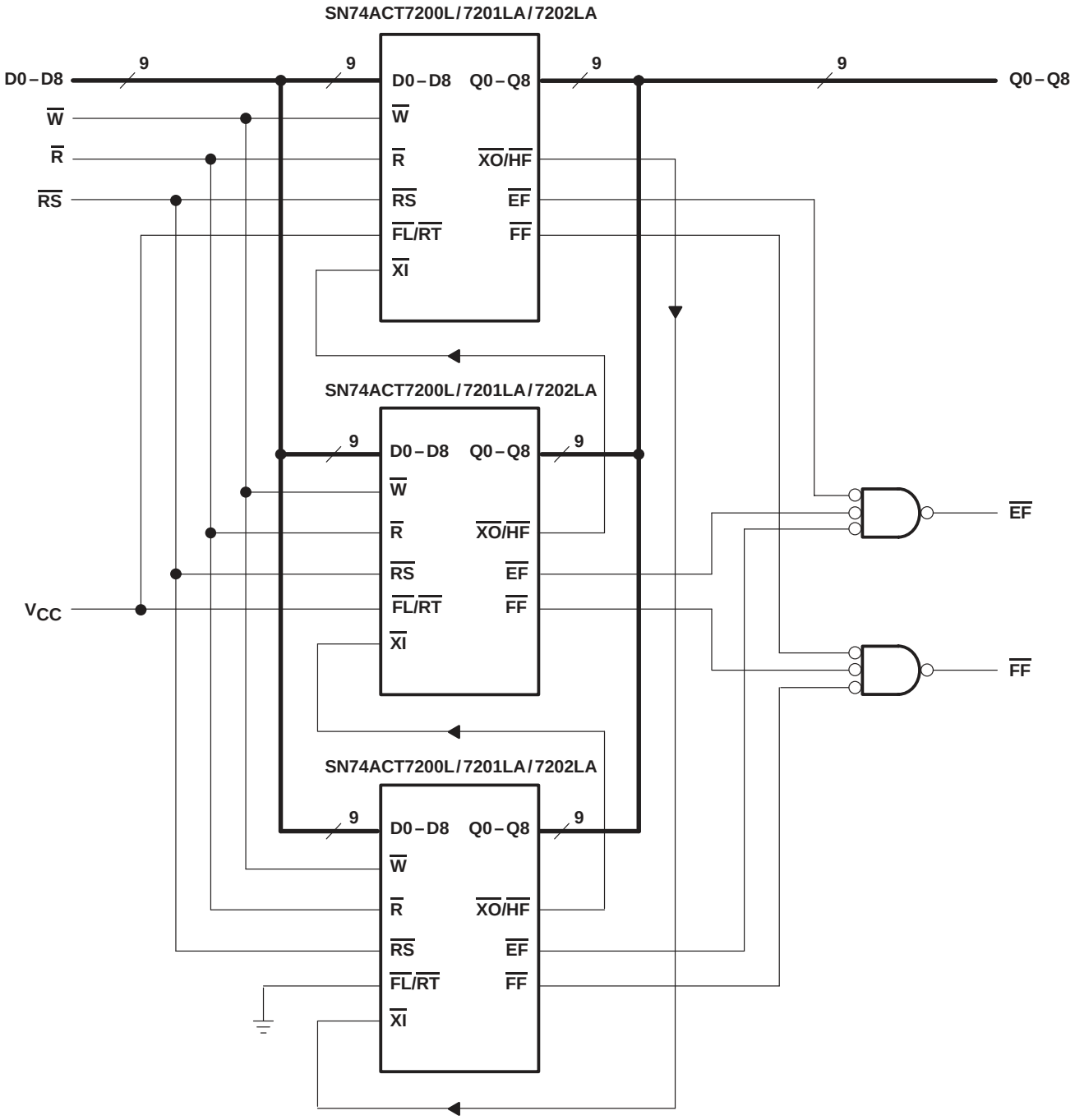


Figure 15. Word-Depth Expansion: 768/1536/3072 Words × 9 Bits

APPLICATION INFORMATION

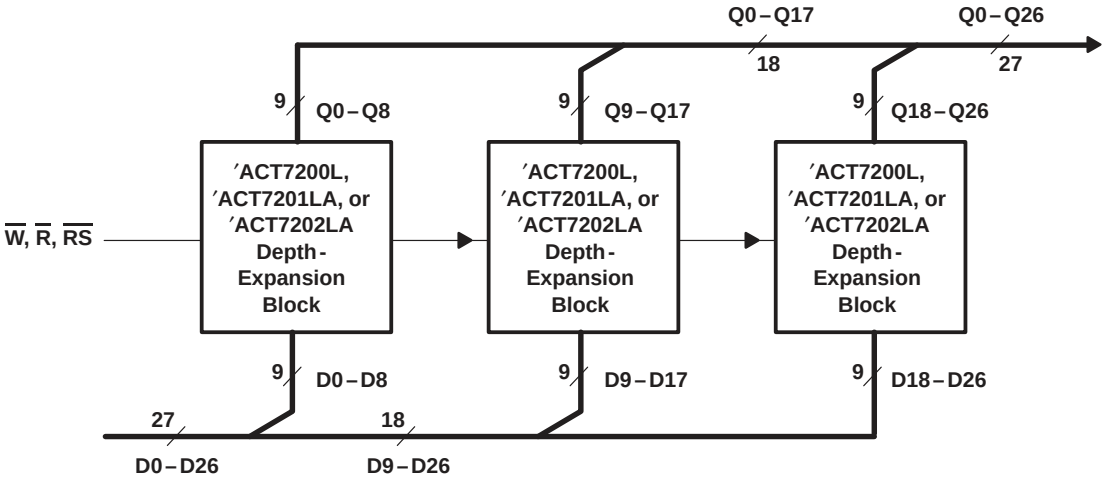


Figure 16. Word-Depth Plus Word-Width Expansion

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74ACT7200L15DV	OBSOLETE	SOP	DV	28		TBD	Call TI	Call TI
SN74ACT7200L15NP	OBSOLETE	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7200L15RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7200L20DV	OBSOLETE	SOP	DV	28		TBD	Call TI	Call TI
SN74ACT7200L20NP	OBSOLETE	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7200L20RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7200L25DV	OBSOLETE	SOP	DV	28		TBD	Call TI	Call TI
SN74ACT7200L25NP	OBSOLETE	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7200L25RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7200L35DV	OBSOLETE	SOP	DV	28		TBD	Call TI	Call TI
SN74ACT7200L35NP	OBSOLETE	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7200L35RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7200L50DV	OBSOLETE	SOP	DV	28		TBD	Call TI	Call TI
SN74ACT7200L50NP	OBSOLETE	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7200L50RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7201LA15DV	OBSOLETE	SOP	DV	28		TBD	Call TI	Call TI
SN74ACT7201LA15NP	OBSOLETE	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7201LA15RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7201LA20DV	OBSOLETE	SOP	DV	28		TBD	Call TI	Call TI
SN74ACT7201LA20NP	OBSOLETE	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7201LA20RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7201LA25DV	OBSOLETE	SOP	DV	28		TBD	Call TI	Call TI
SN74ACT7201LA25NP	OBSOLETE	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7201LA25RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7201LA35DV	OBSOLETE	SOP	DV	28		TBD	Call TI	Call TI
SN74ACT7201LA35NP	OBSOLETE	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7201LA35RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7201LA50DV	OBSOLETE	SOP	DV	28		TBD	Call TI	Call TI
SN74ACT7201LA50NP	OBSOLETE	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7201LA50RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7202LA15DV	OBSOLETE	SOP	DV	28		TBD	Call TI	Call TI
SN74ACT7202LA15NP	OBSOLETE	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7202LA15RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7202LA25DV	OBSOLETE	SOP	DV	28		TBD	Call TI	Call TI
SN74ACT7202LA25NP	OBSOLETE	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7202LA25RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7202LA35RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7202LA35RJR	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7202LA50DV	OBSOLETE	SOP	DV	28		TBD	Call TI	Call TI
SN74ACT7202LA50NP	OBSOLETE	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7202LA50RJ	OBSOLETE	PLCC	RJ	32		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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