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Evaluating the ADF5902 24 GHz, ISM Band, Multichannel FMCW Radar Transmitter

FEATURES

Self contained board, including the ADF5902 24 GHz VCO PGA, with integrated 2-channel PA output and fractional-N frequency synthesizer with ramp generation

Windows-based software allows control of the ADF5902 functions from a PC

Externally powered by a 5 V power supply

EVALUATION KIT CONTENTS

EV-ADF5902SD1Z evaluation board

EQUIPMENT NEEDED

PC with Windows XP (or more recent version) and USB port for evaluation software Analog Devices, Inc., EVAL-SDP-CS1Z SDP-S controller board Spectrum analyzer 5 V power supply

DOCUMENTS NEEDED

ADF5902 data sheet PLL Software Installation Guide

SOFTWARE NEEDED

PLL software

GENERAL DESCRIPTION

The EV-ADF5902SD1Z evaluation board allows the user to evaluate the performance of the ADF5902 24 GHz voltage controlled oscillator (VCO) programmable gain amplifier (PGA) with a 2-channel power amplifier (PA) output and ramping phaselocked loop (PLL). Figure 1 shows the EV-ADF5902SD1Z evaluation board, which contains the ADF5902, three high frequency K type Subminiature Version A (SMA) connectors for the local oscillator (LO) output, two transceiver outputs, banana connectors for the power supply, and a connector for the serial interface.

The EV-ADF5902SD1Z evaluation board requires an EVAL-SDP-CS1Z system demonstration platform serial (SDP-S) controller board, which the kit does not include. The EVAL-SDP-CS1Z SDP-S allows software programming of the ADF5902 device.

Full specifications on the ADF5902 are available in the ADF5902 data sheet. Consult the data sheet in conjunction with this user guide when working with the EV-ADF5902SDIZ evaluation board.

The Windows[®]-based PLL software provides easy programming of the synthesizer.



EVALUATION BOARD PHOTOGRAPH

Figure 1.

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REVISION HISTORY

12/2018—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The EV-ADF5902SD1Z evaluation board requires the use of an EVAL-SDP-CS1Z SDP-S controller board to program the device. Purchase the EVAL-SDP-CS1Z SDP-S separately because it is not included in the evaluation kit. See the Evaluation Board Schematics and Artwork section for the detailed schematics (Figure 6 to Figure 12) and layout (Figure 13 and Figure 14) of the EV-ADF5902SD1Z evaluation board.

POWER SUPPLIES

The EV-ADF5902SD1Z evaluation board is powered by a 5 V external power supply that must be connected as described in the Evaluation Board Test section.

INPUT SIGNALS

The 100 MHz temperature controlled crystal oscillator (TCXO), or an external REF input, provides the necessary reference signal. Either are acceptable to use.

Connect an external TX_DATA signal to the TPI test point to control some of the ramping functionality. Use the external REF input synchronized to TX_DATA when using the TX_DATA signal. Remove Resistor R40 when using an external REF input.

OUTPUT SIGNALS

The TX1, TX2, and LO outputs from the ADF5902 contain dc bias voltages, and are available on the J8 (TXOUT1), J9 (TXOUT2), and J4 (LOOUT) output SMAs.

DEFAULT OPERATION

All hardware components necessary to operate the ADF5902 are included on the EV-ADF5902SD1Z.

EVALUATION BOARD TESTING

To evaluate and test the performance of the ADF5902, use the following procedure and reference Figure 2 throughout the process:

- 1. Install the PLL software (see the PLL Software Installation Guide)
- 2. Follow the hardware driver installation procedure (see the PLL software Installation Guide for Windows XP only).
- 3. Connect the EVAL-SDP-CS1Z SDP-S board to the EV-ADF5902SD1Z evaluation board.
- 4. Connect the 5 V power supply to the red and black banana connectors of the EV-ADF5902SD1Z evaluation board.
- 5. Connect the USB cable from the EVAL-SDP-CS1Z SDP-S board to the PC.

- 6. Connect an ac-coupled signal source analyzer to the Transmitter 2 J9 output SMA.
- 7. Run the PLL software.
- 8. Click the **Select Device and Connection** tab in the PLL software window. Select **SDP board (black)**, the ADF5902 device, and click **Connect** (see Figure 3).
- 9. Click the **ADF5902 Controls** tab, and then click **Initialize ADF5902** in the bottom right corner of the window (see Figure 4).
- 10. Measure the TXOUT2 output signal on the J9 output SMA using the spectrum analyzer.



Choose a device to evaluate	
Choose a device to evaluate	
ADF5902 DSB board (green) O SDI Connect	² board (plack)
44-43: Application started. 44-55: Attempting SDP connection 44-55: Rashing LED. 45-75: CRB server at al	ANALOG

Figure 3. PLL Software Front Panel Display, Select Device and Connection

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EVALUATION BOARD SOFTWARE ADF5902 CONTROLS

Click the **ADF5902 Controls** tab in the PLL software window (see Figure 4) to select the user configurable register settings. Consult the register descriptions of the ADF5902 data sheet for details. Default settings are recommended for most registers.

After powering up the board, click the **Initialize ADF5902** box in the bottom right of the PLL software window to perform the initialization sequence (as described in the ADF5902 data sheet). Following this sequence, the ADF5902 transmitter powers up and all ADF5902 blocks calibrate.

The **ADF5902 Controls** tab allows access to the **PLL Setup** tab and the **Ramp Generation** tab.

PLL SETUP

To configure the PLL functionality of the ADF5902, take the following steps:

1. In the **PLL Setup** tab (see Figure 4), set the reference frequency (RF) settings for the PLL in the **RF Settings** section, and the required settings for the TX2, TX1, and LO outputs in the **Register 0** section.

- In the RF Settings section, type the reference frequency in the Reference Frequency box. The PFD frequency is calculated from the Reference Frequency value, the R counter value, the Ref Doubler (reference doubler option), and the Ref/2 (reference divided by 2 option).
- 3. Ensure that the value in the **PFD Frequency** box matches the value specified when designing the loop filter for the ADF5902.
- 4. Program the charge pump setting in the **Register 12** section to match the loop filter design by clicking the **Charge Pump Setting** dropdown menu and selecting a value.
- 5. Click the **Muxout** dropdown menu in the **Register 3** section, and then select the signal connected to the output of the MUXOUT pin.

To program any of the ADF5902 registers, click the button under each register value in the **Registers** section at the bottom of Figure 4 to write that value to the device. For example, to write the value for Register R0, click the **Write R0** button.

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A green background of a register value indicates that the register value has changed in the **PLL Setup** tab, and that a write of this register to the device is required.

Analog Devices	ADF5	902 Software															-	
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ect Device and Cor	nnecti	on ADF5902 (Contro	Is Other Funct	ons													
PLL Setup Ramo G	Sener	ation		****														
RF Settings	Jenen	auuri				Register 0				Re	gister 2			F	Register	11		
VCO Fre	quen	by: 24	1025	MHz	•	TX2 Amp C	al: N	lomal operation		~	ADC Star	t: Normal op	eratio	n ~	Counter	s: Normal Op	eration	~
Reference Fre	quen	cy: 100		MHz		TX1 Amp C	al: 1	lomal operation		~ AD	IC average	s: 1		~	SD Rese	t: 0. Enabled	~	
R counter: 1	\sim	Ref Double	er:] Ref /2:		PUP VO	0: F	owered on		~ AD	C CLK Div	8	50	F F	Register	12		
PFD Free	quenc	y: 100	100 MHz			VCO Amp C	al: N	Normal operation		~ Re	rister 3				Charge	Pump Setting:	2.24	∼ mA
Channel s	spacin	ig: 2.3002322	36/63	0312 HZ		PUP AD	C: F	owered on	~	~	9000 0	page o				ump in-state:	U. Disab	ed Y
FF	RAC		1000			PUP TX	2 0	DN .		~	Muxout:	3-state output	đ.	~				
(120 + 419	4304	PFD Cal. (1 -)x 100	MHz) x 2	VCO (MH = 24025	z)	PUP TX	(1: 0	DEE		~	10 Level:	3.3 V	~					
N = 120.125	OD				PUP L	PUP LO: ON 🗸			~ Free	quency Re	adback: R	un Fre	aq Check					
Register 4	Register 4			Register 1				Loci	Locked Frequency:									
Ramp Status/ Analog Test Bus: Ramp Down to MUXOUT 🗸				Tx Amp Cal Code: 255				Readback:										
						Register 7				000	0000 None			~				
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legisters																		
x 801FE5A0	0x	20642	0x	2004	0x	6	0x	40003E88	0x	1D32A64	4A Ox	4F0000	0	12038EE	0x	10	1	1055005
Write R0	11 8	Write R2		Write R4	1 3	Write R6		Write R8		Write R10	1	Vrite R12	1	Write R14	W	hte R16	Initialia	e ADF5902
x FFF7FFE1	0x	1890803	0x	F04005	0x	100A027	0x	2800B929	0x	110	0B 0x	180500	0	120F			Re	calibrate
Write R1	0.0	Write R3		Write R5		Write R7		Write R9		Write R11	1	Vrite R13		Write R15			Ă	DF5902
44:48: Application s 44:55: Attempting S 44:55: Flashing LEE 44:57: SDP connect	tarted DP o D. ted.	l. onnection						*			Softw	are version: 0.	.1.7		I			G
P board connect	ed. U	sing connecto	A		-		_											

Figure 4. PLL Software Window Display, ADF5902 Controls

RAMP GENERATION

To configure the ramp functionality of the ADF5902,

- 1. Click the **Ramp Generation** tab in the PLL software window (see Figure 5).
- 2. Select the ramp type from the **Ramp mode** dropdown menu in the **Modulation Type** section, and set the various ramp parameters in the **CLK1**, **Slope 0**, **Slope 1**, **Slope 2**, **Slope 3**, and **Timing Parameters** sections.

Figure 5 shows an example of the ramping settings for a continuous triangular ramp of 144 ramp steps over 200 MHz at the ADF5902 transceiver output, with a ramp time of 5 ms. For 200 MHz, the PLL is programmed for a 100 MHz ramp because the feedback to the PLL is divided by two.

3. After each parameter is set in the PLL software, write it to the device by clicking the corresponding register write button.

Analog Devic	es ADF5	902 Software														. <u>-</u> 0 8	
ile Tools	Help																
lect Device and	Connecti	on ADF5902	Controls	S Other Funct	ions												
LL Setup Ran	p Gener	ation															
Ramping and S	hift-Keyin	g															
Modulation Ty	pe			Slope 0)	Slop	e 1		Slope 2		Slope	3		Timing Pa	arameters		
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Pamo mode:	Casting	aug beingen der		DEV:	455 🜩	DE	V: -7280		DEV:	455	DEV	- [-7280 🜲	CLK2_0:	10 💠	Ramp (us):	144.0
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Single Full In:	Disable	d ~		Steps	144	Ste	os: 91	.1	Steps:	144	step		9	CLK2_2:	10 0	Ramp (us):	144.0
CLK1:		10 🔤						54			nd	10 L		CLK2 3	10	Ramp (us):	9.000
Other				Output		Out	put		Output		Outp	ut		-	1.5.4		
Charma Di	ma Callin	2.24		Freq ste	ep (kHz): 594.274	Freq	step (kHz): -11,	108	Freq step (kH	z): 694	.2/4 Freq s	tep (kHz): -11,108	Delays			
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			Pecieta	e 12									Delay	(us):	0.0	00	
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TXdata					and the second se				Delay 1			~	ewy 5	Delt	av 1.	0.4	
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TYPUT								1						Dea	ay Z:	U	
IX Data Ingg	er: 0, D	sable ~		Chip En	able			/	· · · · ·		/			Dek	sy 3:	0 🜩	
				Chip Ena	ible: High \sim		Delay 0			Delay i			1				
TXdata inv	rt: 0.N	ot inverted ~		1	Send												
	1000																
Registers																	
x 801FE5A	0 0x	20642	0x	2004	0x	6 0x	40003E88	0x	1D32A64A	0x	4F000C	0x	12038EE	0x	10		
Write R0		Write R2	1 2	Write R4	Write R6		Write R8		Write R10	W	hte R12		Write R14	Write	R16	Initialize	ADF590
x FFF7FFE	1 0x	1890803	0x	F04005	0x 100A02	7 0x	2800B929	0x	110B	0x	18050D	0x	120F			Reca	librata
Write R1		Write R3		Write R5	Write R7		Write R9		Write R11	W	nte R13		Write R15			ADF	5902
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Figure 5. PLL Software Window Display, ADF5902 Ramps Generation

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Figure 6. EV-ADF5902SD1Z Evaluation Board Schematic (Page 1)



Figure 7. EV-ADF5902SD1Z Evaluation Board Schematic (Page 2)



Figure 8. EV-ADF5902SD1Z Evaluation Board Schematic (Page 3)



Figure 9. EV-ADF5902SD1Z Evaluation Board Schematic (Page 4)





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Figure 11. EV-ADF5902SD1Z Evaluation Board Schematic (Page 6)



Figure 12. EV-ADF5902SD1Z Evaluation Board Schematic (Page 7)

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Figure 13. EV-ADF5902SD1Z Evaluation Board Layer 1 Top Side



Figure 14. EV-ADF5902SD1Z Evaluation Board Layer 4 Bottom Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 1. Bill of Materials

interest in the second se	turer Part Number
2 C1, C2 1 nF, 0603 capacitors Murata	GRM1885C1H102JA01D
1 C12 220 pF, 0805 capacitor Phycomp	(Yageo) CC0805JRNPO9BN221
4 C15, C22, C27, C127 100 nF, 0603 capacitors AVX	06035C104KAT2A
4 C18, C24, C29, C129 1 nF, 0402 capacitors MurataA	GRM1555C1H102JA01
1 C13 3.3 nF, 0805 capacitor TDK	C2012C0G1H332J
4 C21, C26, C31, C131 10 pF, 0402 capacitors Phycomp	(Yageo) CC0402JRNP09BN100
1 C14 100 pF, 0805 capacitor Yageo	CC0805FRNPO9BN101
1 C16 47 nF, 0402 capacitor AVX	0402YD473KAT2A
1 C23 220 nF, 0402 capacitor TDK	C1005X5R0J224K
1 C28 220 nF, 0603 capacitor Murata	GCM188R71H224KA64D
4 C32, C34, C36, C38 1 μF, 0805 capacitors Murata	GRM21BR71H105KA12L
1 C40 22 μF, 0805 capacitor Taiyo Yud	len LMK212BJ226MG-T
1 C41 10 pF, 0603 capacitor Murata	GRM1885C1H100JA01D
1 D1 Diode, standard, 1 A, 50 V ON Semio	conductor 1N4001G
1 D2 Diode, Schottky, 0.5 A, 20 V ON Semic	conductor MBR0520LT1G
1 E1 Ferrite bead Wurth Ele	ektronik 7427-92642
2 J1, J7 Connector PCB end launch jack Cinch	142-0701-851
3 J4, J8, J9 Connector PCB SMA right angle Rosenber jack	rger 02K243-40M
1 J5 Connector PCB vertical type Hirose receptable SMD	FX8-120S-SV(21)
1 P2 Connector PCB single socket black Deltron	571-0100
1 P3 Connector PCB single socket red Deltron	571-0500
10 R1, R3, R8 to R10, R40, R45, R50, R55, 0 Ω, 0603 resistors Multicom R56	MC0603WG00000T5E-TC
4 R46 to R49 330 Ω, 0603 resistors Multicom	MC 0.063W 0603 330R
1 R14 Do not install Do not in	stall Do not install
1 R18 510 Ω, 0805 resistor Yageo	RC0805JR-07510RL
1 R19 1 kΩ, 0805 resistor Panasoni	c ERJ-6ENF1001V
6 R2, R23, R25, R27, R29, R33 0 Ω, 0402 resistors Panasoni	c ERJ-2GE0R00X
1 R20 0 Ω, 0805 resistor Panasoni	c ERJ-6GEY0R00V
1 R22 5.1 kΩ, 0603 resistor BOURNS	CR0603-FX-5101ELF
2 R35, R36 100 kΩ ,0603 resistors Panasoni	c ERJ-3EKF1003V
1 R41 10 kΩ, 0603 resistor Panasoni	c ERJ-3EKF1002V
1 R43 91 Ω, 0603 resistor Yageo	9C06031A91R0FKHFT
1 TP1 Yellow test point Keystone	Electronics 5000
4 TP16, TP17, TP23, TP24 Red test point Keystone	Electronics 5000
1 U1 ADF5902 24 GHz Tx MMIC Analog D	Devices ADF5902WWCPZ-U1
1 U3 IC 32 kB serial EEPROM Microchip	p 24LC32A-I/MS
1 U4 3.3 V complimentary metal-oxide Analog D semiconductor (CMOS) linear regulator	Devices ADP150AUJZ-3.3-R7
1 U6 3.3 V CMOS linear regulator Analog D	Devices ADP7104ARDZ-3.3
1 Y1 100 MHz crystal clock oscillator Connor-V	Vinfield CWX113-100.0M
3 C20, C25, C30 Do not install Not appli	icable Not applicable
1 C33 Do not install Not appli	icable Not applicable
2 C37, C42 Do not install Not appli	icable Not applicable
3 R6, R21, R42 Do not install Not appli	icable Not applicable
1 R38 Do not install Not appli	icable Not applicable

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Quantity	Reference Designator	Part Description	Manufacturer	Part Number
4	R51 to R54	Do not install	Not applicable	Not applicable
20	TP3, TP6, TP7, TP9 to TP15, TP18, TP20 to TP22, TP29 to TP32, TP34, TP36	Do not install	Not applicable	Not applicable
2	SCREW1, SCREW2	Screw, cheese, nylon, M3×10, PK100	Allthread Plastics Limited	119030010
2	NUT1, NUT2	Nut and washer, nylon, M3, PK100	Duratool	119030011

RELATED LINKS

Resource	Description
ADF5902	Product Page, 24 GHz VCO and PGA with 2-Channel PA Output
ADP7104	Product Page, 20 V, 500 mA, Low Noise, CMOS LDO



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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