A4937

Automotive 3-Phase MOSFET Driver

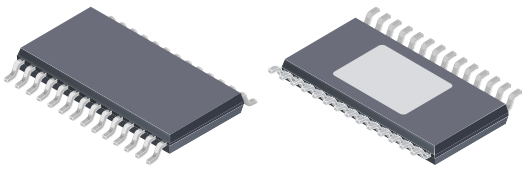
FEATURES AND BENEFITS

- High current 3-phase gate drive for N-channel MOSFETs
- SPI compatible serial control
- Cross-conduction protection
- Programmable dead time
- 5.5 to 50 V supply voltage range
- TTL inputs compatible with 3.3 V and 5 V logic
- Extensive diagnostics output
- Low current sleep mode

APPLICATIONS

- Electronic power steering (EPS, EHPS, EAS)
- Hydraulic pumps
- Engine cooling fan
- Gearbox actuator

PACKAGE: 28-PIN TSSOP WITH EXPOSED THERMAL PAD (SUFFIX LP)



Not to scale

DESCRIPTION

The A4937 is a 3-phase controller for use with N-channel external power MOSFETs and is specifically designed for automotive applications.

A unique charge pump regulator provides full (>10 V) gate drive for battery voltages down to 7 V and allows the A4937 to operate with a reduced gate drive, down to 5.5 V.

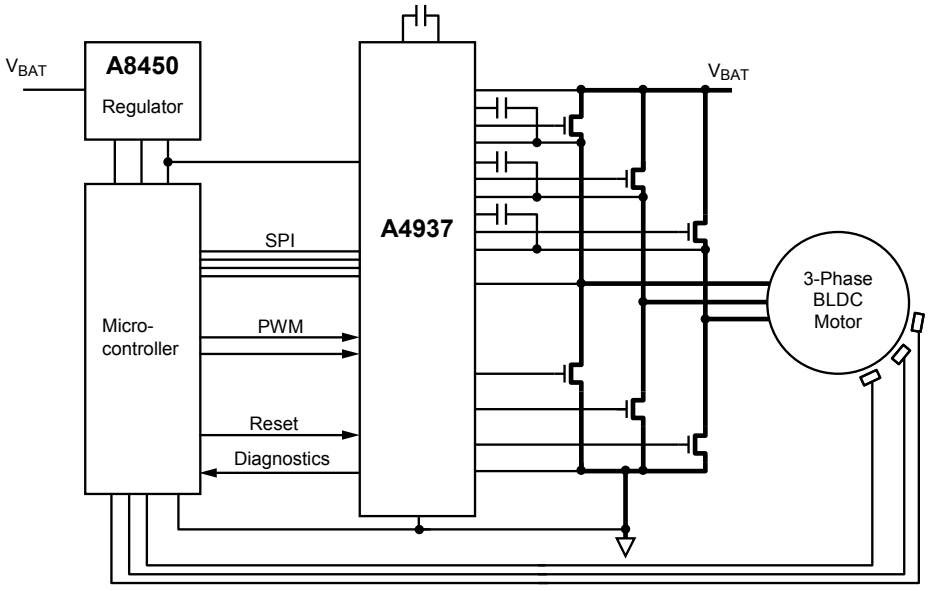
A bootstrap capacitor is used to provide the above battery supply voltage required for N-channel MOSFETs.

Full control over all six power MOSFETs in the 3-phase bridge is provided, through an SPI compatible serial interface, allowing motors to be driven with block or overlap commutation. Power output can be regulated by one or both of the PWM inputs. The power MOSFETs are protected from shoot-through by integrated crossover control and programmable dead time.

Integrated diagnostics provide indication of undervoltage, overtemperature, and power bridge faults, and can be configured to protect the power MOSFETs under most short circuit conditions. Detailed diagnostics are available as a serial data word.

The A4937 is supplied in a 28-pin TSSOP power package with with exposed pad for enhanced thermal dissipation (package type LP). This package is lead (Pb) free, with 100% matte-tin leadframe plating.

Functional Block Diagram



Selection Guide

Part Number	Packing*	Package
A4937KLPTR-A-T	4000 pieces per 13-in. reel	4.4 mm × 9.7 mm, 1.2 mm maximum height TSSOP with exposed thermal pad

*Contact Allegro™ for additional packing options.

Absolute Maximum Ratings*

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		–0.3 to 50	V
Logic Supply Voltage	V_{DD}		–0.3 to 6	V
Terminal VREG	V_{REG}		–0.3 to 16	V
Terminal CP1	V_{CP1}		–0.3 to 16	V
Terminal CP2	V_{CP2}		V_{CP1} – 0.3 to V_{REG} + 0.3	V
Logic Inputs	V_I	STRn, SCK, SDI, PWMH, PWML	–0.3 to 6	V
		RESETn; can be pulled to V_{BB} with >22 kΩ	–0.3 to 6	V
Logic Outputs	V_O	SDO	–0.3 to V_{DD} + 0.3	V
Terminal DIAG	V_{DIAG}		–0.3 to V_{DD} + 0.3	V
Terminal VBRG	V_{BRG}		–5 to 55	V
Terminals CA, CB, CC	V_{Cx}		–0.3 to V_{REG} + 50	V
Terminals GHA, GHB, GHC	V_{GHx}		V_{Cx} – 16 to V_{Cx} + 0.3	V
Terminals SA, SB, SC	V_{Sx}		V_{Cx} – 16 to V_{Cx} + 0.3	V
Terminals GLA, GLB, GLC	V_{GLx}		V_{REG} – 16 to 18	V
Terminal LSS	V_{LSS}		V_{REG} – 16 to 18	V
Ambient Operating Temperature Range	T_A	Limited by power dissipation	–40 to 150	°C
Maximum Continuous Junction Temperature	T_J(max)		150	°C
Transient Junction Temperature	T_{tJ}	Overtemperature event not exceeding 10s, lifetime duration not exceeding 10 hours, guaranteed by design characterization.	175	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

*With respect to GND. Ratings apply when no other circuit operating constraints are present.

Thermal Characteristics may require derating at maximum conditions

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	28	ºC/W
		2-layer PCB with 3.8 in.^{2} of copper area each side	32	ºC/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	ºC/W

*Additional thermal information available on the Allegro website.

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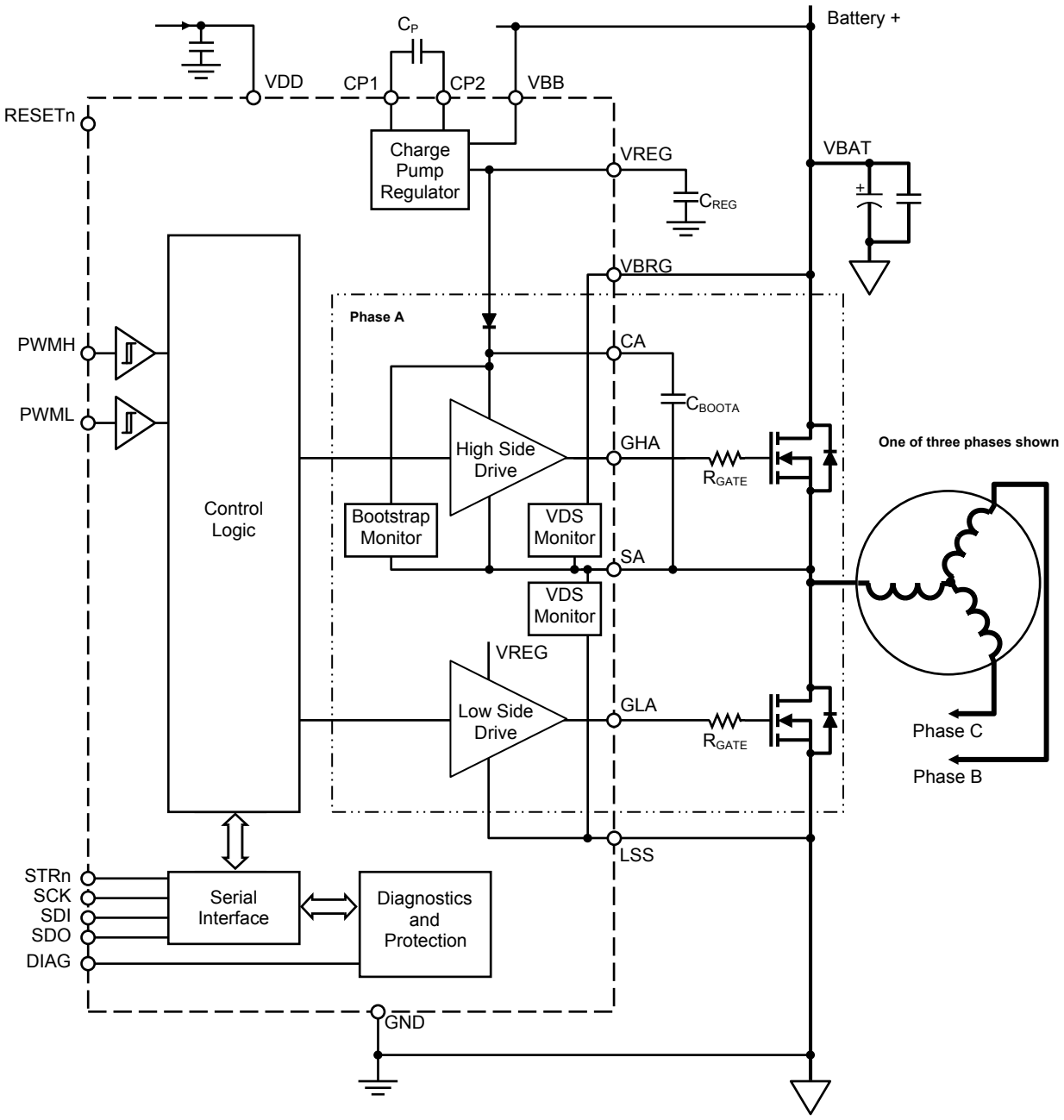
Functional Block Diagram



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Revision Table

Number	Date	Description
2	January 29, 2019	Minor editorial updates
3	February 6, 2020	Minor editorial updates

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