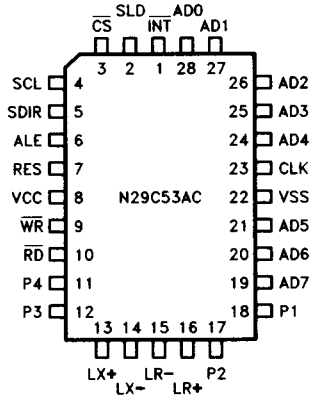
iATC 29C53AC
DIGITAL LOOP CONTROLLER

- **4-Wire Full Duplex Digital Transceiver**
- **CCITT I.430, ANSI TI.605 "S" Interface Compatible**
- **ISDN Basic Rate 144K Bit Per Second**
- **D-Channel Processing Support**
- **Point-To-Point or Point-To-Multipoint Bus Configuration**
- **Same Device Used at Both Ends of Loop**
- **Exceeds 1K Meter Range**
- **iATC Standard SLD Interface**
- **MCS® Standard Microprocessor Interface**
- **Peripheral Interface/Status Port**
- **Low Power, High Density CHMOS**
- **Single +5 Volt Supply**

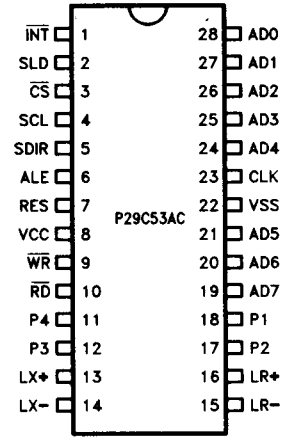
The Intel Advanced Telecommunication Component (iATC) 29C53AC Digital Loop Controller (DLC) is a 4-wire transceiver/controller that is CCITT I.430 and ANSI TI.605 compatible and can function at either loop end. This part has integrated those features which are pertinent to the transceiver function and offers efficient interfacing to other system components such as CODEC/Filters and microcontrollers through the SLD and microprocessor interface ports. It is primarily intended for use in Integrated Services Digital Networks (ISDN) as a basic rate digital data transceiver which transfers data at 144 Kbps as three separate channels—two 64 Kbps digitized-voice/data channels (B channels), and a 16 Kbps signaling/data channel (D channel). The B- and D-channel routing along with D-channel processing (packet framing) is programmable through either the microprocessor or SLD interface ports. The 29C53ACs loop interface uses a 100% pulse-width pseudo-ternary line code which meets CCITT's "S" interface recommendations. It is capable of interfacing with up to eight 29C53ACs in a passive or extended bus configuration as well as point-to-point.

Plastic Chip Carrier
350 x 550 MILS



270097-1

28-Lead Dual-In-Line Package



270097-2

Figure 1. 29C53AC Pin Configurations

September 1992
Order Number: 270097-008

Symbol	Pin No.	Function
V_{CC}	8	**POSITIVE SUPPLY:** Input voltage is +5V ±5%.
V_{SS}	22	**GROUND:** 0V
CLK	23	**MASTER CLOCK:** The 3.84 MHz system clock input is the reference for the loop and the SLD interface.
Res	7	**RESET:** (Active high input). A high level on this pin initializes control registers and places interface outputs in a high impedance state. Operation begins after the high level is removed.
LX^+, LX^-	13, 14	**POLARIZED TRANSMIT LOOP INTERFACE PINS:** These pins will directly drive the twisted pair line through a pulse transformer. The transmitted line code is 100% pulse width pseudo-ternary.
LR^-, LR^+	15, 16	**RECEIVE LOOP INTERFACE PINS:** The receiver is not sensitive to polarity.
SLD	2	**SUBSCRIBER LINE DATALINK:** This pin transfers serial data between the 29C53AC and other SLD based components (e.g., 29C48).
SCL	4	**SUBSCRIBER CLOCK:** 512 KHz signal may be either generated or received by the 29C53AC. This signal clocks the data on the SLD pin.
SDIR	5	**SUBSCRIBER DIRECTION:** An 8 KHz signal may be either generated or received by the 29C53AC to indicate SLD data direction and framing. A high level indicates master to slave transfer; a low level indicates slave to master transfers.
$\overline{CS}$	3	**CHIP SELECT:** (Active low input). A low level on this pin enables the 29C53AC bus interface for the next bus cycle. The value is latched by the falling edge of ALE.
$\overline{RD}$	10	**READ STROBE:** (Active low input). When low, data is transferred from the selected register to the data pins AD (0–7). When no local microprocessor is connected, this pin should be tied to V_{SS}.
$\overline{WR}$	9	**WRITE STROBE:** (Active low input). When $\overline{WR}$ changes from low to high, data on pins AD (0–7) is latched into the 29C53AC. When no local microprocessor is connected, this pin should be tied to V_{SS}.
AD (0–7)	19–21, 24–28	**ADDRESS/DATA PINS:** This is a standard MCS microprocessor bus used to transfer address and data between the local microprocessor and the internal registers of the 29C53AC. When a local microprocessor is not used, these pins should be tied to V_{SS}.
ALE	6	**ADDRESS LATCH ENABLE:** Address is latched from AD(1–5) on falling edge of this signal. State of $\overline{CS}$ is also latched at this time.
$\overline{INT}$	1	**INTERRUPT REQUEST:** This is an open drain active low output. (See text for the interrupt conditions.)
P1, P2	18, 17	**PERIPHERAL INTERFACE INPUTS:** These are standard CHMOS high impedance inputs that are sampled at a 4 KHz rate (once per "s" frame). The sampled data is stored in the LPS register (bits 5 and 6). If any peripheral input bits have changed value since the previous frame, an interrupt condition is indicated; only present status is available.
P3	12	**PERIPHERAL INTERFACE INPUT/OUTPUT PIN:** When configured as an input, this pin has the same characteristics as P1 and P2. The sampled data is stored in the LPS register (bit 7). When programmed as an output, this pin outputs the data stored in the PEC register (bit 1). The pin is configured by bit 2 of the PEC register. An alternate function of this pin and P4 is to indicate the status of the SLD interface. See the section on the SLD interface.
P4	11	**PERIPHERAL INTERFACE OUTPUT PIN:** This pin outputs data stored in the PEC register (bit 0) or SLD status.

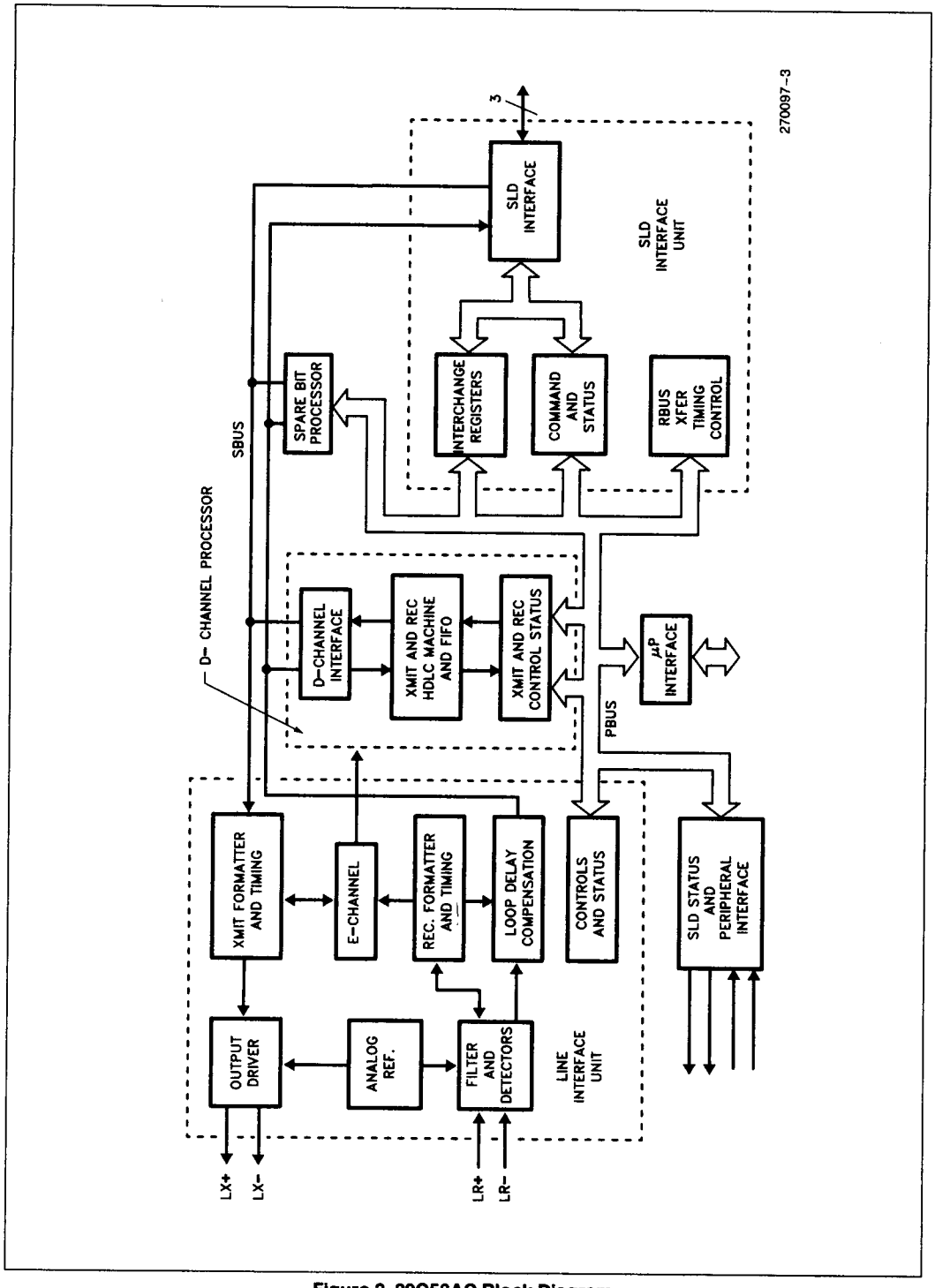


Figure 2. 29C53AC Block Diagram

1.0 INTRODUCTION

The 29C53AC Digital Loop Controller is an advanced, programmable digital transceiver providing the layer one interface at the S or T reference point in Integrated Services Digital Network (ISDN) basic access applications. It provides access to the two B channels and the D channel in accordance with CCITT recommendation I.430 and ANSI standard TI.605, and supports both point-to-point and multipoint topologies. It can be used in linecard (NT) applications, or with the 29C48 programmable CODEC/Filter and appropriate data communications devices in voice/data subscriber (TE) applications.

The 29C53AC may be incorporated at either end of a subscriber loop interface (at the line card or digital telephone/terminal). As shown in Figure 2, the 29C53AC has four separate interfaces: a serial SLD system interface; a parallel peripheral interface; a parallel microprocessor interface and a 4-wire CCITT compatible S-interface (subscriber loop interface).

THE BLOCK DIAGRAM

Figure 2 represents a block diagram of the 29C53AC. Its three major blocks, the line interface unit, the D-channel processor and the SLD interface unit are interconnected by two buses. The parallel bus (PBUS) is used to transfer processed D-channel data and general status and control information, while the serial bus (SBUS) is used to transfer B-channel data and unprocessed D-channel data between the line interface unit and the SLD interface unit.

The SLD interface unit consists of shift registers and serial to parallel converters. Data from both the SBUS and the SLD interface is stored here in appropriate parallel registers before it is loaded into shift registers and passed on. All of the timing circuitry for the SLD interface is located here. This block also contains a command processor which is responsible for executing commands received in the SLD C byte.

The D-channel processor has three major sections. An HDLC section performs some of the basic LAPD protocol functions such as zero insertion or deletion, flag recognition or insertion for frame delineation, abort flag recognition, idle state transmission, and end of packet frame check sequence for both data directions. The FIFO section consists of two 32-byte buffers, one for transmit and one for receive. The control and status section monitors the FIFO data levels and the HDLC section for progress. Interrupts or requests for service may be generated for conditions such as FIFO fullness level, loss of sync, frame check error, overflows and aborts.

The line interface unit contains the line drivers and receivers for the S interface. Connection is made to the transmission lines through a pulse transformer. Formatting, timing and synchronization are also provided here. The receiver includes filters, AGC circuitry, threshold detectors and a loop delay shift register. The loop delay shift register maintains the proper internal frame relationship regardless of loop length (it allows extra propagation delay time for long loops or line repeaters). The received D-channel bits are logically looped back to create the E-channel bits in an NT application through the E-channel circuitry.

The microprocessor interface circuitry allows the 29C53AC to function as a peripheral to a microcontroller or microprocessor. All internal registers are directly accessible.

The spare bits processing block provides access to the FA, N, and A bits. It also provides access to the S and M bits, and supports the S and Q channels.

The peripheral interface circuitry provides an auxiliary port for controlling auxiliary peripherals such as power controllers, etc. It can be programmed to provide SLD status as well.

SLD INTERFACE

The SLD interface provides communication with other devices incorporating SLD interfaces.

As shown in Figure 3, the SLD interface consists of three lines: the SLD bidirectional data line; the 512 KHz SCL clock line; and the 8 KHz SDIR data direction line. SLD data is updated on the rising edge of SCL and is latched on its falling edge. The 125 μs SLD frame period consists of 32 bits transferred in master to slave direction followed by 32 bits in the slave to master direction. The 32 bits compose four 8-bit bytes in the following order: B1 and B2 (voice or data bytes); C (control byte); and S (signaling or status byte). Unprocessed D-channel data may be transported over the S-byte in bits 0 and 1, or over the B2 byte.

The 29C53AC can be operated as an SLD master or slave. As an SLD master, it generates the SCL and SDIR signals. When SDIR is high, the SLD pin outputs data. As a slave, it receives SCL and SDIR sig-

nals and SDIR enables the SLD output driver when it is low. The SLD bus is always active; no powered-down or inactive mode is defined.

In a network termination (NT) application (line card), whether a microprocessor is connected to the 29C53AC or not, the SLD control and signaling bytes may be used for 29C53AC configuration and D-channel transfers. The command bytes are interpreted and executed by the 29C53AC's command processor circuit. The command processor generates internal PBUS cycles to carry out those commands. Internal prioritization resolves PBUS collisions between microprocessor-interface generated and command-processor generated cycles. In case of collisions, the microprocessor interface has higher priority to minimize access time but both cycles will be completed.

"S" TRANSCEIVER

The 4-wire "S" transceiver circuit in the 29C53AC conforms to CCITT recommendation I.430 and ANSI standard TI.605. This transceiver provides the internal drivers for transformer coupling to standard telephone type twisted pair cables.

The "S" transceiver line code is 100% pulse width pseudo-ternary code, with binary ones represented by no line signal, and binary zeros by a positive or negative pulse. Pulses alternate polarity except when a code violation is created for establishing the frame reference timing. The nominal pulse amplitude is 750 mV when a suitable pulse transformer is used.

The 29C53AC transmitter is typically connected to the line through a pulse transformer and series resistance (see Figure 12). The series resistance, when used with protection diodes, provides additional protection against surges. It also increases the output impedance.

The nominal bit rate is 192 Kbps. Figure 4 shows the frame structure. The 250 μs frame transfers two octets of B1, B2 and four bits of D data. The E bits in the master to slave direction echo received D-channel data. The "S" interface slave compares the receive E-channel data to its transmitted D-channel data for D-channel contention as defined in CCITT recommendation I.430. If these bits do not agree, then the slave will abort its transmission effort. The S, M, FA, A, and N bits are all accessible and programmable. The 29C53AC supports the layer 1 maintenance multiframing for the Q and S channels.

The activation protocol described in I.430 is supported by the 29C53AC. An inactive receiver can achieve bit synchronization to an incoming signal with approximately 15 mark-mark transitions. Info 2 or 3 frame alignment is not officially recognized until reception of 16 frames, to allow settling of the 29C53AC's adaptive receive data thresholds. The full activation sequence will complete in approximately 10 ms.

The 29C53AC is not sensitive to the polarity of the wire pair connected to LR^+ and LR^-. Pulses are always interpreted as zeros and framing relies on violations; not on absolute polarity. System configurations may dictate that care be taken in connecting the LX outputs. In a multi-drop bus configuration all TE transmitters must be connected with the same polarity so that positive pulse to negative pulse contention does not take place in the framing and D-channel bits.

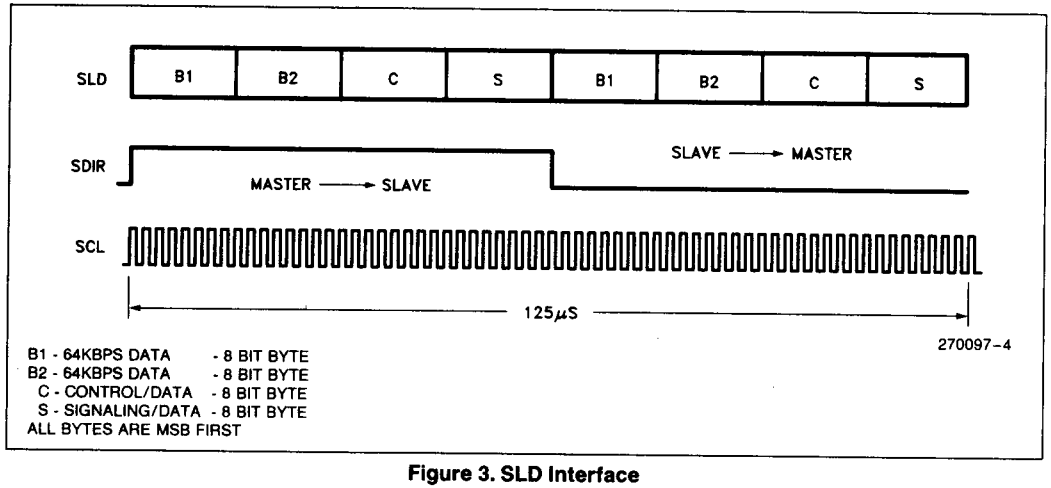


Figure 3. SLD Interface

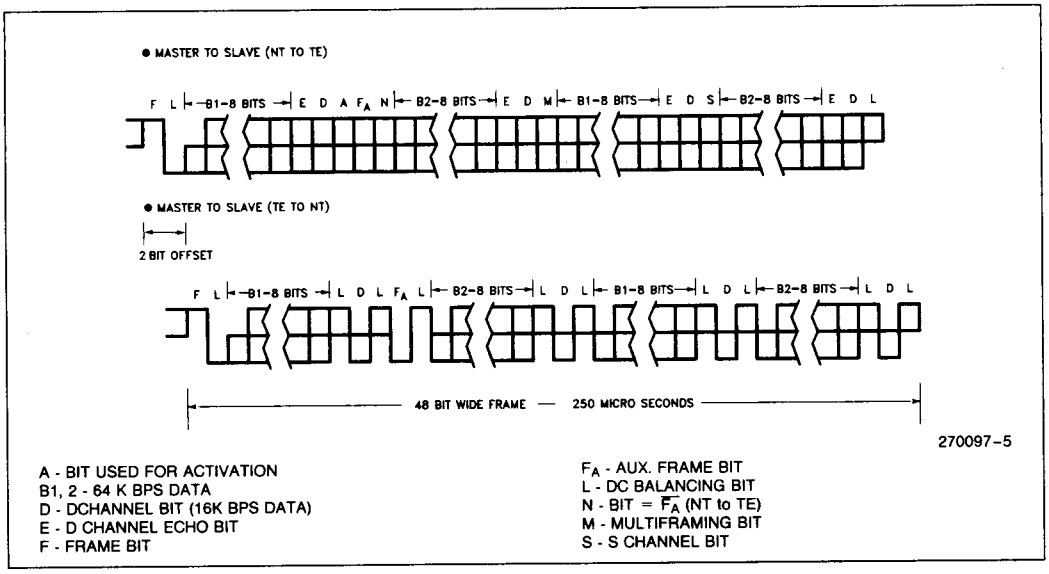


Figure 4. The S-Interface Frame Structure

The 29C53AC, functioning as an "S" interface master in a multi-drop application, can interface with up to eight slave systems. In this multiplexing operation a slave initiates a data transfer to the master, by requesting access and transferring the data in accordance with the D-channel line access protocol (I.440). Figure 5 shows typical applications of the 29C53AC.

The frame alignment timing diagram Figure 6(b) shows the relationship of the "S" interface data to the SLD data. Figure 6(a) shows the block diagram used for the timing diagram. The top timing diagram of Figure 6(b) shows the transmitted "S" data stream from the network terminator (master). The dotted lines depict up to 20 μs propagation delay to the "S" receiver at the terminal equipment (slave) end. The terminal equipment's transmitted "S" interface frame is designed to have a fixed 2-bit frame alignment delay from that of its received frame. The adjustment for loop propagation delay is accounted for in the network terminator's receive circuitry (loop delay section of block diagram). The loop delay circuitry will compensate for up to 10 bit periods of round trip propagation delay which allows line repeaters to be placed in a loop that is several thousand meters long.

MICROPROCESSOR INTERFACE

This interface is designed to operate with standard Intel microprocessors such as the MCS®-48, MCS-51, MCS-85 and 8086 families. All of the 29C53AC's internal registers are accessible and are available by a single microprocessor cycle access. The 29C53AC latches address information from

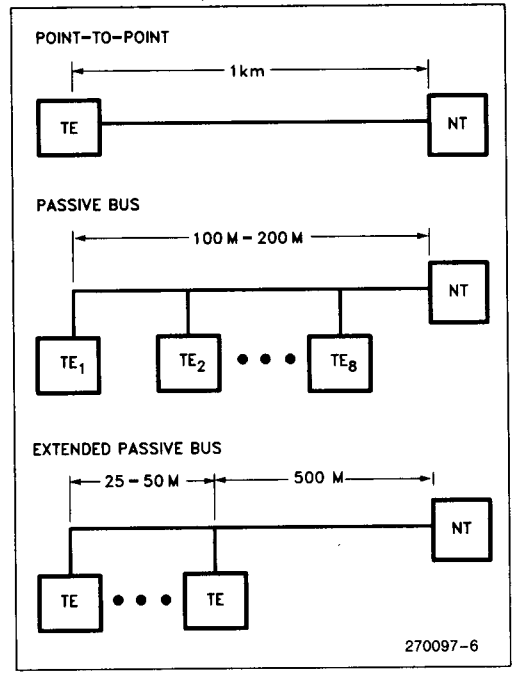


Figure 5. 29C53AC Bus Configurations

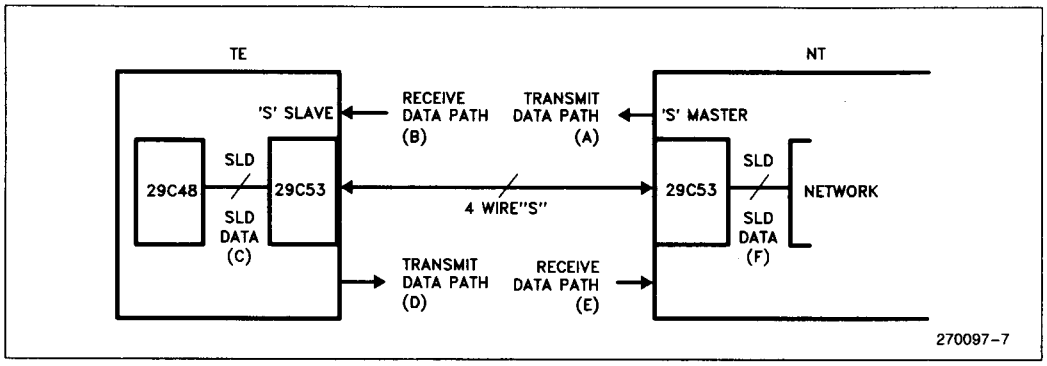


Figure 6(a). Frame Alignment (Block Diagram)

AD1–AD5, and does not use AD0 for addressing. This provides compatibility with 16-bit microprocessors.

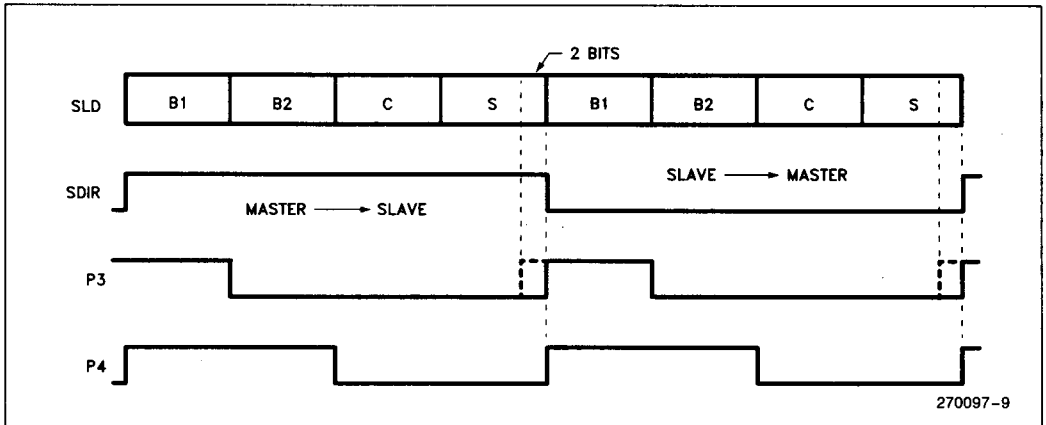
The maskable interrupt pin is activated by the following interrupt status features: D-channel errors; loss of sync on "S" loop; change in spare bits or peripheral interface data; FIFO data transfer requests.

Alternatively, the 29C53AC can operate in the standalone mode in line card and NT applications. This mode is determined after a reset, provided all the microprocessor interface pins have been tied to V_{SS}, except for the interrupt pin. The 29C53AC is then controlled using the C byte of the SLD interface.

PERIPHERAL INTERFACE

The peripheral interface uses four pins to provide control to, and to accept status from, external devices. Two pins are inputs, one is an output and one is configurable either as an input or an output. The configurable pin defaults to the input mode on power up.

The peripheral interface can also be used to indicate SLD status. Figure 7 shows the timing diagram of P3 and P4. B1, B2 and D-channel data on the SLD pin can be selected or gated by using these signals. As noted on the P3 timing, the D-channel is imbedded in the last two bits (0, 1) of the signaling byte. (This must be programmed in the DPC register).



NOTE:
1. Status indicators are activated by the SST Bit in the PEC Register.
2. P3 changes two bits prior to P4 if raw D-channel data is routed over the SLD S byte.

Figure 7. 29C53AC SLD Status Indicators

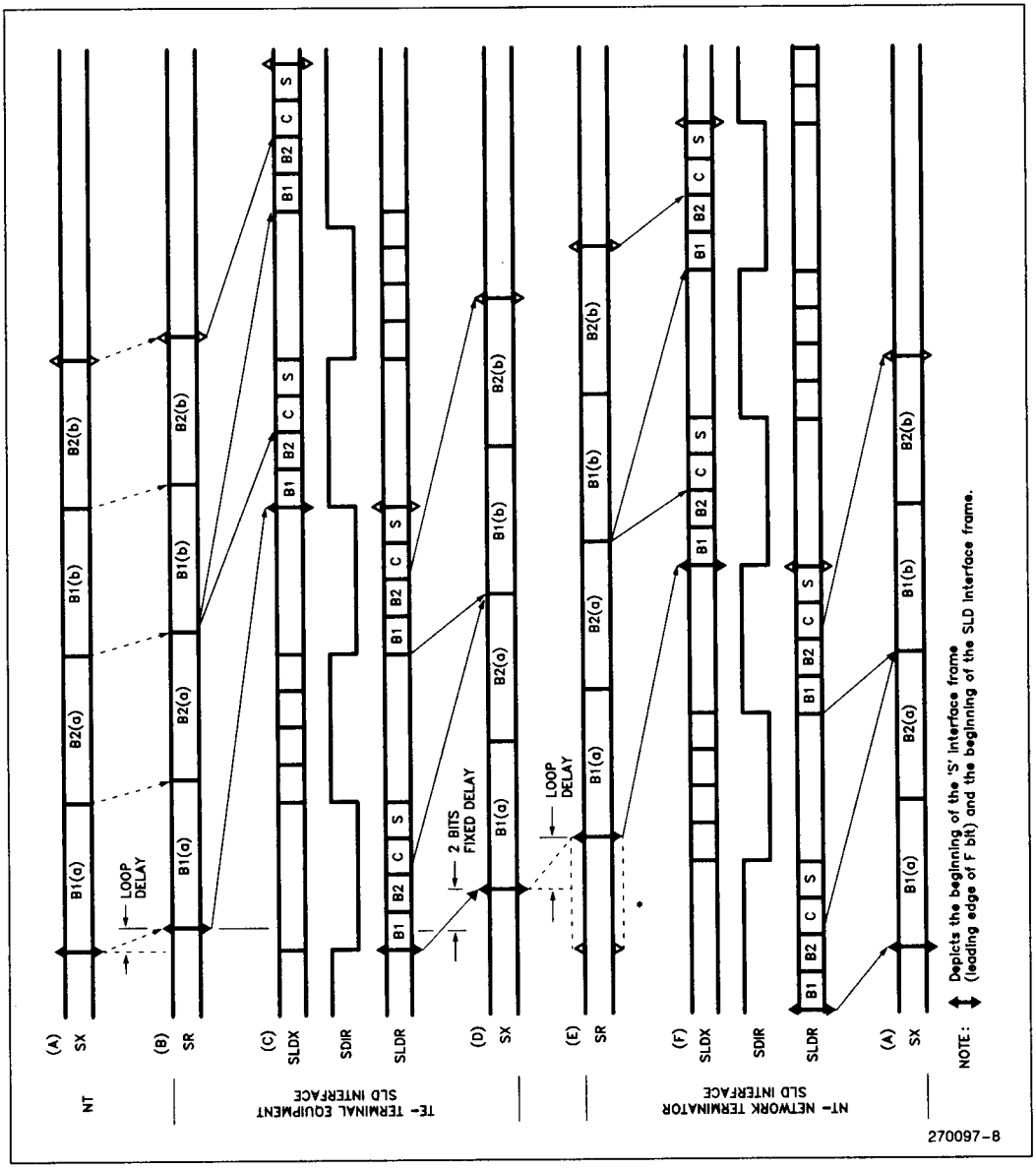


Figure 6(b). Frame Alignment (Timing Diagram)

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Op Code Table

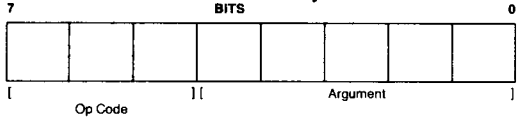
OpCode	Operation	Argument
000	Reserved For Status Poll (Call Verify) By Master	—
001	Single Byte Transfer To Slave	Reg Adr
010	Prepare Single Byte For Transfer To Master	Reg Adr
011	Multiple-Byte D Data Transfer To Slave	#Bytes
100	Multiple-Byte D Data Transfer To Master	Max # Bytes
101	Multiple-Byte Configuration Transfer To Slave	# Bytes
110	Multiple-Byte Status Transfer To Master	# Bytes
111	Reserved For Status Poll (Call Verify) Tail & Idle	—

INTERNAL CONTROL AND STATUS REGISTERS

All of the 29C53AC's internal control and status registers may be accessed through the microprocessor interface or through the SLD interface (when in SLD slave mode). When a microprocessor accesses a register, the address and CS inputs are latched on the trailing edge of ALE. The address is latched from pins AD1–AD5 of the microprocessor port.

In an SLD access, the 29C53AC receives a control byte containing an operation code and an argument. The three most significant bits contain the operation code and the remaining five bits contain the argument. The operation code defines eight transfer types.

SLD Control Byte



The 3-bit operation code in the control byte from the SLD master should normally be 111, indicating the idle state. The transferring of data to and from the 29C53AC is accomplished by indicating the type and the number of bytes to transfer in a non-idle control byte. When a polled response is requested, the 29C53AC responds to the poll operation code 000. This can be used for the transfer of one or several bytes of information.

The D-channel block transfers from the 29C53AC to the SLD master preface the data bytes with a byte header specifying the number of following bytes (less than or equal to the maximum specified) and the status of the packet they belong to. All transferred data bytes belong to the same packet; the transfers occur until the selected number of bytes are transferred or an EOP (end of packet) is detected. The EOP may occur even when there are additional bytes in the FIFO. The header byte contains the byte count in the lowest five bits and the packet status in the upper three bits.

Data transfers over the SLD line cannot be made in both directions simultaneously. Multiple commands and data bytes may follow each other directly from the line card controller to the 29C53AC if the previous command has been fully executed.

It is possible to fully configure the 29C53AC over the SLD interface. Provisions are also made to perform this transfer at a 2 byte-per frame rate using both the C and S bytes of the SLD. The first control byte of a configuration transfer to the 29C53AC specifies the type of operation to be performed and the number of data bytes to follow. The system interface command unit loads the internal registers with the information as it is received. When the specified number of data bytes have been transferred, the 29C53AC assumes the next input is a control byte.

The order of the bytes in a configuration or status block transfer is determined by the addresses of the internal registers. A multiple-byte transfer, beginning with register 00H, transfers the data to or from that register and increments the address counter.

The register table below identifies the address of each 29C53AC register. The status registers are read-only registers while all control registers are read/write registers. Because all the register addresses do not fit into the 5-bit address space, a register test mode has been included which permits reading the contents of control registers at addresses which normally are status registers. Where no register is assigned a location in the register test mode, the normal status register located at this address is read.

Table 1. 29C53AC Registers

Parallel Port Address	Internal Address(1)	Access	Symbol	Function
00	00000	RD	EXS	Interrupt Status
00	00000	WR (RT)	EXM	Interrupt Mask
02	00001	RD	DPS	D-Channel Processor Status
02	00001	WR (RT)	DPC	D-Channel Processor Control
04	00010	RD	LPS	Loop and Peripheral Interface Status
04	00010	WR (RT)	LCR	Loop Interface Control
06	00011	RDWR	PEC	Peripheral Interface and E-Channel Control
08	00100	RD	RFN	Receive FIFO Status - # of Bytes Used
08	00100	WR (RT)	SCR	SLD Interface Control
0A	00101	RD	XFN	Transmit FIFO Status - # of Free Bytes
0A	00101	WR (RT)	SDC	SLD Data Transfer Configuration
0C	00110	RD	SBR	Spare Bits Receive Status
0C	00110	WR (RT)	SBX	Spare Bits Transmit
0E	00111	RDWR	LLB	Loop Interface Loopback Control
10	01000	RD	RFO	Receive FIFO Output
12	01001	WR	XFI	Transmit FIFO Input
14	01010	RDWR	GCR	General Command Register
16	01011	RDWR	DPR	D-Channel Priority Counter
18	01100	RDW	RFXF	Receive FIFO Interrupt Level
1A	01101	RDWR	XFXF	Transmit FIFO Interrupt Level
1C	01110	RD	PLENH	Packet Length High Byte
1C	01110	WR (RT)	DUTH	D-Channel Byte Counter Underflow and Overflow Threshold
1E	01111	RD	PLENL	Packet Length Low Byte
1E	01111	WR (RT)	DOTH	D-Channel Byte Counter Overflow Threshold
20	10000	RDWR	SBC	Spare Bit Control
22	10001	RDWR	PSR	Position Selection
24	10010	RD	RSR	Receive Service Request
26	10011	RD	XSR	Transmit Service Request
30	11000	RDWR	B1LS	B1 Data in Loop to SLD Direction
32	11001	RDWR	B2LS	B2 Data in Loop to SLD Direction
34	11010	RDWR	CR	Control Byte from SLD
36	11011	RDWR	SR	Signaling Byte from SLD
38	11100	RDWR	B1SL	B1 Data in SLD to Loop Direction
3A	11101	RDWR	B2SL	B2 Data in SLD to Loop Direction
3C	11110	RDWR	CX	Control Byte to SLD
3E	11111	RDWR	SX	Signaling Byte to SLD

NOTE:
1. Address represents AD1–AD5. AD0 is not used by the 29C53AC for addressing.

29C53AC Register Definitions

In the register descriptions that follow, the acronym, name, five bit address, and whether the register can be written or read (or read only in RT mode) are provided in the heading. For easy reference, the registers are listed in alphabetical order.

B1LS B1 Data "S" to SLD Direction 11000 R, W

7	6	5	4	3	2	1	0
B1 data							

This register provides access to the B1 channel data flow in the direction from the "S" loop to SLD interface. Data can be read or overwritten by the microprocessor in intercept mode (see SCR register). Also, data can be accessed so the MSB is in bit 7 (default mode) or flipped so that the LSB is in bit 7 by issuing the appropriate GCR command.

B2LS B2 Data "S" to SLD Direction 11001 R, W

7	6	5	4	3	2	1	0
B2 data							

This register provides access to the B2 channel data flow in the direction from the "S" loop to SLD interface. Data can be read or overwritten by the microprocessor in intercept mode (see SCR register). Also, data can be accessed so the MSB is in bit 7 (default mode) or flipped so that the LSB is in bit 7 by issuing the appropriate GCR command.

B1SL B1 Data SLD to "S" Direction 11100 R, W

7	6	5	4	3	2	1	0
B1 data							

This register provides access to the B1 channel data flow in the direction from the SLD interface to the "S" loop. Data can be read or overwritten by the microprocessor in intercept mode (see SCR register). Also, data can be accessed so the MSB is in bit 7 (default mode) or flipped so that the LSB is in bit 7 by issuing the appropriate GCR command.

B2SL B2 Data SLD to "S" Direction 11101 R, W

7	6	5	4	3	2	1	0
B2 data							

This register provides access to the B2 channel data flow in the direction from the SLD interface to "S" loop. Data can be read or overwritten by the microprocessor in intercept mode (see SCR register). Also, data can be accessed so the MSB is in bit 7 (default mode) or flipped so that the LSB is in bit 7 by issuing the appropriate GCR command.

CR Control Byte Receive 11010 R, W

7	6	5	4	3	2	1	0
data							

This address provides access to the receive control byte register pair in the SLD register bank. In SLD master mode, this register contains the received control (C) byte from the SLD link. This is typically control information read back from an SLD slave device such as the 29C48. Register contents are only valid in SSM (SLD master) mode.

CX Control Byte Transmit 11110 R, W

7	6	5	4	3	2	1	0
data							

This address provides access to the transmit control byte register pair in the SLD register bank. In SLD master mode, data placed in this register is transmitted over the SLD link in the C byte. This is typically control information sent to an SLD slave device such as the 29C48. Data is only transmitted in SSM (SLD master) mode.

DOTH Overflow Threshold (Low Byte) 01111 W (RT)

7	6	5	4	3	2	1	0
Overflow Threshold Bits 0–7							

This overflow threshold (maximum packet length) may be specified in the range 1–4095. An exception is generated (see DPS register) if the threshold is equaled or exceeded. Setting this register to 00H (default) disables this function. The most significant four bits of the overflow threshold are set in the DUTH register.

DPC D-Channel Processor Control 00001 W (RT)

7	6	5	4	3	2	1	0
unused		DRT		B2D	D-Ch. Routing		

DRT D-channel routing through B2 on the SLD if bits 2–0 are 101.

BITS 5	4	
0	0	route through B2 bits 0, 1
0	1	route through B2 bits 2, 3
1	0	route through B2 bits 4, 5
1	1	route through B2 bits 6, 7

B2D When the raw D channel is routed to the SLD in the B2 byte (DPC bits 2–0 = 101), this bit sets the value for the unused bits of the transmit direction B2 byte (all zeroes or all ones).

D-channel routing is programmed in bits 2–0 of this register for both NT and TE operation. D-channel processing can be bypassed to provide a clear 16K bits per second channel over the SLD line if desired. Bit 1/3/5/7 of the B2 channel or bit 1 of the S channel will be the first one transferred over the "S" bus in this case.

BITS			D-CHANNEL MODE
2	1	0	
0	0	0	Processor inactive, disconnect from SBUS
0	0	1	Loopback test mode (1)
0	1	0	Reserved
0	1	1	Processor active on SBUS, normal operation
1	0	0	Processor inactive, raw D through SLD S byte bits 1, 0
1	0	1	Processor inactive, raw D through SLD B2 byte as set in DPC 4, 5
1	1	0	Reserved
1	1	1	Reserved

NOTE:
1. Bit PEC.4 (EM0) must also be set to one to use the D-channel loopback test mode when operating as a loop slave (TE) if the loop interface is not synchronized.

DPR D-Channel Priority 01011 R, W

7	6	5	4	3	2	1	0
unused			ZIS	unused			PRI

ZIS When ZIS = 1, the transmitter will not perform zero insertion on the outgoing D-channel frame. The data in the FIFO will be transmitted as is. When ZIS = 0, zero insertion is enabled which is normal operation. The default for this bit is 0.

PRI When PRI = 0, the higher priority class (8) is selected for the D-channel priority logic. When PRI = 1, the lower priority class (10) is selected. This bit defaults to 1, selecting the lower priority class.

DPS D-Channel Processor Status 00001 R

7	6	5	4	3	2	1	0
XB	transmit status			RD	receive status		

XB Transmitter busy. This bit is set to 1 whenever D-channel processor is transmitting. This bit does not affect the XDP bit in EXS, or cause an interrupt. This bit is zero when the transmitter is inactive or awaiting priority on the D-channel.

Transmit status, encoded as follows:

Bit 4 if set to 1, the packet being transmitted was aborted due to FIFO underrun. The FIFO was emptied, and no EOP tag was found.

Bit 5 if set to 1, the packet being entered to the FIFO by the microprocessor was aborted due to FIFO overrun. The FIFO was written to when full.

Bit 6 if set to 1, the packet being transmitted was aborted due to loss of priority, or loss of sync. At a TE, priority is lost if the E-channel bit just received does not match the last transmitted D bit.

RB Receiver busy. This bit is set when a packet is currently being received. This bit does not affect the RDP bit in EXS, or cause an interrupt.

Receive status. The status of the packet which the microprocessor has access to (appears at RFO) is encoded as follows:

BITS			Receive Status
2	1	0	
0	0	0	Still receiving, no EOP yet
0	0	1	Good EOP
0	1	0	FCS error
0	1	1	FIFO underrun (read when empty)
1	0	0	FIFO overrun (FIFO full when next byte received)
1	0	1	Packet underflow (packet too short, threshold set in DUTH)
1	1	0	Packet overflow (packet too long, threshold set in DOTH)
1	1	1	Abort or loss of sync

DUTH Underflow and Overflow (High Byte) Threshold 01110 W (RT)

7	6	5	4	3	2	1	0
underflow threshold				overflow threshold bits 11–8			

The underflow threshold (minimum packet length) may be specified in the range 1–15. An exception is generated (see DPS register) if the threshold is not exceeded. Setting this register to 00H (default) disables this function. The upper four bits of the overflow threshold are also contained here.

EXM Exception Mask 00000 W (RT)

7	6	5	4	3	2	1	0
0	XSR	RSR	PC	SX	LS	XDP	RDP

Setting a bit to 1 in this register enables the associated exception to generate an interrupt, and to appear in the S byte of the SLD line. This register is initialized to 00H, all interrupt sources masked.

EXS Exception Status 00000 R

7	6	5	4	3	2	1	0
X	XSR	RSR	PC	SX	LS	XDP	RDP

This is the main status register. It should be polled first when investigating the source of an exception. Some status is expanded in additional registers. When unmasked, bits set in EXS cause an interrupt, and affect the SLD signaling byte status.

X reserved for future use, should be masked.

XSR request for transmit FIFO data transfer. The transmit FIFO is at the programmed level of emptiness (set in XFXF). Or, if XFXF = 0, the closing flag of a packet has been transmitted.

RSR request for receive FIFO data transfer. A complete D-channel packet has been received, or the FIFO is full to the programmed level (set in RFXF).

PC change noted in peripheral interface inputs. Read LPS bits 5–7 for status.

SX exception noted in spare bit unit (multiframing or A bit change). Read SBC for more information.

LS loss or gain of synchronization to the "S" loop. Read LPS for loop status.

XDP D-channel processor exception, transmit side. Read DPS bits 4–6 to determine cause.

RDP D-channel processor exception, receive side. Read DPS bits 0–2 to determine cause.

GCR General Command Register 01010 R, W

7	6	5	4	3	2	1	0
command code							

Writing one of the listed codes to the GCR register causes the specified event to execute once. A new command should not be written to GCR for five cycles of CLK. Where the code contains X's, those bits have no effect. Reading the GCR register reads the previous command.

GCR Commands

CODE	COMMAND	EVENT
111XXXXX	GRST	Reset all internal units.
011XXX11	GDRAB	Clear receive FIFO to next EOP (ignore data from loop until FLAG if none presently in FIFO).
011XXX10	GDRCL	Clear entire receive FIFO.
011XXX01	GDXAB	Abort and clear the transmit packet currently being constructed by the microprocessor.
011XXX00	GCXCL	Stop D-channel transmission, clear transmit FIFO, and indicate idle on transmitted D-channel.
010XXX10	GDXMK	Mark EOP in transmit FIFO (no effect if FIFO empty).
010XXXT1	GLMX4, GLMX2	Transmit INFO 4 (T = 0) or INFO 2 (T = 1) regardless of receive state. GLMX2 must be issued once before GLMX4 will cause INFO 4 to be transmitted. GTD must be issued to after GLMX4 return to normal operation.
010XXX00	GSSY	Synchronize S frame to the next SLD frame (valid only when the loop is inactive).
001XXXNF	GB1F, GB2F	N = select B1 (0) or B2 (1). F = 0, don't flip (bit reverse) B1/B2 between PBUS and SBUS (MSB first). F = 1, flip B1/B2 between PBUS and SBUS (LSB first).
000XXX0A	GTST	Set PBUS address A5 to A (A = 1 for register test mode).
000XXX1D	GTA, GTD	Set D = 1 for loop activation command, set D = 0 for loop deactivation command.
otherwise	no effect	no action taken.

LCR Loop Interface Control 00010 W (RT)

7	6	5	4	3	2	1	0
unused		B1E	B2E	XMIT	MODE		

B1E, B2E B-Channel Transmit Enables (no effect in LSM modes)

0 disable transmitter for Bn subframes

1 enable transmitter for Bn subframes

XMIT Transmitter Enable (no effect in LSM modes)

0 power/down/disable transmitter (output is high impedance)

1 enable transmitter

MODE Loop Interface Mode

bits

2 1 0

0 0 0 LOFF power down/disable transceiver

0 0 1 LOFF power down/disable transceiver

0 1 0 reserved

0 1 1 reserved

1 0 0 LSSA Adaptive Receive Timing, Slave (TE)

1 0 1 LSMH Hybrid Receive Timing, Master (NT) Extended passive bus or point-to-point

1 1 0 LSMA Adaptive Receive Timing, Master (NT)

1 1 1 LSMF Fixed Receive Timing, Master (NT) Short passive bus

LLB Loop Interface Loopback Control 00111 R, W

7	6	5	4	3	2	1	0
TM1	DL	B2L	B1L	TM2	DS	B2S	B1S

For data looped back towards the loop, the analog circuitry and data formating and deformating is included. For data looped back towards the system (SLD) interface, the loopback occurs at the interface to the internal SBUS. None of the data formating, or analog circuitry is included. The loop interface must be active and synchronized to use these loopback features.

TM1 1 = Test mode which selects short activation (approximately 5 "s" frames) and fixed receive data thresholds (240 mV). 0 = Normal operation (activation requires approximately 16 "s" frames and thresholds are adaptive).

DL 1 = Loopback D toward loop, 0 = disable loopback

B2L 1 = Loopback B2 toward loop, 0 = disable loopback

B1L 1 = Loopback B1 toward loop, 0 = disable loopback

TM2 1 = Test mode which sets internal voltage reference to ½ V_{CC}. 0 = Normal operation. Set this bit to zero.

DS 1 = Loopback D toward system, 0 = disable loopback

B2S 1 = Loopback B2 toward system, 0 = disable loopback

B1S 1 = Loopback B1 toward system, 0 = disable loopback

When operating as a loop slave (TE), bit PEC.4 (EM0) must also be set to one to use the D-channel loopback toward the system interface (set by the DS bit) if the loop interface is not synchronized.

LPS Loop, Peripheral Interface Status 00010 R

7	6	5	4	3	2	1	0
P3S	P2S	P1S	RS	encoded loop interface status			

P3S state of peripheral interface pin P3 when configured as an input

P2S state of peripheral interface pin P2

P1S state of peripheral interface pin P1

RS indicates a received signal (1), or no received signal (0). This bit becomes active after at least three pulses were detected in the previous 48 bit period. This period may not be aligned to the receive frame if the receiver is not yet synchronized. The RS bit is updated once every 48 bit period, and does not cause an interrupt or affect the LS bit in the EXS register. The RS bit does not cause any change in state of the loop interface state machine.

Loop interface status code:

BITS

3 mode: master(1)/slave(0)

2 transmitter enable (both LCR.3 AND LCR.2 are set)

1, 0 11 = active

10 = initialize (init)

01 = initialize

11 = inactive

PEC Peripheral Interface, E Channel Control 00011 R, W

7	6	5	4	3	2	1	0
TM3	AA	EM1	EM0	SST	P3OEN	P3	P4

TM3 1 = Test mode which enables a once per frame, active low strobe to be output on pin P1 (normally an input) which indicates the start of an "s" transmit frame. P2 is also configured as an output (DPLL status).

0 = Normal operation. P1 and P2 are inputs.

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29C53AC LOOP INTERFACE STATES (LPS Register)

BITS 3210	Description
1111	LSM3 active: sending INFO4
1110	LSM2 remote init: receiving INFO 1
1101	LSM1 local init: send INFO 2 on local request
1100	LSM0 inactive, powered up (receiver active)
1011	— (unused) —
1010	LMP2 passive resync, < 16 frames correct
1001	LMP1 passive resync, < 3 pulses per frame
1000	— (unused) —
0111	LSS3 active: sending INFO3
0110	LSS2 remote init: sync to INFO 2/INFO 4
0101	LSS1 local init: send INFO 1 on local request
0100	LSS0 inactive, powered up (receiver active)
0011	LSP3 active, receive only, successful passive resync
0010	LSP2 passive resync, < 16 frames correct
0001	LSP1 passive resync, < 3 Pulses per frame
0000	LOFF inactive, powered down (receiver inactive)

AA auto-answer mode enabled (1), or disabled (0)

EM1, EM0

Master, LSM modes

0X generate E channel from received D

10 force E channel to logical zero

11 force E channel to logical one

Slave, LSS mode

X0 normal E-channel function, contention resolution mechanism is enabled

01 ignore E channel, always transmit D-channel data without waiting for priority. Loss of priority exception is suppressed

11 Force loss of priority

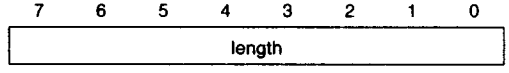
SST present SLD status on P3 and P4 if 1, or if 0, P3 and P4 are I/O pins controlled by PEC bits 0–2.

P3OEN P3 output enable (also enabled by SST). 0 = input, 1 = output

P3 P3 output value

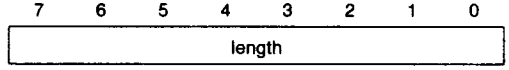
P4 P4 output value

PLENH D-Channel Packet Length High Byte
01110 R



This register holds the upper byte of the length of the current D-channel packet. The count is updated as the packet is read out of the receive FIFO. Reads of PLENH should be done a minimum of 3 CLK cycles after reading RFO.

PLENL D-Channel Packet Length Low Byte
01111 R



This register holds the lower byte of the length of the current D-channel packet. The count is updated as the packet is read out of the receive FIFO. Reads of PLENL should be done a minimum of 3 CLK cycles after reading RFO.

PSR Position Selection Register 10001 R, W

7	6	5	4	3	2	1	0
any bit set							

A one in any bit of this register enables that bit onto the microprocessor bus when the XSR and RSR registers are read. Those bits of PSR in the zero state disable the corresponding bit positions of the microprocessor bus of the 29C53AC so that those bits remain in a high impedance state when RSR or XSR are read.

This register allows the processor to poll up to eight 29C53AC transceivers on the same microprocessor bus at one time, with each having its own status bit position in the byte. Using this method the processor can check status on all 29C53AC devices with a single read.

See also RSR (Receive Service Request) and XSR (Transmit Service Request).

This register cannot be accessed via SLD command.

RFN Receive FIFO Number 00100 R

7	6	5	4	3	2	1	0
EOP	MORE	FULL	number of bytes avail.				

This register indicates the number of bytes in the receive FIFO as detailed below. (Undefined unless the D-channel processor is enabled.)

EOP Minimum of one byte in the receive FIFO is marked as the end of a packet if EOP = 1. If EOP = 0, no byte marked as end of packet.

MORE If MORE = 1, more information is available in the receive FIFO beyond the first packet, delineated by an EOP marker. If MORE = 0, no data lies beyond the first packet.

FULL The entire FIFO is filled if 1. The FIFO is not full if 0.

number If at least one EOP is marked, this value is the number of bytes to the first EOP. If no EOP is marked, this value indicates the number of valid bytes in the receive FIFO.

RFO Receive FIFO Output 01000 R

7	6	5	4	3	2	1	0
data							

Read from this register to read from the receive FIFO. Do not write to this location, as one byte will be lost from the packet (read out from the FIFO). Reads from this location should be separated by 4 CLK cycles.

RFXF Receive FIFO Exception Fullness 01100 R, W

7	6	5	4	3	2	1	0
unused			RFXF				

If the number of bytes accumulated in the FIFO is equal to or exceeds this 5-bit number, or if the receive FIFO contains a byte marked EOP, the receive FIFO exception RSR is activated. Setting this register to zero disables this function. However, a packet tagged EOP will still set the RSR exception.

RSR Receive Service Request 10010 R

7	6	5	4	3	2	1	0
each bit set to state of RSR							

All bits in this register reflect the same status, the state of the RSR bit in the EXS register. When this register is read, only those bits indicated by a 1 in the corresponding bit positions in the PSR register are enabled onto the microprocessor bus. The remaining bit positions on the microprocessor port pins remain in a high impedance state during a read. This allows up to eight 29C53AC transceivers connected to the same microprocessor bus to be polled for status with one read. This feature is useful, for example, in linecard applications where multiple 29C53AC devices are controlled by one microprocessor.

See also PSR (Position Selection Register) and XSR (Transmit Service Request).

SBC Spare Bit Control 10000 R, W

7	6	5	4	3	2	1	0
MFE	MDX	MS	SIE	MIE	MX	AXE	AX

All exceptions are generated at the beginning of the ISDN frame following the event which causes the exception.

MFE Multiframe function enable. When MFE = 1, the spare bit unit is in the multiframe mode. When MFE = 0, the 29C53AC will not perform any of the multiframing procedures.

MDX Multiframe Q/S data change exception indication. When MFE = 1, this bit is set to 1 if a Q/S bit quartet is received that is different from the previous one received, and a spare bit exception (SX in EXS) is generated. This bit is cleared upon reading SBC.

MS Multiframe sync indication. When MFE = 1, this bit indicates the multiframe synchronization status (1 = in sync, 0 = out of sync). When MS changes from 1 to 0, a spare bit exception is generated (SX in EXS). When MFE = 0, this bit is always a one.

SIE Single frame interrupt enable. Setting this bit to a 1 enables the generation of a spare bit exception (SX in EXS) every ISDN frame. The single frame exception does not have an indication as such, but the indication should be inferred if the SX bit in EXS and the SIE bit are set. If SIE = 0, no single frame exception is generated.

MIE Multiframe interrupt enable. When MFE = 1, setting MIE to a 1 enables the generation of a spare bit exception (SX in EXS) when the MX bit becomes set. MIE = 0 masks the MX bit from producing a spare bit exception.

MX Multiframe exception indication. When MFE = 1, this bit becomes set to 1 on the first frame of the 20 frame multiframe, indicating that new Q or S transmit data can be written to SBX, and that new Q or S receive data is available in SBR. MX is cleared upon reading SBC. If MFE = 0, MX is not set. At the TE the multiframe exception indication is not dependent on multiframe sync being established.

AXE Activation bit change exception enable. Setting AXE to a 1 enables the generation of a spare bit exception (SX in EXS) when AX becomes set. For AXE = 0, the A bit exception is suppressed.

AX Activation bit exception indication. This bit becomes set to 1 after a change in the received A bit value at the TE, only after the loop interface has acquired synchronization. The state of the A bit can be read in SBR. This bit is cleared upon reading SBC.

SBR Spare Bit Receive 00110 R

7	6	5	4	3	2	1	0
QS4/X	QS3/X	QS2/X	QS1/S	S/M	N	FA	A

(MFE = 1/MFE = 0)

QS1–QS4 Q or S bit quartet received. These bits are only valid when MFE = 1. QS1 is received first.

S S bit received. Valid only in LSS (TE) mode. When MFE = 1 the S bit is located at SBR.3, and when MFE = 0, at SBR.4.

M M bit received. Valid only in LSS mode. This bit is not indicated in SBR when MFE = 1.

N N bit received. Valid only in LSS mode.

FA FA bit received.

A A bit received. Valid only in LSS mode.

NOTE:

The Q and S bit quartets are updated every 20 frames, while the remaining bits are updated every frame.

SBX Spare Bit Transmit 00110 W (RT)

7	6	5	4	3	2	1	0
QS4/X	QS3/X	QS2/FAE#	QS1/S	S/M	N=FA	FA	A#

(MFE = 1/MFE = 0)

QS1–QS4 Q or S bit quartet transmission. These bits are only valid when MFE = 1. QS1 is transmitted first.

FAE# FA echo enable. Valid only when MFE = 0 and in LSS (TE) mode. If FAE# is 0, the 29C53AC automatically echoes the received FA bit from the NT in the FA bit position of its transmit frame. If FAE# is 1, the transmitted FA bit follows the state of bit SBR.1. The default is FAE# = 0, and the FA bit is echoed.

S S bit transmitted. Valid only in LSM (NT) modes. When MFE = 1, the S bit is located at SBR.3, and when MFE=0, at SBR.4. When MFE = 1, the S bit is transmitted in the frames of the multiframe when FA is not equal to 1.

M M bit transmitted. Valid only in NT mode and MFE = 0.

N = FA Control for the N bit. Valid only in the NT mode. If N = FA is set to 1 the N bit transmitted will equal the FA bit value. The N = FA bit should be set to 0 for normal operation so that the N bit will be the complement of the FA bit. The default is N = FA set to 0.

FA FA bit transmitted. When MFE = 0 (and FAE# = 1 for LSS mode) this bit controls the value of the transmitted FA bit (normally 0). If MFE = 1, this bit controls the value of the transmitted FA bit during frames not involved in the multiframe procedure.

A# Control for the A bit. Valid only in the NT mode. The complement of this bit is sent in the A bit position of the transmit frame. For the default value of zero the A bit is transmitted as a one. During activation, the A bit is set to zero during INFO 2 regardless of the state of A#.

SCR System Interface Control 00100 W (RT)

7	6	5	4	3	2	1	0
unused		B2M		B1M		SIM	

This register configures the system, or SLD interface. It defaults to 00H upon power up, which is the

SLD slave mode. In this mode, the 29C53AC expects to receive its timing reference from the SLD interface. Therefore, in a terminal or other application where the SLD interface will be a signal source, the SLD mode master mode should be programmed immediately after reset.

Bits 5, 4 B2 Mode

0 0 enable normal SLD transfers (default mode).

1 0 microprocessor intercept of B2

0 1 loop back B2 toward system interface

1 1 loop back B2 toward loop interface

Bits 3, 2 B1 Mode

0 0 enable normal SLD transfers (default mode).

1 0 microprocessor intercept of B1

0 1 loop back B1 toward system interface

1 1 loop back B1 toward loop interface

Bits 1, 0 System Interface Mode

0 0 SSS SLD slave (default mode). The 29C53AC SIDR and SCL pins are inputs, and the 29C53AC transmits data on SLD when SDIR is low

1 0 SSN SLD interface for intelligent NT2. The 29C53AC generates SCL and SDIR, and transmits data on SLD when SDIR is low

0 1 SSM SLD master. The 29C53AC generates SCL and SDIR, and transmits data on SLD when SDIR is high.

1 1 reserved

SDC SLD Data Transfer Configuration 00101 W (RT)

7	6	5	4	3	2	1	0
ID		CE	MP	MCS	MF	SS	SC

This register has no effect in SLD master mode (SSM).

ID No effect as control bit; reads "1, 0" to identify version described here.

CE Command Enable

0 Ignore commands received on the SLD line (except when RD and WR are both low during reset)

1 Enable execution of SLD commands

MP Multiple Transfer to SLD Master

0 respond to poll command received in control byte

1 respond immediately beginning in the next half of the SLD frame

MCS Multiple Byte Configuration and Status Transfer

0 use control byte only (one byte per SLD frame)

1 use both control and signaling bytes (two bytes per SLD frame)

MF Multiple Byte FIFO transfers (both directions)

0 use control byte only (one byte per SLD frame)

1 use both control and signaling bytes (two bytes per SLD frame)

SS Single Status Byte Transfer (29C53AC to SLD master)

0 respond to poll command received in SLD control byte

1 respond immediately beginning in the next half of the SLD frame

SC Single Command/Configuration Byte Transfer (SLD master to 29C53AC)

0 data follows in control byte of next frame

1 data follows in the same frame's signaling byte

SR Signaling Byte Receive 11011 R, W

7	6	5	4	3	2	1	0
data							

This address provides access to the receive signaling byte register pair in the SLD register bank. In SLD master mode, this register contains the received signaling (S) byte from the SLD link. This is typically signaling or status information read back from an SLD slave device. Register contents are only valid in SSM (SLD Master) mode.

SX Signaling Byte Transmit 11111 R, W

7	6	5	4	3	2	1	0
data							

This address provides access to the transmit signaling byte register pair in the SLD register bank. In SLD master mode, data placed in this register is transmitted over the SLD link in the S byte. This is typically signaling or status information sent to an SLD slave device. Register contents are only transmitted in SSM (SLD Master) mode.

XFI Transmit FIFO Input 01001 W

7	6	5	4	3	2	1	0
data							

This is the input address for the transmit FIFO. This register should not be read, as it will cause the previous contents of XFI to be entered into the FIFO, and the FIFO count (XFN) to be incremented. Writes to this register should be separated by 3 CLK cycles.

XFN Transmit FIFO Number 00101 R

7	6	5	4	3	2	1	0
0	0	number of free bytes					

This register indicates the number of empty bytes in the transmit FIFO. The count requires 5 CLK cycles to update after a write to XFI. XFN can only be read through the microprocessor bus and not through the SLD port. Undefined unless the D-channel processor is enabled.

XFXF Transmit FIFO Exception Fullness 01101 R, W

7	6	5	4	3	2	1	0
unused			XFXF				

If the number of untransmitted bytes in the transmit FIFO is equal to this 5-bit number, the transmit service request (XSR) bit is set in EXS.

XSR Transmit Service Request 10011 R

7	6	5	4	3	2	1	0
each bit set to state of XSR							

All bits in this register reflect the same status, the state of the XSR bit in the EXS register. When this register is read, only those bits indicated by a 1 in the corresponding bit positions in the PSR register are enabled onto the microprocessor bus. The remaining bit positions on the microprocessor port pins remain in a high impedance state during a read. This allows up to eight 29C53AC transceivers connected to the same microprocessor bus to be polled for status with one read. This feature is useful, for example, in linecard applications where multiple 29C53AC devices are controlled by one microprocessor.

See also PSR (Position Selection Register) and RSR (Receive Service Request).

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin .... V_{SS} −0.5V to V_{CC} to +0.5V
Maximum Voltage on V_{CC} with Respect to V_{SS} ..... +7V
Total Power Dissipation ..... 500 mW

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS V_{CC} = +5V ±5%; V_{SS} = 0V; T_A = 0°C to 70°C;

Typical Values are at T_A = 25°C and Nominal Power Supply Values

DIGITAL INTERFACES

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{ILK} I_{OLK}	Input/Output Leakage Current (Excluding LR+, LR−, LX+, LX−)			±10	μA	$V_{SS} \le V_{IN} \le V_{CC}$
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = +2.0 mA I_{OL} = 1.2 mA for P1−P4, SLD
V_{OH1}	Output High Voltage	2.4			V	I_{OH} = −400 μA
V_{OH2}	Output High Voltage	0.9 V_{CC}			V	I_{OH} = −40 μA
C	Pin Cap. (ex. LR±, LX±)			10	pF	

POWER SUPPLY CURRENT (Averaged over 1 ms)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
$I_{CC(P)}$	Power Down (Standby)		4	8	mA	SLD and CLK Active
$I_{CC(I)}$	Idle Operating Current		8	12	mA	Receiver, SLD, CLK Active
$I_{CC(N)}$	Normal Operating Current			20	mA	Everything is Active (Excluding Current for Output Loads)

A.C. Characteristics V_{CC} = 5V ±5%; V_{SS} = 0V; T_A = 0°C–70°C; CLK = 3.84 MHz

RECEIVER

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{RD}	Minimum Received Differential Pulse Voltage		300	400	mV	
Z_{IR}	LR+, LR− Input Impedance	30	60		KΩ	Each Pin
C_{IR}	LR+, LR− Input Capacitance		10	20	pF	Each Pin

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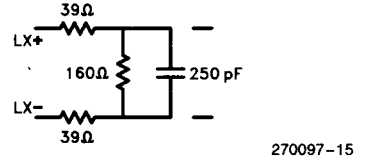
TRANSMITTER

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{XD}	Transmit Differential Pulse Voltage	1800	2000	2200	mV	R_L = 2000 (Note 1), R_L = 240
Z_{OX_1}	LX+, LX− Output Impedance	30	60		KΩ	Each Pin, Transmitting Binary One
Z_{OX_2}	LX+, LX− Output Impedance		2	5	Ω	Transmitting Binary Zero, Each Pin
C_{OX}	Output Capacitance		30	40	pF	Each Pin
C_L	Capacitive Load between LX+, LX−			1500	pF	Parallel with 300Ω Directly across LX+ and LX− (Note 2)
t_{MR}	Transmit Pulse Rise Time			400	ns	Test Load
I_{XL}	Source, Sink Current Limit			17	mA	R_L = 75
PHU	Pulse Height Unbalance		0.5	3	%	Test Load
t_{PW}	Pulse Width	5.16	5.21	5.26	μs	CLK = 3.84 MHz ±100 ppm (Note 3)

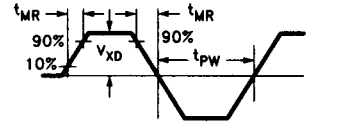
TIMING

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
J	Timing Extraction Jitter ("S" Slave Mode)	0		±5	%	
PD	Total Phase Deviation LX with Respect to LR	−7		+15	%	CLK = 3.84 MHz ±100 ppm

NOTES:
1. This is essentially the open circuit voltage.
2. This is a stability test. Overshoot less than 25%, damping time less than 1.5 μs.
3. Free running, measured between zero crossing of adjacent pulses. During DPLL adjustment in LSS (TE) mode, the framing pulse may be wider or narrower by one cycle of CLK (260 ns).



Transmitter Test Load



Differential Output
across LX+, LX− for V_{XD}
across 160Ω test circuit
load for t_{MR}, t_{PW}

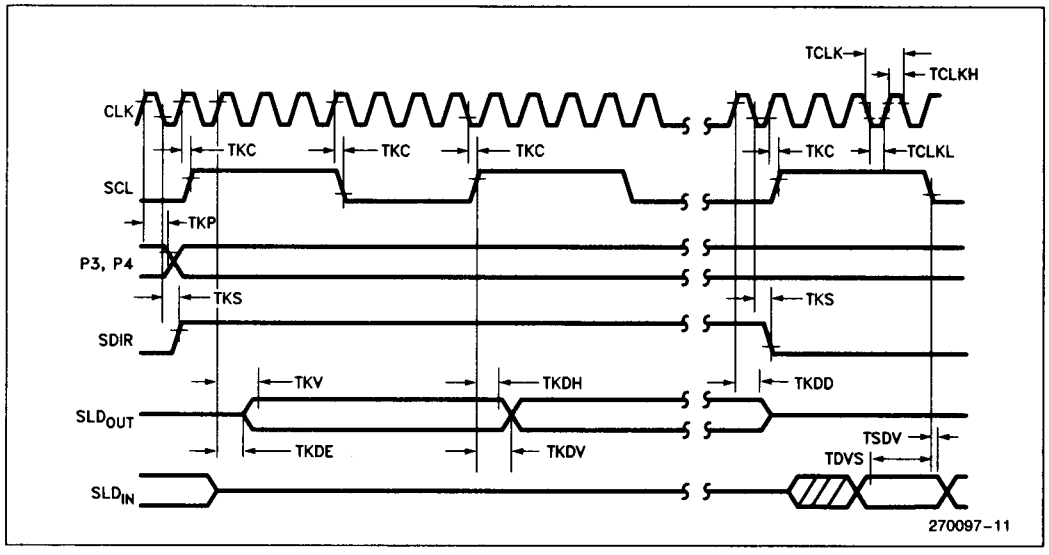


Figure 8. SLD Interface Timing (29C53AC As Master)

SLD INTERFACE TIMING (29C53AC as Master)

Symbol	Parameter	Min	Max	Units
TKC	CLK to SCL Delay		180	ns
TKS	CLK to SDIR Delay		180	ns
TKP	CLK to P3/P4 Delay(4)		150	ns
TKV	CLK to SLD Data Valid		150	ns
TKDE	CLK to SLD Driver Enabled	0		ns
TKDV	SCL to SLD Data Valid		150	ns
TKDH	SLD Data Hold After Clock Edge	0		
TKDD	CLK to SLD FLoat		150	ns
TDVS	SLD Data Input Setup Time to SCL	50		ns
TSDV	SLD Data Hold Time After SCL	80		ns
TCLK	CLK Period(5)	230	1000	ns
TCLKL	CLK Low Time	115	550	ns
TCLKH	CLK High Time	115	550	ns

NOTES:
1. 29C53AC samples SLD input data on SCL falling edge.
2. 29C53AC changes SLD output data on SCL rising edge.
3. 29C53AC SLD out is enabled 1½ CLK cycles after the SDIR rising edge and disabled ½ CLK cycle before the SDIR falling edge (as master only).
4. P3/P4, when programmed to output SLD status, changes state while SCL is low, approximately one CLK period ahead of SCL rising edge.
5. Range over which the 29C53AC will function. The frequency of CLK must be 3.84 MHz ±100 ppm to meet layer 1 recommendations for free running bit rate.

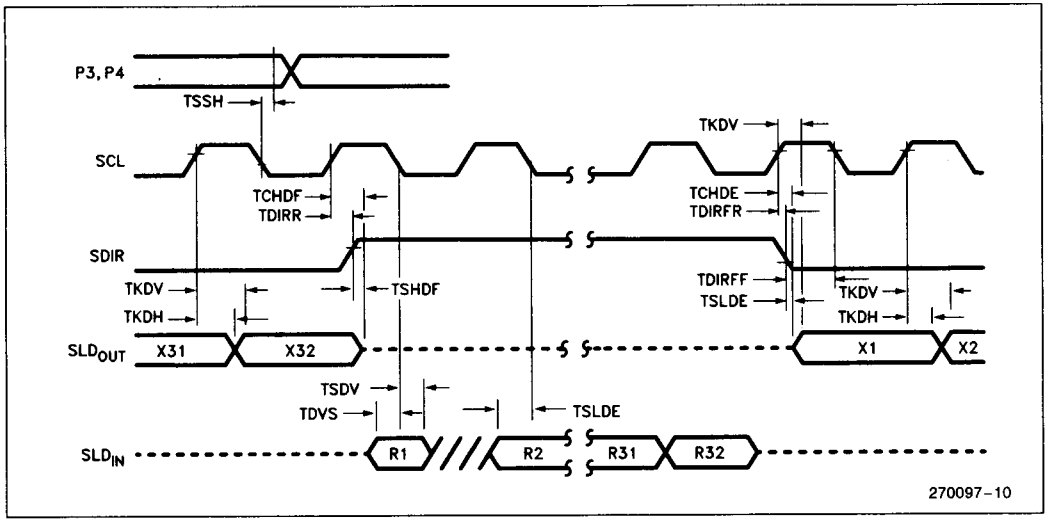


Figure 9. SLD Interface Timing (29C53AC As Slave)

SLD INTERFACE TIMING (29C53AC as Slave)

Symbol	Parameter	Min	Max	Units
TDIRR	SCL to SDIR Rising Edge	−130	130	ns
TDIRFR	SCL to SDIR Falling Edge	−150		ns
TDIRFF	SDIR to SCL Falling Edge	150		ns
TCHDF	SCL High to Data Out Float		50	ns
TSHDF	SDIR High to Data Out Float		50	ns
TKDH	Output Data Hold After SCL Edge	0		
TKDV	Output Data Valid After SCL Edge		100	ns
TDVS	SLD Input Data Setup Time	50		ns
TSDV	SLD Input Data Hold Time	80		ns
TCHDE	Enable SLD Output After SCL	0		ns
TSLDE	Enable SLD Output After SDIR	0		ns
TSSH	SLD Status Hold After SCL(3)	80	TCLK + TCLKL + 100	ns

NOTES:
1. 29C53AC samples SLD input data on SCL falling edge.
2. 29C53AC changes SLD output data on SCL rising edge.
3. P3/P4, when programmed to output SLD status, are generated on the first CLK rising edge after SCL high to low transition is detected. SCL is sampled on CLK falling edge.

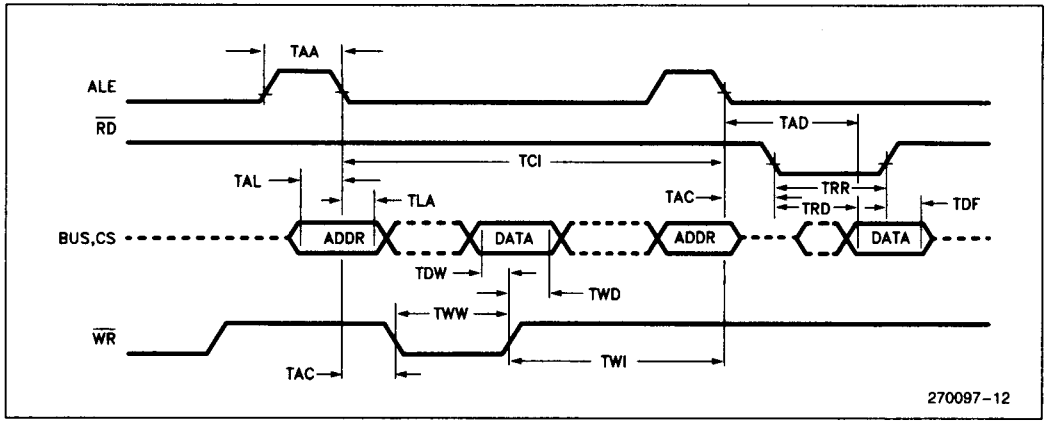
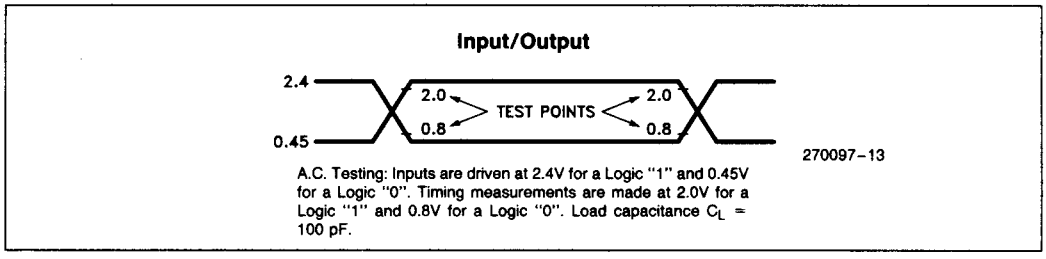


Figure 10. Microprocessor Bus Timing

MICROPROCESSOR BUS TIMING

Symbol	Parameter	Min	Max	Units
TAL	Address Setup Before ALE Trailing Edge	10		ns
TLA	Address Hold After ALE Trailing Edge	20		ns
TWW	Write Control Signal Width	100		ns
TDW	Data Setup Before $\overline{WR}$ Trailing Edge	40		ns
TWD	Data Hold After $\overline{WR}$ Trailing Edge	15		ns
TAA	ALE Pulse Width	30		ns
TWI	Active $\overline{CS}$ Cycle Disallowed After $\overline{WR}$(1)	2.5 × TCLK + 30		
TRR	Read Control Signal Width	100		ns
TRD	Access Time from $\overline{RD}$ Leading Edge		100	ns
TAD	Access Time from ALE Trailing Edge		250	ns
TDF	Float Delay After $\overline{RD}$ Trailing Edge		40	ns
TCI	Active $\overline{CS}$ Cycle Time for FIFO Access, RFO XFI for other registers	4 × TCLK 3 × TCLK 2 × TCLK		ns
TAC	ALE to Control Pulse	10		ns

NOTE:
1. Allow 3 extra clock cycles for GCR commands to execute.



A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0". Load capacitance C_L = 100 pF.

Figure 11. A.C. Testing Input, Output Waveform

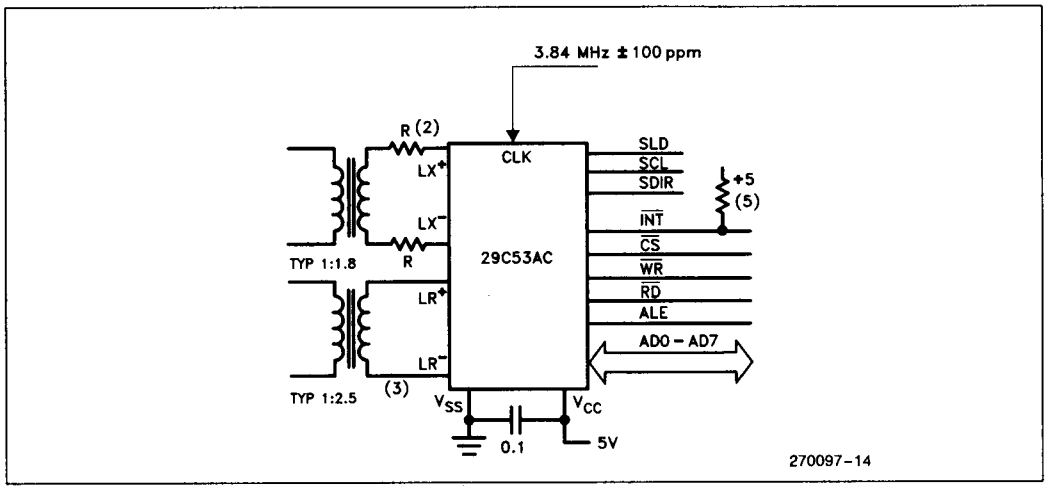


Figure 12. 29C53AC Application Diagram

NOTES:
1. The SLD port will be connected to an SLD master in NT applications, or to SLD slave devices such as the 29C48 programmable CODEC/Filter or appropriate data communication devices in TE applications.
2. Series resistance is used to increase the output impedance during transmission of a binary zero to greater than 20Ω on the loop side. It also serves as protection against surges when used in combination with external protection diodes.
3. A lower turns ratio (e.g., 1:1.8) may be used at the cost of a lower ratio of received signal to locally generated noise.
4. Appropriate protection circuitry can be added depending upon the application.
5. Pullup selected for approximately 1 mA I_{OL}.