

## Features

- Fully integrated, PLL-stabilized VCO
- Frequency range from 310 MHz to 440 MHz
- FSK through crystal pulling allows modulation from DC to 40 kbit/s
- High FSK deviation possible for wideband data transmission
- ASK achieved by on/off keying of internal power amplifier
- FM possible with external varactor
- Wide power supply range from 2.2 V to 5.5 V
- High over-all frequency accuracy
- Very low standby current
- Adjustable output power range from -12 dBm to +2 dBm
- Adjustable current consumption from 4.8 mA to 11.5 mA
- FSK deviation and center frequency independently adjustable
- Differential output well-suited for loop antenna
- External clock available for  $\mu$ C drive, down to 1.9 V supply
- "Clock only" mode
- Conforms to EN 300 220 and similar standards

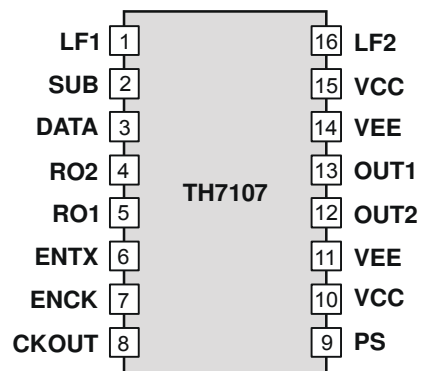
## Ordering Information

<i><b>Part No.</b></i>	<i><b>Temperature Code</b></i>	<i><b>Package Code</b></i>
TH7107	E (-40 °C to 85 °C)	FC (QSOP16)

## Application Examples

- Keyless car and central locking
- Low-power telemetry
- Alarm and security systems
- General digital data transmission
- General analog audio signal transmission

## Pin Description



## General Description

The TH7107 FSK/ASK/FM transmitter IC is designed for applications in the European 433MHz industrial-scientific-medical (ISM) band, according to the EN 300 220 telecommunications standard. It can also be used for any other system with carrier frequencies ranging from 310 MHz to 440 MHz (e.g. for applications in the US 315MHz ISM band).

The transmitter's carrier frequency  $f_c$  is determined by the frequency of the reference crystal  $f_{ref}$  that is used. The integrated PLL synthesizer ensures that each RF value, ranging from 310 MHz to 440 MHz, can be achieved by using a crystal with reference frequency according to:  $f_{ref} = f_c/N$ , where  $N = 32$  is the PLL feedback divider ratio.

**Document Content**

<b>1</b>	<b>Theory of Operation</b> .....	<b>3</b>
1.1	General.....	3
1.2	Block Diagram .....	3
<b>2</b>	<b>Functional Description</b> .....	<b>4</b>
2.1	FSK Modulation .....	4
2.2	Frequency Modulation .....	4
2.3	ASK Modulation.....	4
2.4	Mode Control Logic.....	4
<b>3</b>	<b>Pin Definition and Description</b> .....	<b>5</b>
<b>4</b>	<b>Electrical Characteristics</b> .....	<b>7</b>
4.1	Absolute Maximum Ratings .....	7
4.2	Normal Operating Conditions.....	7
4.3	Crystal Parameters.....	7
4.4	DC Characteristics.....	8
4.5	AC Characteristics.....	8
4.6	Output Power Selection.....	8
<b>5</b>	<b>Crystal Pulling</b> .....	<b>9</b>
5.1	Center Frequency as Function of CX1 and CX2 .....	9
5.2	Frequency Deviation as Function of CX1 and CX2 .....	10
<b>6</b>	<b>Test Circuit</b> .....	<b>11</b>
6.1	Test circuit component list (Fig. 4) .....	11
<b>7</b>	<b>Spectrum Plots</b> .....	<b>12</b>
<b>8</b>	<b>Package Information</b> .....	<b>14</b>
<b>9</b>	<b>Reliability Information</b> .....	<b>15</b>
<b>10</b>	<b>ESD Precautions</b> .....	<b>15</b>
<b>11</b>	<b>Disclaimer</b> .....	<b>16</b>

## 1 Theory of Operation

### 1.1 General

As depicted in Fig.1, the TH7107 transmitter consists of a fully integrated voltage-controlled oscillator (VCO), a divide-by-32 divider (div32), a phase-frequency detector (PFD) and a charge pump. An external loop filter at pin LF determines the dynamic behavior of the PLL and suppresses reference spurious signals. The VCO's output signal feeds the power amplifier (PA). RF signal power  $P_o$  can be adjusted in six steps from  $P_o = -12$  dBm to +2 dBm either by changing the value of resistor RPS or by varying the voltage  $V_{PS}$  at pin PS. The open-collector differential output (OUT1, OUT2) can be used to either directly drive a loop antenna or to be converted to a single-ended impedance by means of a balanced-to-unbalanced (balun) transformer. For maximum available output power, the differential output should be matched to a load of about 1 k $\Omega$ . Bandgap biasing ensures stable operation of the IC at a power supply range of 2.2 V to 5.5 V.

### 1.2 Block Diagram

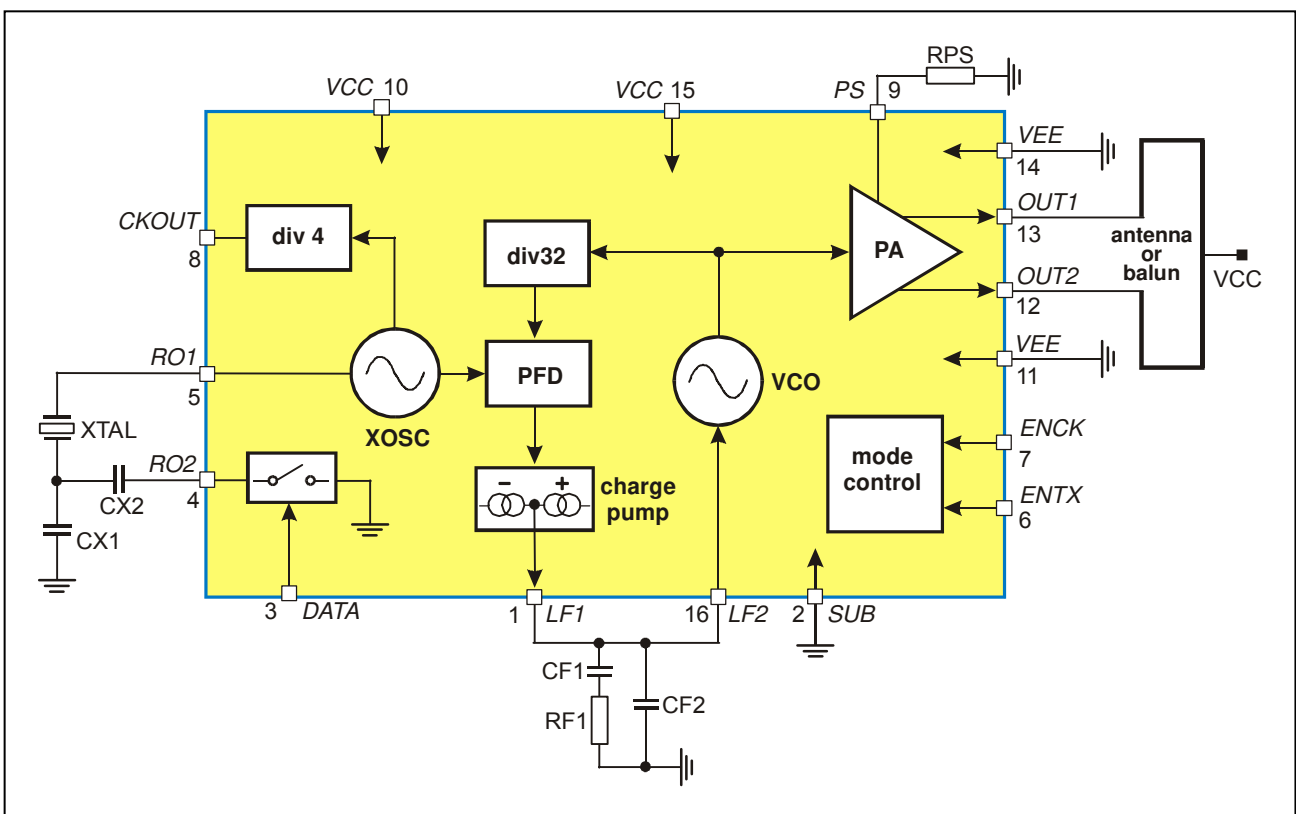


Fig. 1: Block diagram with external components

## 2 Functional Description

### 2.1 FSK Modulation

A Colpitts crystal oscillator (XOSC) is used as the reference oscillator of a phase-locked loop (PLL) synthesizer. FSK modulation is achieved by pulling the crystal (XTAL) through the data. So a CMOS-compatible data stream applied at input DATA digitally modulates the XOSC. Two external pulling capacitors CX1 and CX2 allow the FSK deviation and center frequency to be adjusted independently. At DATA = LOW CX2 is connected in parallel to CX1 leading to the low-frequency component of the FSK spectrum ( $f_{min}$ ); while at DATA = HIGH CX2 is deactivated and the XOSC is set to its high frequency, leading to  $f_{max}$ .

An external reference signal can be directly AC-coupled to pin RO1. Then the TH7107 is used without an XTAL. The reference signal has to contain the FSK (or FM) and sets the carrier frequency.

### 2.2 Frequency Modulation

For FM operation an external varactor is required. It simply acts as a pulling capacitor connected in series to the crystal. Then the analog modulation signal, applied through a series resistor, directly modulates the XOSC.

### 2.3 ASK Modulation

The TH7107 can be ASK-modulated by applying data directly at pin PS. This turns the PA on and off and therefore leads to an ASK signal at the output.

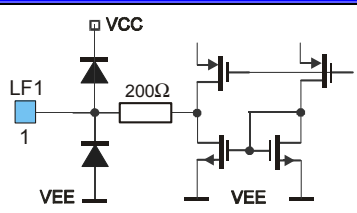
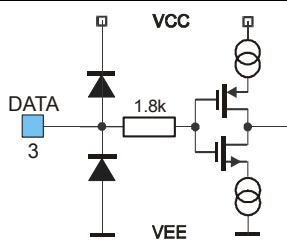
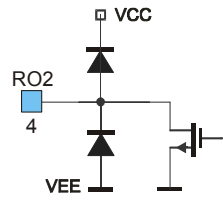
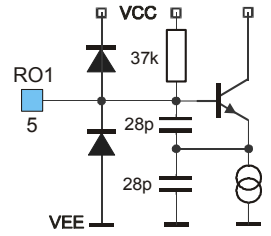
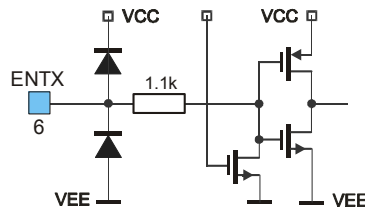
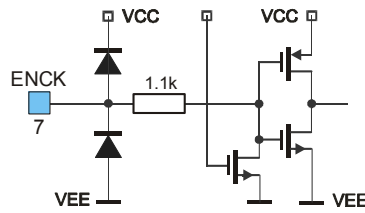
### 2.4 Mode Control Logic

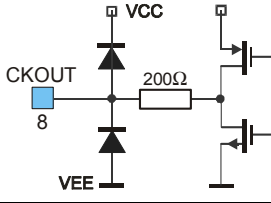
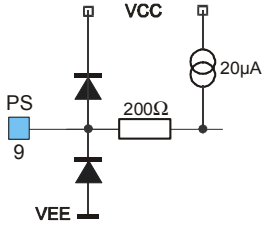
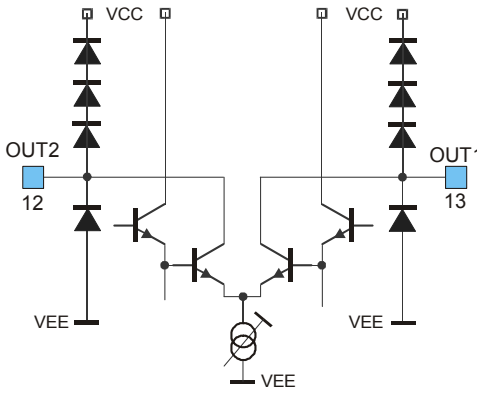
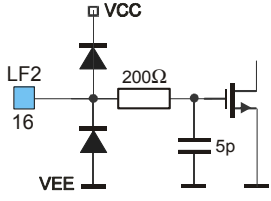
The mode control logic allows four different modes of operation as listed in the following table. The mode control pins ENCK and ENTX are pulled-down internally. This guarantees that the whole circuit is shut down if these pins are left floating.

The clock output CKOUT can be used to drive a  $\mu\text{C}$ . This output can be activated by the ENCK pin as required for any specific application. Clock frequency is 1/4 of the reference crystal frequency.

ENCK	ENTX	Mode	Description
0	0	all OFF	whole circuit in standby
0	1	TX only	TX active, no clock available
1	0	clock only	TX standby and clock available
1	1	all ON	TX active and clock available

### 3 Pin Definition and Description

Pin No.	Name	I/O Type	Functional Schematic	Description
1	LF1	output		charge pump output, connection to loop filter
2	SUB	ground		negative power supply, substrate connection
3	DATA	input		FSK data input, CMOS-compatible
4	RO2	analog I/O		XOSC FSK pulling pin, MOS switch
5	RO1	analog I/O		XOSC connection to XTAL, Colpitts type crystal oscillator
6	ENTX	input		mode control input, CMOS-compatible with internal pull-down
7	ENCK	input		mode control input, CMOS-compatible with internal pull-down

Pin No.	Name	I/O Type	Functional Schematic	Description
8	CKOUT	output		clock output, CMOS-compatible
9	PS	analog I/O		power-select and ASK input, high-impedance comparator logic  TX standby: $I_{PS} = 0$ TX active: $I_{PS} = 20\mu A$
10	VCC	supply		positive power supply
11	VEE	ground		negative power supply
12	OUT2	output		differential power amplifier output, open collector
13	OUT1	output		differential power amplifier output, open collector
14	VEE	ground		negative power supply
15	VCC	supply		positive power supply
16	LF2	input		VCO tuning input, connec- tion from loop filter

## 4 Electrical Characteristics

### 4.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	$V_{CC}$		0	7.0	V
Input voltage	$V_{IN}$		-0.3	$V_{CC}+0.3$	V
Storage temperature	$T_{STG}$		-65	150	°C
Junction temperature	$T_J$			150	°C
Thermal Resistance	$R_{thJA}$			112	K/W
Power dissipation	$P_{diss}$			0.12	W
Electrostatic discharge	$V_{ESD1}$	human body model, 1)	-1.0	+1.0	kV
	$V_{ESD2}$	human body model, 2)	-0.75	+0.75	

1) all pins except OUT1, OUT2      2) pins OUT1, OUT2

### 4.2 Normal Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	$V_{CC}$		2.2	5.5	V
Operating temperature	$T_A$		-40	85	°C
Input low voltage CMOS	$V_{IL}$	ENTX, ENCK, DTA pins		$0.3 \cdot V_{CC}$	V
Input high voltage CMOS	$V_{IH}$	ENTX, ENCK, DTA pins	$0.7 \cdot V_{CC}$		V
XOSC frequency	$f_{ref}$	set by the crystal	9.7	13.75	MHz
VCO frequency	$f_c$	$f_c = 32 \cdot f_{ref}$	310	440	MHz
Clock frequency	$f_{clk}$	$f_c = f_{ref} / 4$	2.4	3.4	MHz
FSK deviation	$\Delta f_{FSK}$	depends on CX1, CX2 and crystal parameter	$\pm 5$	$\pm 100$	kHz
Data rate FSK	$R_{FSK}$	NRZ		40	kbit/s
FM deviation	$\Delta f_{FM}$	adjustable with V1 and CX3		$\pm 6$	kHz
Modulation frequency FM	$f_{mod}$			5	kHz
Data rate ASK	$R_{ASK}$	NRZ		40	kbit/s

### 4.3 Crystal Parameters

Parameter	Symbol	Condition	Min	Max	Unit
Crystal frequency	$f_0$	fundamental mode, AT	9.7	13.75	MHz
Load capacitance	$C_L$		10	15	pF
Static capacitance	$C_0$			7	pF
Resonance resistance	$R_1$			60	$\Omega$
Spurious response	$a_{spur}$	only required for FSK		-10	dB

#### 4.4 DC Characteristics

all parameters under normal operating conditions, unless otherwise stated;  
typical values at  $T_A = 23\text{ }^\circ\text{C}$  and  $V_{CC} = 3\text{ V}$

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Standby current	$I_{SBY}$	ENCK=0, ENTX=0		0.05	0.1	$\mu\text{A}$
Clock only current	$I_{CLK}$	ENCK=1, ENTX=0	0.7	0.9	1.6	mA
Operating current	$I_{CC}$	ENCK=x, ENTX=1, RPS=56k $\Omega$	6	8.6	12	mA
Input current	$I_{IN}$	DATA=x, ENCK=0, ENTX=0	-1		1	$\mu\text{A}$
Pull down current	$I_{PD}$	ENCK=1, ENTX=1	3	8	30	$\mu\text{A}$
Pull up current	$I_{PS}$	ENCK=1, ENTX=1	14	20	24	$\mu\text{A}$
MOS switch On resistance	$R_{ON}$	DATA=0, ENTX=1	10	25	80	$\Omega$

#### 4.5 AC Characteristics

all parameters under normal operating conditions, unless otherwise stated;  
typical values at  $T_A = 23\text{ }^\circ\text{C}$  and  $V_{CC} = 3\text{ V}$ ;  
ENCK = 1, ENTX = 1, RPS = 56 k $\Omega$ ,  $f_c = 433.6\text{ MHz}$ , test circuit shown in Fig. 4

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output power	$P_o$			-1		dBm
Reference spurs	$P_{ref}$	@ $f_c \pm f_{ref}$		-44		dBm
Clock spurs	$P_{clk}$	@ $f_c \pm f_{clk}$		-44		dBm
Harmonic content	$P_{harm}$	@ $2f_c, 3f_c, 4f_c$		-40		dBm
Spurious output signal	$P_{off}$	$V_{PS} \leq 0.1\text{ V}$		-60		dBm
Phase noise	PN	@ $f_c \pm 200\text{ kHz}$		-83	-79	dBc/Hz
VCO gain	$K_{VCO}$			200		MHz/V
Charge pump current	$I_{CP}$			$\pm 260$		$\mu\text{A}$
Clock voltage swing	$V_{CKOUT}$	$C_{load} = 5\text{ pF}$		2		$V_{pp}$
Start-up time	$t_{on}$	from "all OFF" to any other mode		1.2	1.4	ms

#### 4.6 Output Power Selection

typical values at  $T_A = 23\text{ }^\circ\text{C}$  and  $V_{CC} = 3\text{ V}$ ;  
ENCK = 1, ENTX = 1,  $f_c = 433.6\text{ MHz}$ , test circuit shown in Fig. 4

RPS / k $\Omega$	$\geq 68$	56	47	39	27	15
$V_{PS} / \text{V}$	$\geq 2$	1.1	0.9	0.7	0.5	0.3
$I_{CC} / \text{mA}$	11.5	8.6	7.3	6.2	5.3	4.8
$P_o / \text{dBm}$	2	-1	-4	-7	-10	-12
$P_{harm} / \text{dBm}$	$\leq -40$	$\leq -40$	$\leq -40$	$\leq -45$	$\leq -45$	$\leq -50$



## 5 Crystal Pulling

### 5.1 Center Frequency as Function of CX1 and CX2

The center frequency  $f_c$  is defined as  $(f_{max} + f_{min}) / 2$ .

typical values at  $T_A = 23\text{ }^\circ\text{C}$  and  $V_{CC} = 3\text{ V}$ :

XTAL = 13.55 MHz, Cload = 15 pF, shown in Fig. 2

	CX2 = 1 nF	CX2 = 100 pF	CX2 = 47 pF
CX1 / pF	$f_c$ / MHz	$f_c$ / MHz	$f_c$ / MHz
22	433.612	433.619	433.625
32	433.604	433.610	433.614
40	433.598	433.604	433.608
49	433.596	433.601	433.604
61	433.593	433.598	433.600
104	433.587		

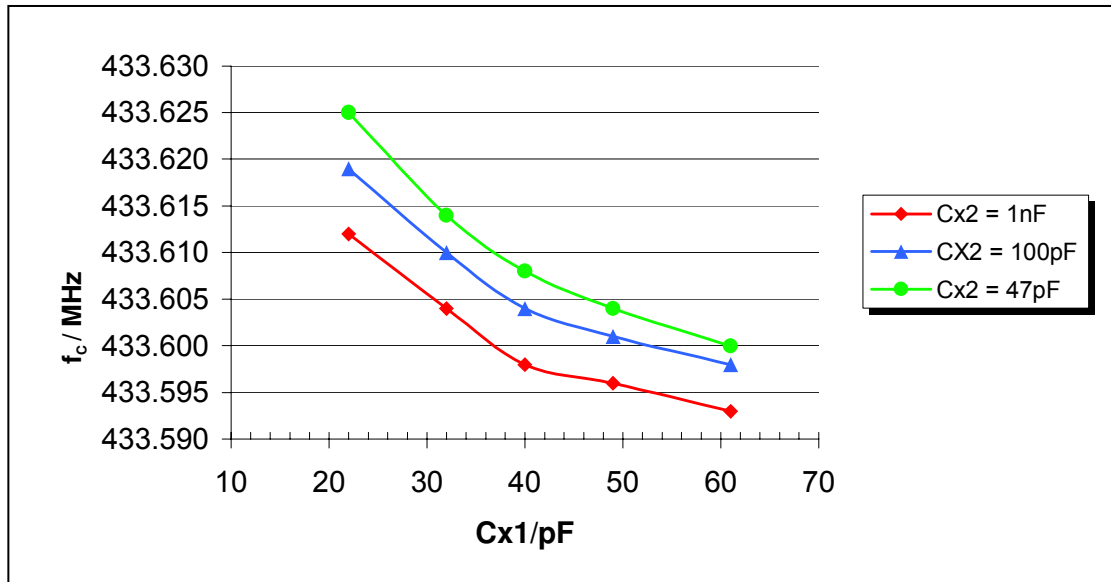


Fig. 2: Center frequency vs. CX1, at different CX2

## 5.2 Frequency Deviation as Function of CX1 and CX2

The frequency deviation  $\Delta f$  is defined as  $(f_{\max} - f_{\min}) / 2$ .

typical values at  $T_A = 23\text{ }^\circ\text{C}$  and  $V_{CC} = 3\text{ V}$ :

XTAL = 13.55 MHz, Clod = 15 pF, shown in Fig. 3

	CX2 = 1 nF	CX2 = 100 pF	CX2 = 47 pF
CX1 / pF	$\pm \Delta f$ / kHz	$\pm \Delta f$ / kHz	$\pm \Delta f$ / kHz
22	34	27	21
32	25	19	14
40	20	14	10
49	17	11.5	8
61	13	9	5.5
104	8		

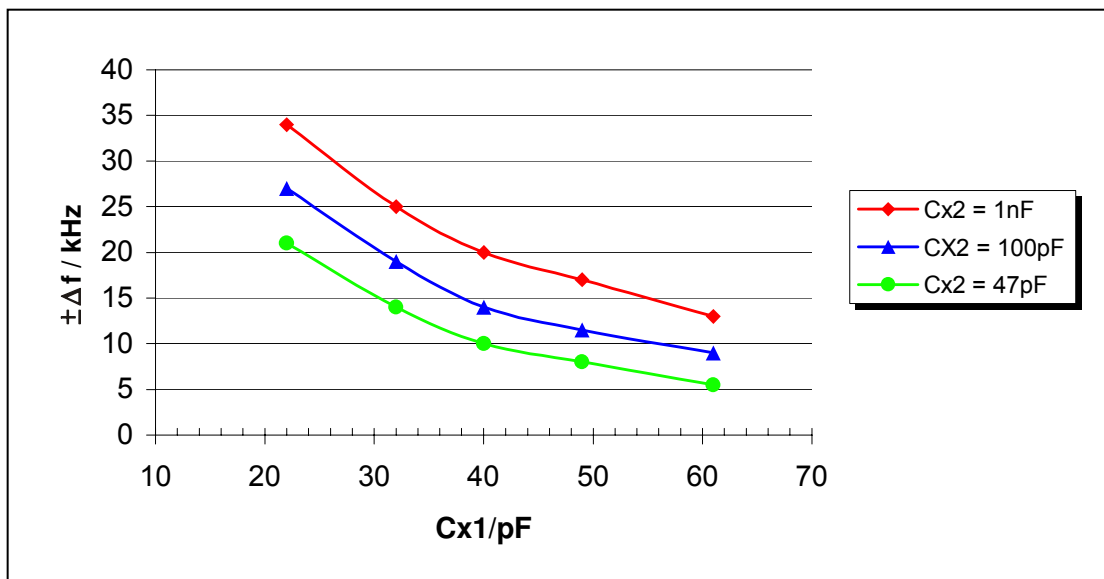
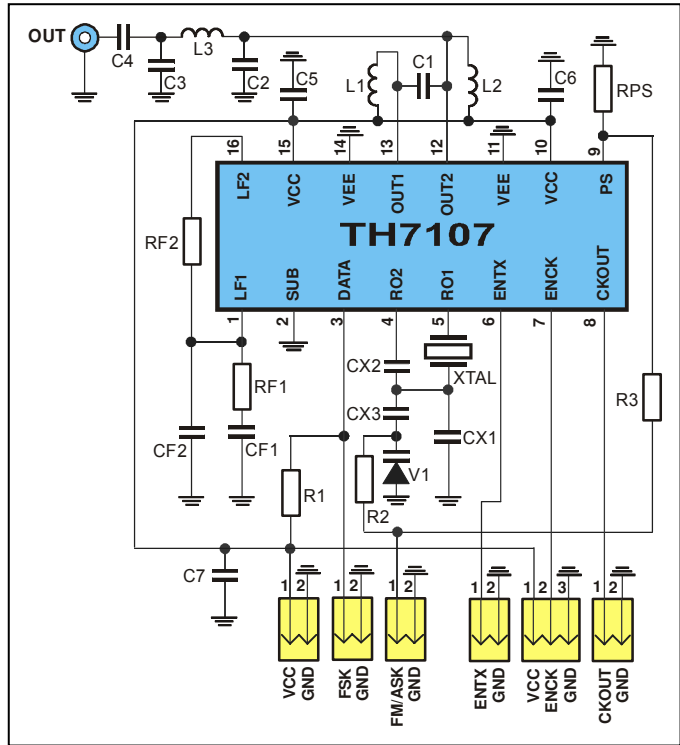


Fig. 3: Frequency deviation vs. CX1, at different CX2

### 6 Test Circuit

Fig. 4: Test circuit for FSK, ASK and FM; with 50Ω matching network



#### 6.1 Test circuit component list (Fig. 4)

Part	Size	Value	Tolerance	Description
CF1	0603	10 nF	±10%	loop filter capacitor
CF2	0603	12 pF	±10%	loop filter capacitor
CX1_FSK	0603	39 pF	±5%	XOSC capacitor for FSK ( $\Delta f = \pm 20$ kHz), <b>note 1</b>
CX1_ASK	0603	68 pF	±5%	XOSC capacitor for ASK, trimmed to $f_c$ , <b>note 1</b>
CX2	0603	1 nF	±5%	XOSC capacitor (for FSK only), <b>note 1</b>
CX3	0603	1 nF	±10%	XOSC capacitor (for FM only)
C1	0603	2.7 pF	±5%	impedance matching capacitor
C2	0805	0.68 pF	±5%	impedance matching capacitor
C3	0805	3.9 pF	±5%	impedance matching capacitor
C4	0603	150 pF	±5%	impedance matching capacitor
C5	0603	330 pF	±10%	blocking capacitor
C6	0603	330 pF	±10%	blocking capacitor
C7	1206	220 nF	±20%	blocking capacitor
L1	0603	22 nH	±5%	impedance matching inductor
L2	0603	22 nH	±5%	impedance matching inductor
L3	0805	33 nH	±5%	impedance matching inductor
RF1	0805	2.0 kΩ	±10%	loop filter resistor
RF2	0805	4.3 kΩ	±10%	loop filter resistor
RPS	0805	56 kΩ	±10%	power-select resistor
R1	0805	470 kΩ	±10%	optional pull-up resistor
R2	0805	30 kΩ	±10%	varactor bias resistor, (for FM only)
R3	0805	0 Ω	±10%	ASK jumper, (for ASK only)
V1	SOD323	BB535		varactor diode (for FM only)
XTAL	HC49/S	13.55 MHz fundamental wave	±30ppm calibr. ±30ppm temp.	crystal, $C_{load} = 12$ pF to 15 pF, $C_{0, max} = 7$ pF, $R_{m, max} = 40$ Ω

**Note 1:** value depends on crystal parameters

## 7 Spectrum Plots

All plots depict TH7107's typical performance at  $V_{CC} = 3.0\text{ V}$  and  $T_A = 23\text{ }^\circ\text{C}$ , derived with the test circuit shown in Fig. 4.

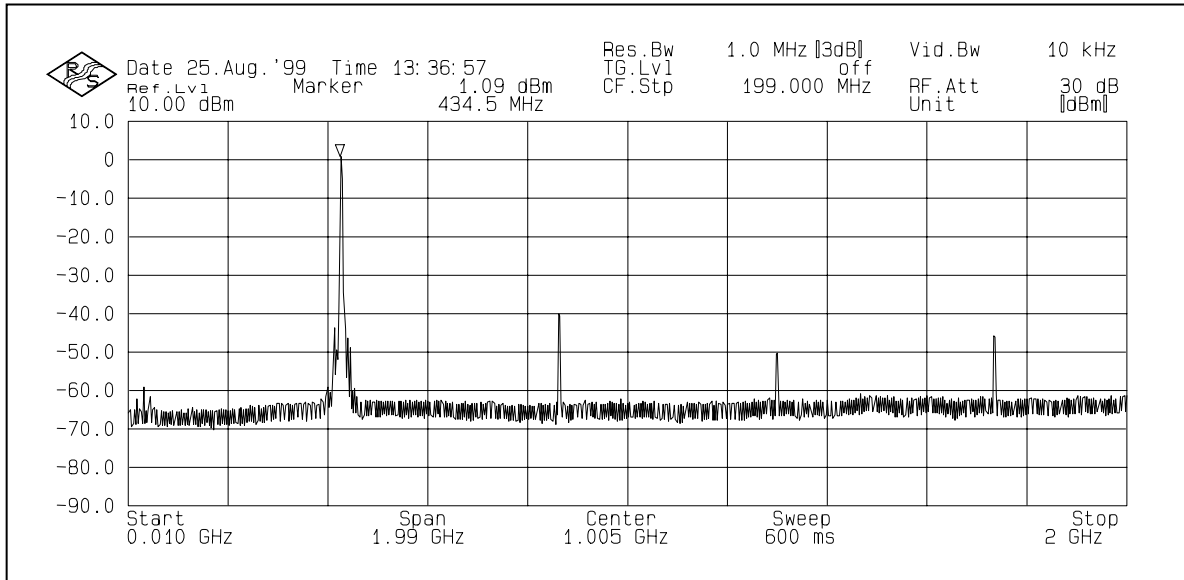


Fig. 5: RF output signal and spurious emissions, CW mode (DATA = HIGH)

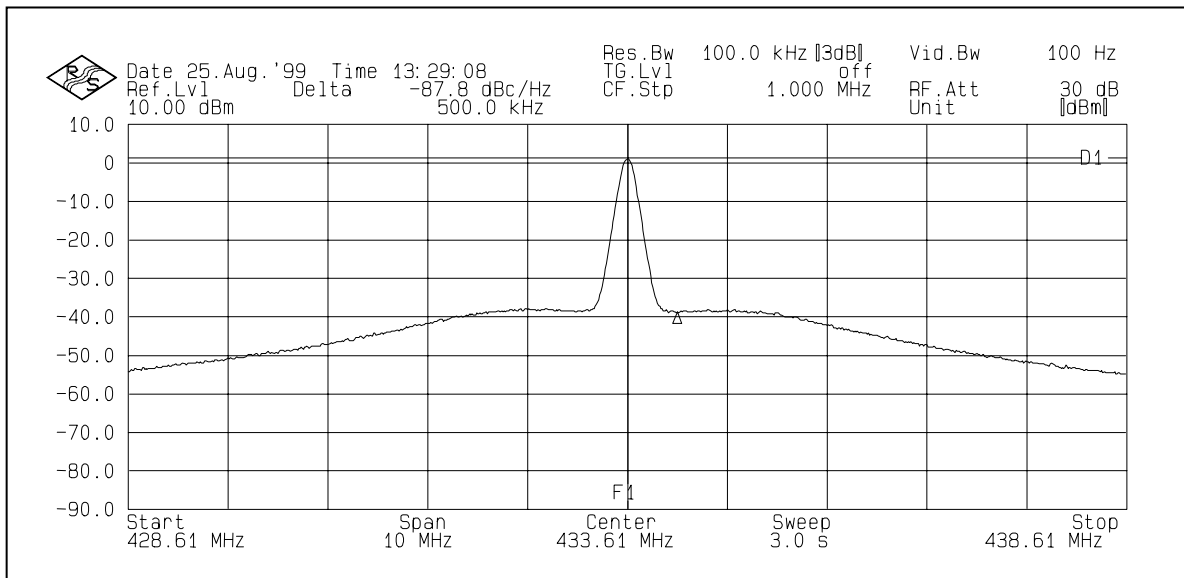


Fig. 6: Single-sideband phase noise at 500 kHz offset, CW mode (DATA = HIGH)

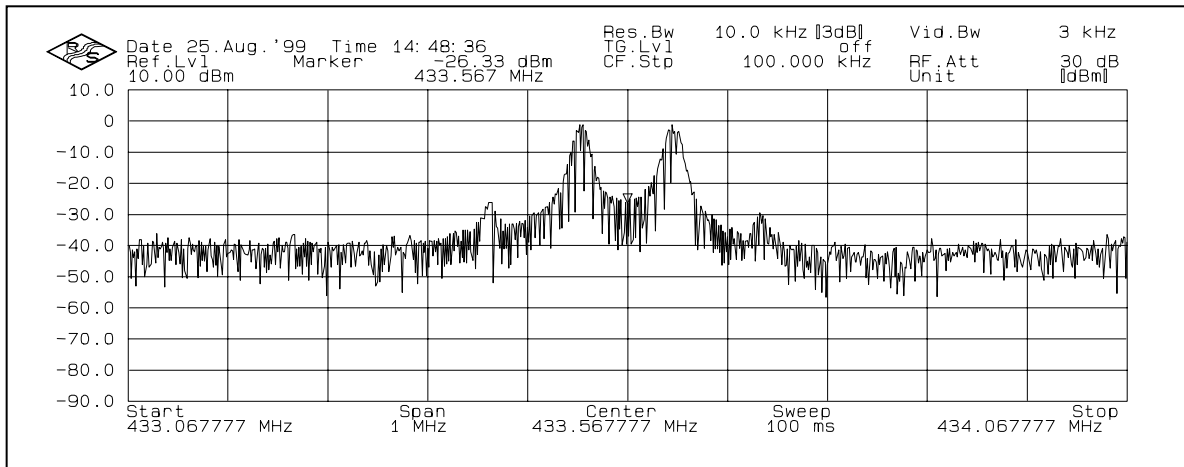


Fig. 7: FSK modulation with  $R_{FSK} = 6.6$  kbit/s NRZ

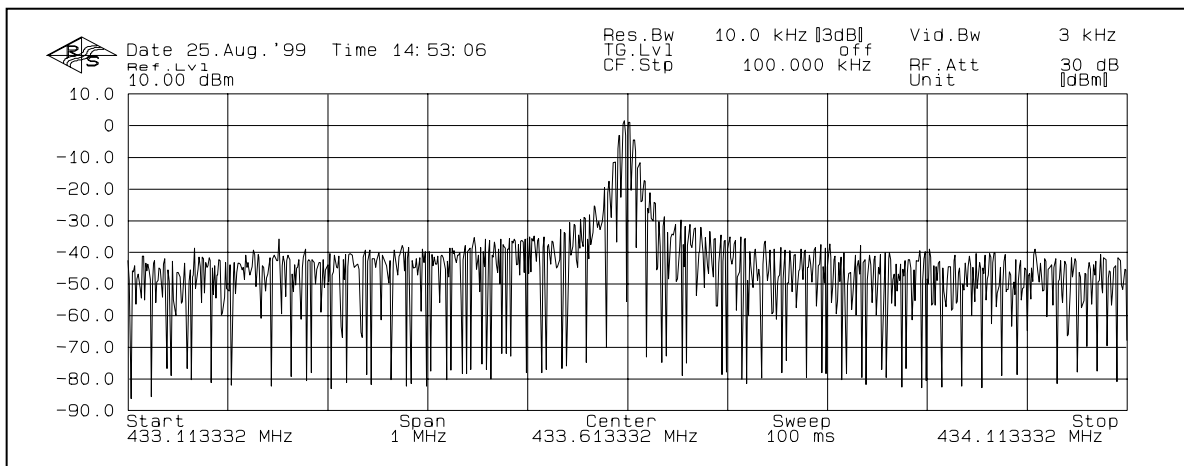


Fig. 8: ASK modulation with  $R_{ASK} = 4$  kbit/s NRZ

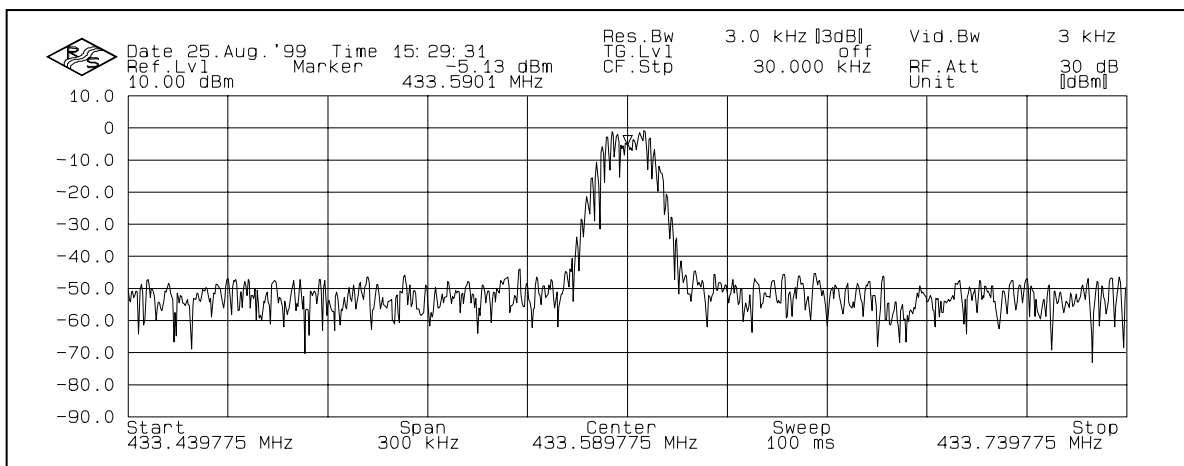


Fig. 9: FM with  $f_{mod} = 2$  kHz, FM input signal with  $1 V_{pp}$  around  $1.5 V_{DC}$ , DATA = HIGH

## 8 Package Information

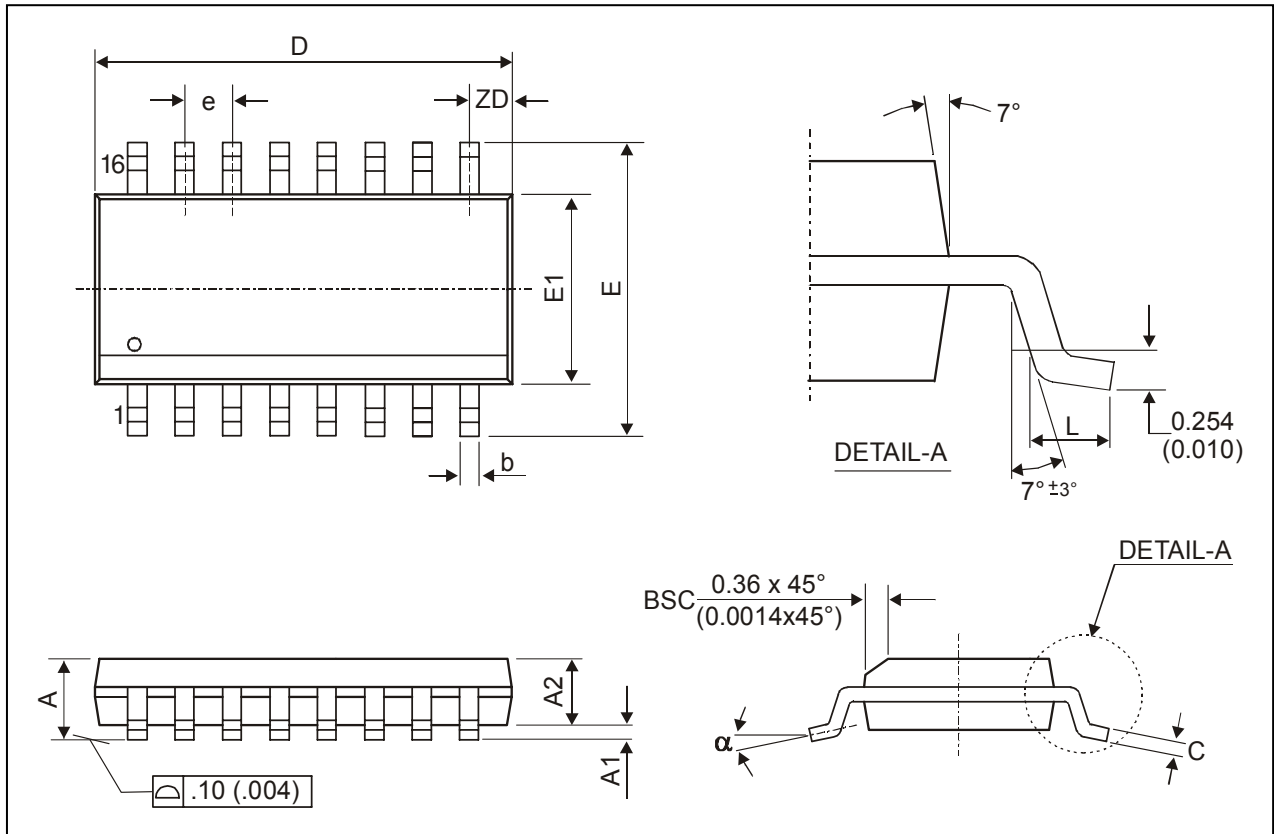


Fig. 10: QSOP16 (Quarter size Small Outline Package)

all Dimension in mm, coplanarity < 0.1mm												
	D	E1	E	A	A1	A2	e	b	ZD	C	L	$\alpha$
min	4.80	3.81	5.79	1.35	0.10	1.37	0.635	0.20	0.230	0.19	0.40	0°
max	4.98	3.99	6.20	1.75	0.25	1.50	0.635	0.30	0.230	0.25	1.27	8°
all Dimension in inch, coplanarity < 0.004"												
min	0.189	0.150	0.228	0.0532	0.0040	0.054	0.025	0.008	0.009	0.075	0.016	0°
max	0.196	0.157	0.244	0.0688	0.0098	0.059	0.025	0.012	0.009	0.098	0.050	8°

## **9 Reliability Information**

Melexis devices are classified and qualified regarding suitability for infrared, vapor phase and wave soldering with usual (63/37 SnPb-) solder (melting point at 183degC).

The following test methods are applied:

- IPC/JEDEC J-STD-020A (issue April 1999)  
Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface Mount Devices
- CECC00802 (issue 1994)  
Standard Method For The Specification of Surface Mounting Components (SMDs) of Assessed Quality
- MIL 883 Method 2003 / JEDEC-STD-22 Test Method B102  
Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

For more information on manufacturability/solderability see quality page at our website:  
<http://www.melexis.com/>

## **10 ESD Precautions**

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).

Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

## **Your Notes**

## **11 Disclaimer**

Devices sold by Melexis are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. Melexis makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Melexis reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with Melexis for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by Melexis for each application.

The information furnished by Melexis is believed to be correct and accurate. However, Melexis shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interrupt of business or indirect, special incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of Melexis' rendering of technical or other services.

© 2002 Melexis NV. All rights reserved.

---

For the latest version of this document. Go to our website at  
**[www.melexis.com](http://www.melexis.com)**

Or for additional information contact Melexis Direct:

**Europe and Japan:**  
Phone: +32 1367 0495  
E-mail: [sales\\_europe@melexis.com](mailto:sales_europe@melexis.com)

**All other locations:**  
Phone: +1 603 223 2362  
E-mail: [sales\\_usa@melexis.com](mailto:sales_usa@melexis.com)

QS9000, VDA6.1 and ISO14001 Certified