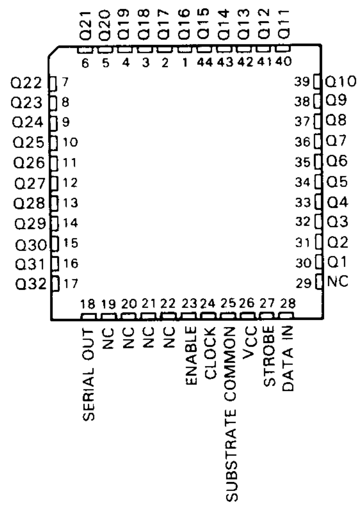
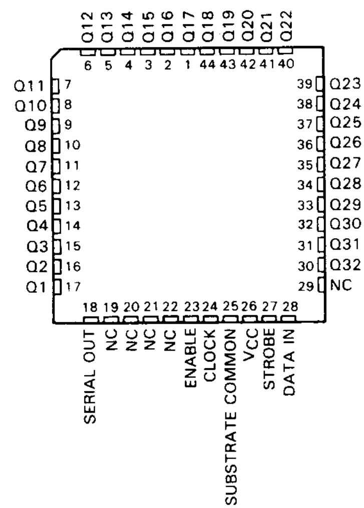
D2743, APRIL 1986

- Each Device Drives 32 Electrodes
- High-Voltage Open-Drain DMOS Outputs
- 50-mA Output Current Capability
- CMOS-Compatible Inputs
- Very Low Steady-State Power Consumption

SN55551 . . . FD PACKAGE
(TOP VIEW)



SN55552 . . . FD PACKAGE
(TOP VIEW)



NC—No internal connection

description

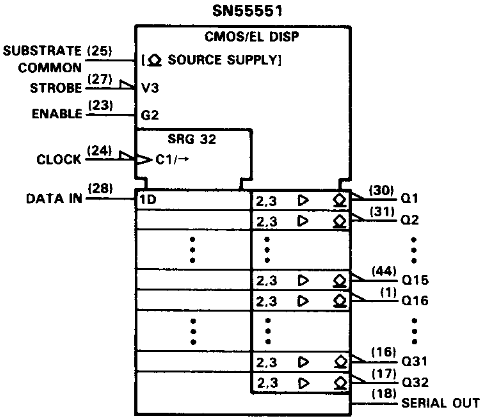
The SN55551 and SN55552 are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS-compatible and all outputs are high-voltage open-drain DMOS transistors. The SN55552 output sequence has been reversed from the SN55551 for ease in printed circuit board layout.

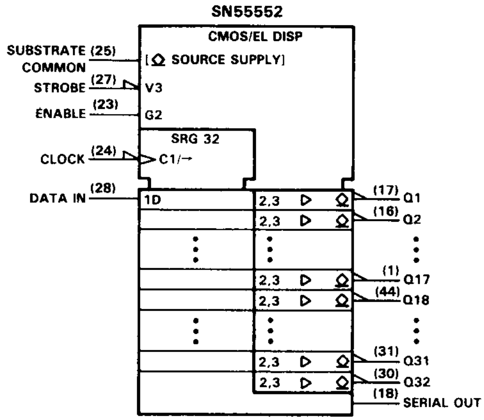
The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the Substrate Common terminal. Serial data is entered into the shift register on the high-to-low transition of the clock input. A high Enable input allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When the Strobe input is low, all output transistors are turned on. The Serial Data output from the shift register may be used to cascade additional devices. This output is not affected by the Enable or Strobe inputs.

The SN55551 and SN55552 are characterized for operation over the full military temperature range of −55°C to 125°C.

† BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

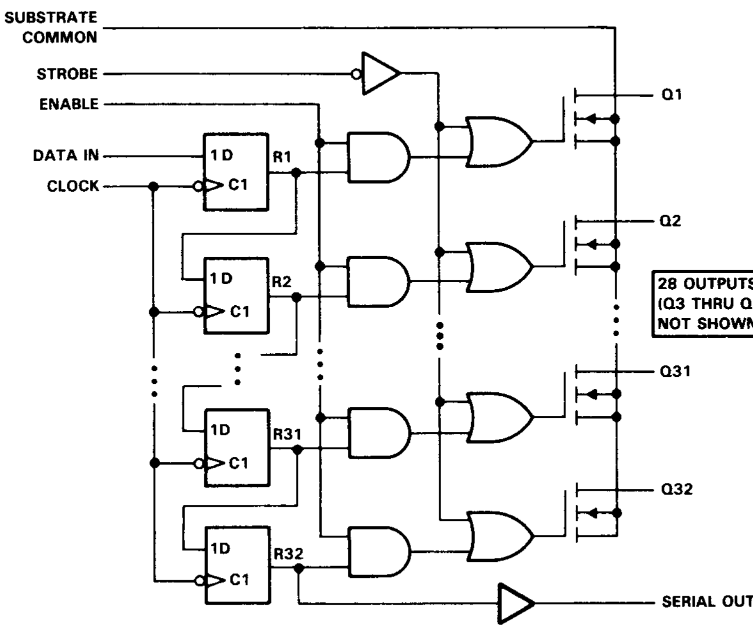
logic symbols†





† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. The symbol ◇ here indicates an n-channel open-drain output.

logic diagram (positive logic)



TEXAS INSTRUMENTS
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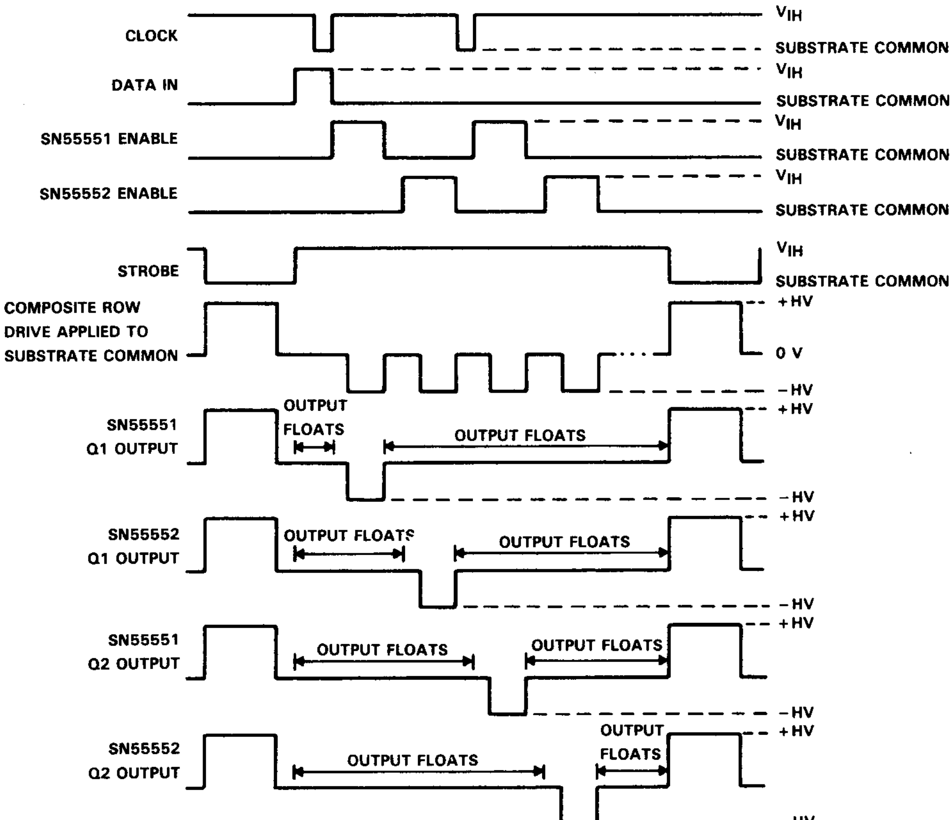
FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R32	OUTPUTS	
	CLOCK	ENABLE	STROBE		SERIAL	Q1 THRU Q32
LOAD	↓	X	X	Load and Shift†	R32	Determined by Enable and Strobe
	No. ↓	X	X	No Change	R32	Determined by Enable and Strobe
ENABLE	X	L	H	As determined above	R32	All Q outputs off
	X	H	H	As determined above	R32	Determined by R1 through R32
STROBE	X	X	L	As determined above	R32	All Q outputs on

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.
†Register R32 takes on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.

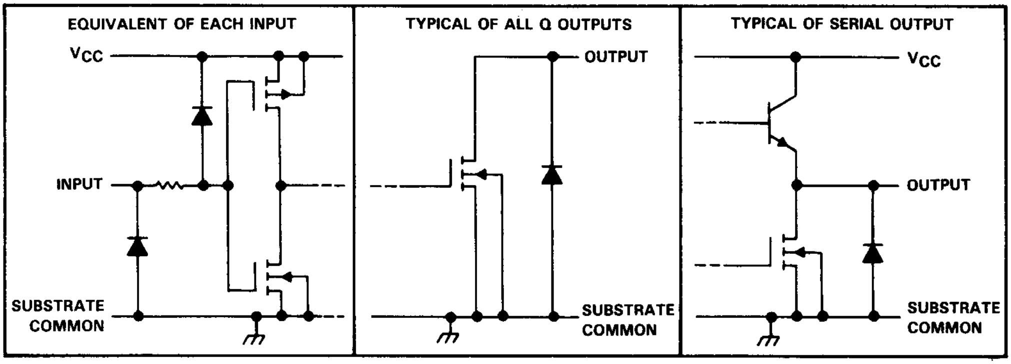
typical operating sequence



HV = high voltage

NOTE: During operation Clock, Data In, Enable, and Strobe are referenced to the Composite Row Drive signal received at the Substrate Common pin of the device.

schematic of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	18 V
Q off-state output voltage, $V_{O(off)}$	225 V
Input voltage	V_{CC} + 0.3 V
Substrate common terminal current (see Note 2)	1.5 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3)	1825 mW
Minimum operating free-air temperature	−55°C
Operating case temperature	125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds	260°C

NOTES: 1. Voltage values are with respect to substrate common terminal.
2. Duty cycle is limited by package dissipation.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 14.6 mW/°C.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			10.8	12	15	V
$V_{O(off)}$	Off-state Q output voltage			0		200	V
V_{IH}	High-level input voltage			0.75V_{CC}		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−0.3		0.25V_{CC}	V
$I_{O(on)}$	On-state Q output current	V_{DD} = 80 V, Duty cycle ≤ 1%	V_{CC} = 10.8 V, T_C = 25°C			50	mA
			V_{CC} = 15 V, T_C = 25°C			80	
f_{clock}	Clock frequency, T_A = 25°C					6.25	MHz
t_w	Clock pulse duration, high or low, T_A = 25°C			80			ns
t_{su}	Setup time, data valid before clock↓, T_A = 25°C			20			ns
t_h	Hold time, data valid after clock↓, T_A = 25°C			110			ns
T_A	Operating free-air temperature			−55			°C
T_C	Operating case temperature					125	°C

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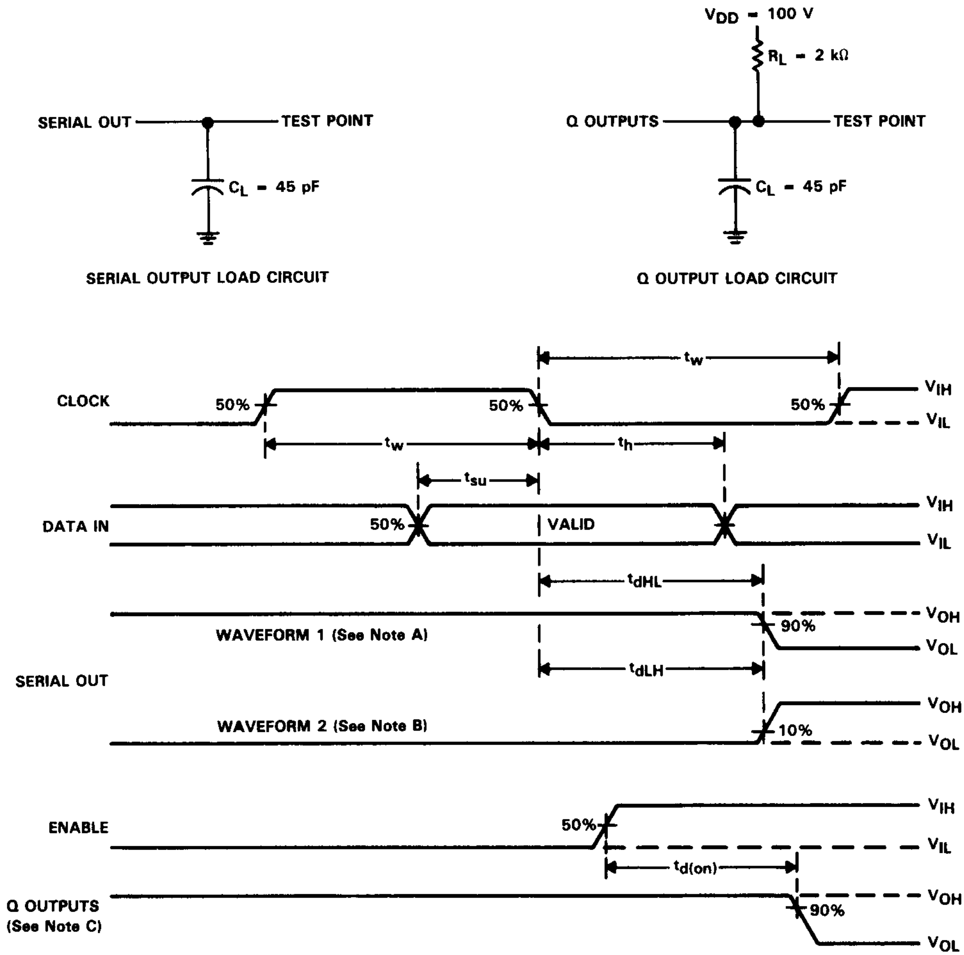
electrical characteristics over recommended operating temperature range, V_{CC} = 12 V, substrate common at 0 V

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Serial outputs	$I_O = -100\ \mu A$	10		V
V_{OL}	Low-level output voltage	Q outputs	$I_O = 50\ mA$		50	V
		Serial output	$I_O = 100\ \mu A$		1.5	
I_{IH}	High-level input current		$V_I = 12\ V$		5	μA
I_{IL}	Low-level input current		$V_I = 0$		−5	μA
$I_{O(off)}$	Off-state Q output current		$V_O = 200\ V$		50	μA
I_{CC}	Supply current				500	μA

switching characteristics, V_{CC} = 12 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{dLH}	Delay time, clock↓ to serial↓	C_L = 45 pF to common, See Figure 1		200	ns
t_{dHL}	Delay time, clock↓ to serial↑			200	ns
t_{dHL}	Delay time, enable to Q output↓	V_{DD} = 100 V, R_L = 2 kΩ, C_L = 45 pF to common, See Figure 1		500	ns

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. Waveform 1 is for internal conditions such that a low is clocked into R32.
B. Waveform 2 is for internal conditions such that a high is clocked into R32.
C. To measure $t_{d(on)}$, a high is stored in the associated register.

FIGURE 1. SWITCHING CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

MAXIMUM ON-STATE Q OUTPUT CURRENT
vs
SUPPLY VOLTAGE

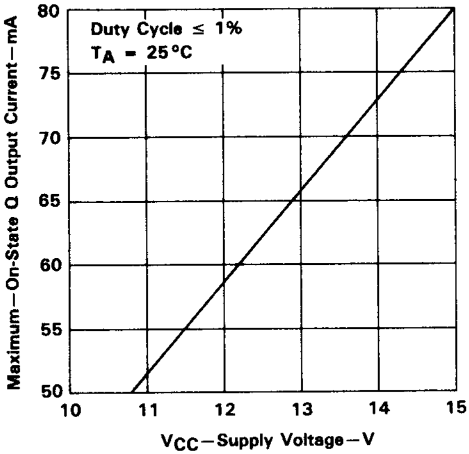


FIGURE 2

TYPICAL CHARACTERISTICS

OUTPUT CHARACTERISTICS SHOWING
SAFE OPERATION AREA (SOA)

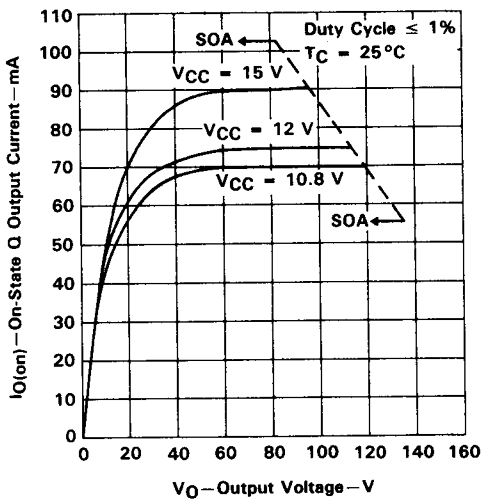


FIGURE 3

OUTPUT SATURATION CURRENT
vs
JUNCTION TEMPERATURE

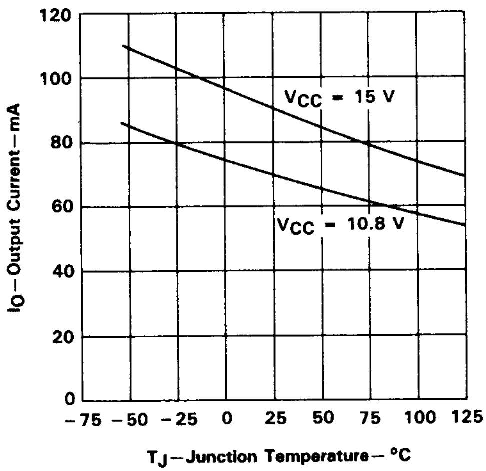


FIGURE 4