

+3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display Link-87.5 MHz

Check for Samples: [DS90C385A](#)

FEATURES

- Pin-to-Pin Compatible to DS90C383, DS90C383A and DS90C385
- No Special Start-Up Sequence Required between Clock/Data and /PD Pins. Input Signals (Clock and Data) can be Applied Either Before or After the Device is Powered.
- Support Spread Spectrum Clocking up to 100kHz Frequency Modulation and Deviations of $\pm 2.5\%$ Center Spread or -5% Down Spread
- "Input Clock Detection" Feature Will Pull All LVDS Pairs to Logic Low When Input Clock is Missing and When /PD Pin is Logic High
- 18 to 87.5 MHz Shift Clock Support
- Tx Power Consumption < 147 mW (typ) at 87.5MHz Grayscale
- Tx Power-Down Mode < 60 μ W (typ)
- Supports VGA, SVGA, XGA, SXGA(Dual Pixel), SXGA+(Dual Pixel), UXGA(Dual Pixel).
- Narrow Bus Reduces Cable Size and Cost
- Up to 2.45 Gbps Throughput
- Up to 306.25Megabyte/sec Bandwidth
- 345 mV (typ) Swing LVDS Devices for Low EMI
- PLL Requires No External Components
- Compliant to TIA/EIA-644 LVDS standard
- Low Profile 56-lead TSSOP Package

DESCRIPTION

The DS90C385A is a pin to pin compatible replacement for DS90C383, DS90C383A and DS90C385. The DS90C385A has additional features and improvements making it an ideal replacement for DS90C383, DS90C383A and DS90C385. family of LVDS Transmitters.

The DS90C385A transmitter converts 28 bits of LVCMOS/LVTTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over the fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 87.5 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 612.5Mbps per LVDS data channel. Using a 87.5 MHz clock, the data throughput is 306.25Mbytes/sec. This transmitter can be programmed for Rising edge strobe or Falling edge strobe through a dedicated pin. A Rising edge or Falling edge strobe transmitter will interoperate with a Falling edge strobe FPDLink Receiver without any translation logic.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces with added Spread Spectrum Clocking support.

Block Diagram

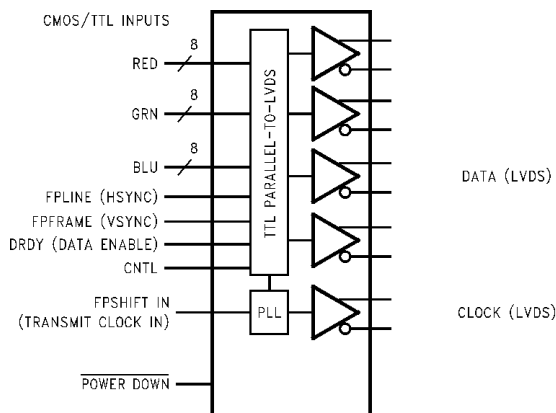


Figure 1. DS90C385A



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

| | | |
|--|----------------------------|------------------------------|
| Supply Voltage (V_{CC}) | | -0.3V to +4V |
| CMOS/TTL Input Voltage | | -0.5V to ($V_{CC} + 0.3V$) |
| LVDS Driver Output Voltage | | -0.3V to ($V_{CC} + 0.3V$) |
| LVDS Output Short Circuit Duration | | Continuous |
| Junction Temperature | | +150°C |
| Storage Temperature | | -65°C to +150°C |
| Lead Temperature (Soldering, 4 seconds) | | +260°C |
| Maximum Package Power Dissipation Capacity at 25°C | TSSOP Package | 1.63 W |
| Package Derating | | 12.5 mW/°C above +25°C |
| ESD Rating | HBM, 1.5k Ω , 100pF | 7kV |
| | EIAJ, 0 Ω , 200 pF | 500V |
| Latch Up Tolerance at 25°C | | ± 100 mA |

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Recommended Operating Conditions

| | Min | Nom | Max | Unit |
|--|-----|-----|------|------------------|
| Supply Voltage (V_{CC}) | 3.0 | 3.3 | 3.6 | V |
| Operating Free Air Temperature (T_A) | -10 | +25 | +70 | °C |
| Supply Noise Voltage (V_{CC}) | | | 200 | mV _{PP} |
| TxCLKIN frequency | 18 | | 87.5 | MHz |

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|---------------------------------------|---|--|--------------|-------|-----------------|------|----|
| LVCMOS/LVTTL DC SPECIFICATIONS | | | | | | | |
| V _{IH} | High Level Input Voltage | | 2.0 | | V _{CC} | V | |
| V _{IL} | Low Level Input Voltage | | 0 | | 0.8 | V | |
| V _{CL} | Input Clamp Voltage | I _{CL} = -18 mA | | -0.79 | -1.5 | V | |
| I _{IN} | Input Current | V _{IN} = 0.4V, 2.5V or V _{CC} | | +1.8 | +10 | μA | |
| | | V _{IN} = GND | -10 | 0 | | μA | |
| LVDS DC SPECIFICATIONS | | | | | | | |
| V _{OD} | Differential Output Voltage | R _L = 100Ω | 250 | 345 | 450 | mV | |
| ΔV _{OD} | Change in V _{OD} between complimentary output states | | | | 35 | mV | |
| V _{OS} | Offset Voltage ⁽¹⁾ | | 1.13 | 1.25 | 1.38 | V | |
| ΔV _{OS} | Change in V _{OS} between complimentary output states | | | | 35 | mV | |
| I _{OS} | Output Short Circuit Current | V _{OUT} = 0V, R _L = 100Ω | | -3.5 | -5 | mA | |
| I _{OZ} | Output TRI-STATE [®] Current | Power Down = 0V, V _{OUT} = 0V or V _{CC} | | ±1 | ±10 | μA | |
| TRANSMITTER SUPPLY CURRENT | | | | | | | |
| ICCTW | Transmitter Supply Current, Worst Case | R _L = 100Ω, C _L = 5 pF, Worst Case Pattern (Figure 2 Figure 4) "Typ" values are given for V _{CC} = 3.6V and T _A = +25°C, "Max" values are given for V _{CC} = 3.6V and T _A = -10°C | f = 25 MHz | | 31 | 45 | mA |
| | | | f = 40 MHz | | 37 | 50 | mA |
| | | | f = 65 MHz | | 48 | 60 | mA |
| | | | f = 87.5 MHz | | 55 | 65 | mA |
| ICCTG | Transmitter Supply Current, 16 Grayscale | R _L = 100Ω, C _L = 5 pF, 16 Grayscale Pattern (Figure 3 Figure 4) "Typ" values are given for V _{CC} = 3.6V and T _A = +25°C, "Max" values are given for V _{CC} = 3.6V and T _A = -10°C | f = 25 MHz | | 29 | 40 | mA |
| | | | f = 40 MHz | | 33 | 45 | mA |
| | | | f = 65 MHz | | 39 | 50 | mA |
| | | | f = 87.5 MHz | | 44 | 55 | mA |
| ICCTZ | Transmitter Supply Current, Power Down | Power Down = Low Driver Outputs in TRI-STATE [®] under Power Down Mode | | 17 | 150 | μA | |

(1) V_{OS} previously referred as V_{CM}.

Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|---|-------|------|-------|------|
| TCIT | TxCLK IN Transition Time (Figure 6) | 1.0 | | 6.0 | ns |
| TCIP | TxCLK IN Period (Figure 7) | 11.42 | T | 55.55 | ns |
| TCIH | TxCLK IN High Time (Figure 7) | 0.35T | 0.5T | 0.65T | ns |
| TCIL | TxCLK IN Low Time (Figure 7) | 0.35T | 0.5T | 0.65T | ns |
| TXIT | TxIN , and PWR DOWN pin Transition Time | 1.5 | | 6.0 | ns |
| TXPD | Minimum pulse width for PWR DOWN pin signal | 1 | | | us |

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | Min | Typ | Max | Unit | |
|--------|--|--|-------|-------|-------|----|
| LLHT | LVDS Low-to-High Transition Time (Figure 5) | | 0.75 | 1.4 | ns | |
| LHLT | LVDS High-to-Low Transition Time (Figure 5) | | 0.75 | 1.4 | ns | |
| TPPos0 | Transmitter Output Pulse Position (Figure 13) ⁽¹⁾ | f = 25MHz | -0.45 | 0 | +0.45 | ns |
| TPPos1 | Transmitter Output Pulse Position | | 5.26 | 5.71 | 6.16 | ns |
| TPPos2 | Transmitter Output Pulse Position | | 10.98 | 11.43 | 11.88 | ns |
| TPPos3 | Transmitter Output Pulse Position | | 16.69 | 17.14 | 17.59 | ns |
| TPPos4 | Transmitter Output Pulse Position | | 22.41 | 22.86 | 23.31 | ns |
| TPPos5 | Transmitter Output Pulse Position | | 28.12 | 28.57 | 29.02 | ns |
| TPPos6 | Transmitter Output Pulse Position | | 33.84 | 34.29 | 34.74 | ns |
| TPPos0 | Transmitter Output Pulse Position (Figure 13) ⁽¹⁾ | f = 40 MHz | -0.25 | 0 | +0.25 | ns |
| TPPos1 | Transmitter Output Pulse Position | | 3.32 | 3.57 | 3.82 | ns |
| TPPos2 | Transmitter Output Pulse Position | | 6.89 | 7.14 | 7.39 | ns |
| TPPos3 | Transmitter Output Pulse Position | | 10.46 | 10.71 | 10.96 | ns |
| TPPos4 | Transmitter Output Pulse Position | | 14.04 | 14.29 | 14.54 | ns |
| TPPos5 | Transmitter Output Pulse Position | | 17.61 | 17.86 | 18.11 | ns |
| TPPos6 | Transmitter Output Pulse Position | | 21.18 | 21.43 | 21.68 | ns |
| TPPos0 | Transmitter Output Pulse Position (Figure 13) ⁽¹⁾ | f = 65 MHz | -0.20 | 0 | +0.20 | ns |
| TPPos1 | Transmitter Output Pulse Position | | 2.00 | 2.20 | 2.40 | ns |
| TPPos2 | Transmitter Output Pulse Position for Bit 2 | | 4.20 | 4.40 | 4.60 | ns |
| TPPos3 | Transmitter Output Pulse Position for Bit 3 | | 6.39 | 6.59 | 6.79 | ns |
| TPPos4 | Transmitter Output Pulse Position | | 8.59 | 8.79 | 8.99 | ns |
| TPPos5 | Transmitter Output Pulse Position | | 10.79 | 10.99 | 11.19 | ns |
| TPPos6 | Transmitter Output Pulse Position | | 12.99 | 13.19 | 13.39 | ns |
| TPPos0 | Transmitter Output Pulse Position (Figure 13) ⁽¹⁾ | f = 87.5 MHz | -0.20 | 0 | +0.20 | ns |
| TPPos1 | Transmitter Output Pulse Position | | 1.48 | 1.68 | 1.88 | ns |
| TPPos2 | Transmitter Output Pulse Position | | 3.16 | 3.36 | 3.56 | ns |
| TPPos3 | Transmitter Output Pulse Position | | 4.84 | 5.04 | 5.24 | ns |
| TPPos4 | Transmitter Output Pulse Position | | 6.52 | 6.72 | 6.92 | ns |
| TPPos5 | Transmitter Output Pulse Position | | 8.20 | 8.40 | 8.60 | ns |
| TPPos6 | Transmitter Output Pulse Position | | 9.88 | 10.08 | 10.28 | ns |
| TSTC | Required TxIN Setup to TxCLK IN (Figure 7) at 85MHz | 2.5 | | | ns | |
| THTC | Required TxIN Hold to TxCLK IN (Figure 7) at 87.5 MHz | 0.5 | | | ns | |
| TCCD | TxCLK IN to TxCLK OUT Delay. Measure from TxCLK IN edge to immediately crossing point of differential TxCLK OUT by following the positive TxCLK OUT. 50% duty cycle input clock is assumed. (Figure 8) | T _A = -10°, and 87.5MHz for "Min", T _A = 70°, and 25MHz for "Max", V _{CC} = 3.6V, R _{FB} pin = VCC | 3.086 | | 7.211 | ns |
| | Measure from TxCLK IN edge to immediately crossing point of differential TxCLK OUT by following the positive TxCLK OUT. 50% duty cycle input clock is assumed. (Figure 9) | T _A = -10°, and 87.5MHz for "Min", T _A = 70°, and 25MHz for "Max", V _{CC} = 3.6V, R _{FB} pin = GND | 2.868 | | 6.062 | ns |

(1) The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).

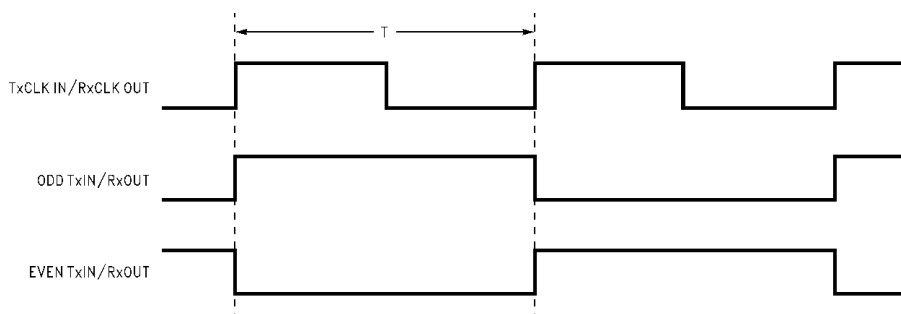
Transmitter Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|---|--------------|---------------------|-----|------|
| SSCG | Spread Spectrum Clock support; Modulation frequency with a linear profile. ⁽²⁾ | f = 25 MHz | 100kHz ±2.5%/-5% | | |
| | | f = 40 MHz | 100kHz ±2.5%/-5% | | |
| | | f = 65 MHz | 100kHz ±2.5%/-5% | | |
| | | f = 87.5 MHz | 100kHz ±2.5%/-5% | | |
| TPLLS | Transmitter Phase Lock Loop Set (Figure 10) | | | 10 | ms |
| TPDD | Transmitter Power Down Delay (Figure 12) | | | 100 | ns |

(2) Care must be taken to ensure TSTC and THTC are met so input data are sampling correctly. This SSCG parameter only shows the performance of tracking Spread Spectrum Clock applied to TxCLK IN pin, and reflects the result on TxCLKOUT+ and TxCLKOUT- pins.

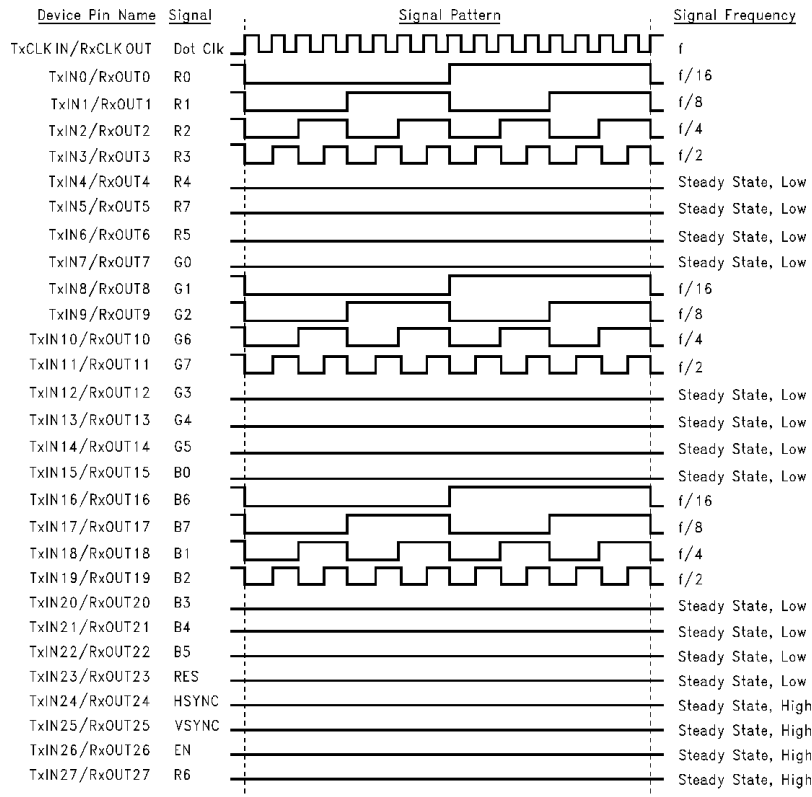
AC Timing Diagrams



- A. The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVCMOS/LVTTL I/O.
- B. Figure 2 and Figure 3 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Figure 2. "Worst Case" Test Pattern

AC Timing Diagrams (continued)



- A. The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.
- B. Figure 2 and Figure 3 show a falling edge data strobe (TxCLK IN/RxCLK OUT).
- C. Recommended pin to signal mapping. Customer may choose to define differently.

Figure 3. "16 Grayscale" Test Pattern - DS90C385A

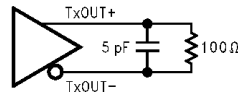


Figure 4. DS90C385A (Transmitter) LVDS Output Load. 5pF is shown as board loading

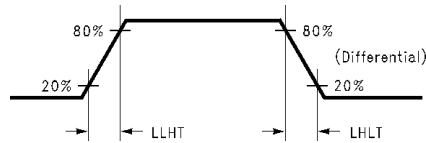


Figure 5. DS90C385A (Transmitter) LVDS Transition Times

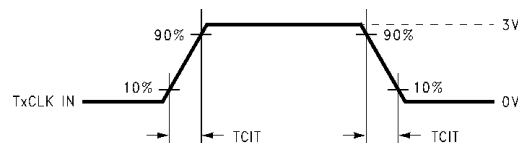


Figure 6. DS90C385A (Transmitter) Input Clock Transition Time

AC Timing Diagrams (continued)

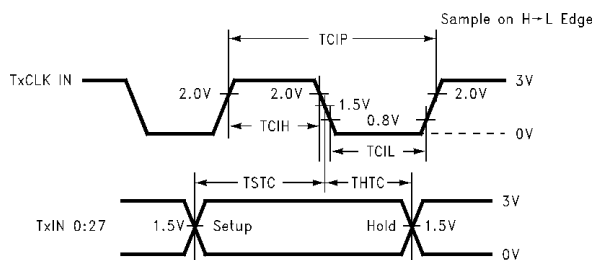


Figure 7. DS90C385A (Transmitter) Setup/Hold and High/Low Times with R_FB pin = GND (Falling Edge Strobe)

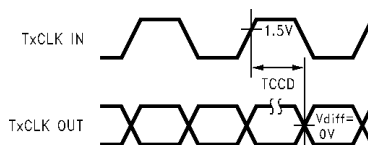


Figure 8. DS90C385A (Transmitter) Clock In to Clock Out Delay with R_FB pin = VCC

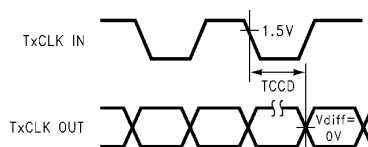


Figure 9. DS90C385A (Transmitter) Clock In to Clock Out Delay with R_FB pin = GND

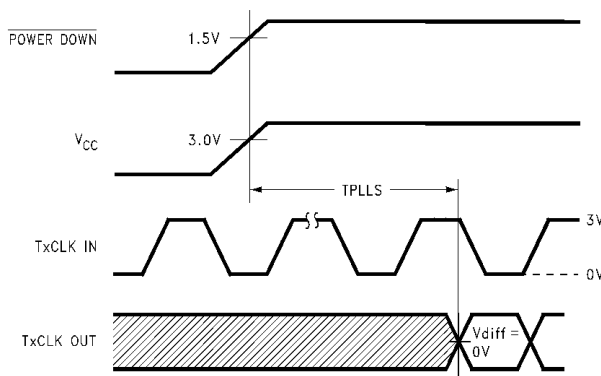


Figure 10. DS90C385A (Transmitter) Phase Lock Loop Set Time

AC Timing Diagrams (continued)

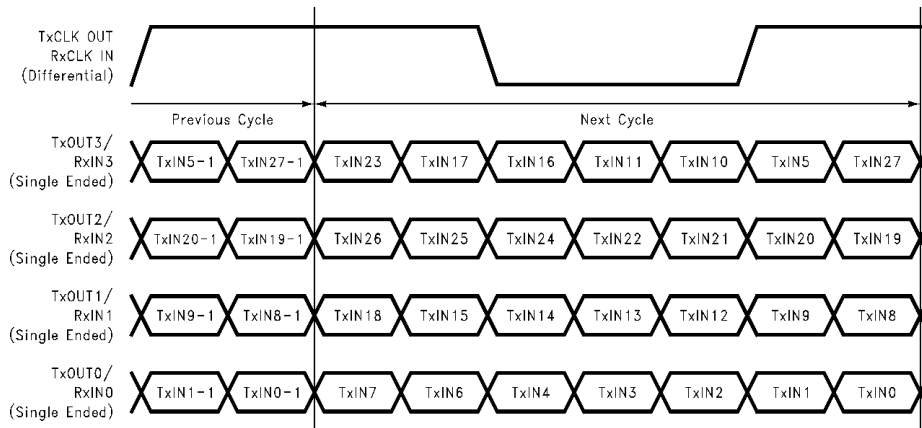


Figure 11. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs - DS90C385A

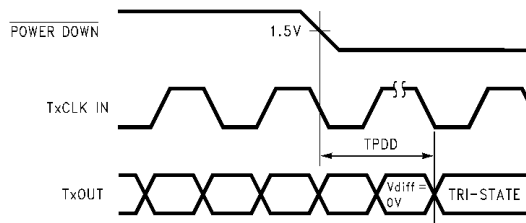


Figure 12. Transmitter Power Down Delay

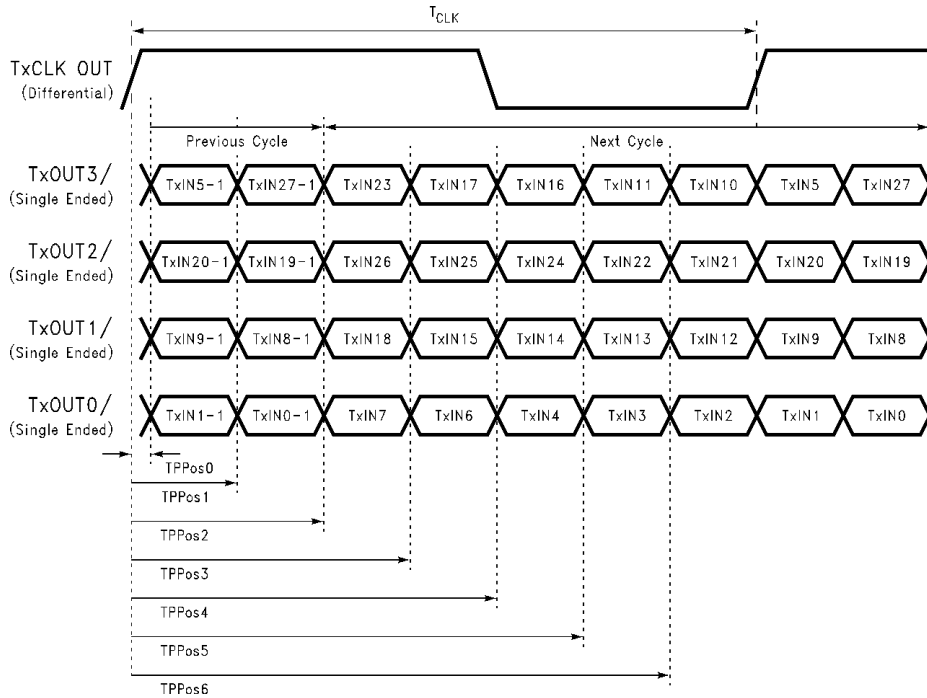
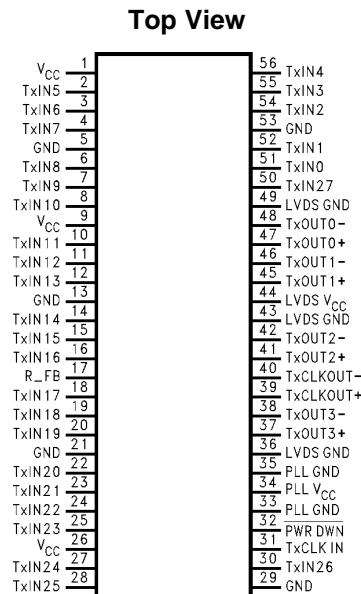


Figure 13. Transmitter LVDS Output Pulse Position Measurement - DS90C385A

DS90C385A DGG (TSSOP) Package Pin Descriptions — FPD Link Transmitter

| Pin Name | I/O | No. | Description |
|----------------------|-----|-----|---|
| TxIN | I | 28 | LVTTL level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable). |
| TxOUT+ | O | 4 | Positive LVDS differential data output. |
| TxOUT- | O | 4 | Negative LVDS differential data output. |
| TxCLKIN | I | 1 | LVTTL level clock input. Pin name TxCLK IN. |
| R_FB | I | 1 | LVTTL level programmable strobe select (See Table 1). |
| TxCLK OUT+ | O | 1 | Positive LVDS differential clock output. |
| TxCLK OUT- | O | 1 | Negative LVDS differential clock output. |
| PWR DOWN | I | 1 | LVTTL level input. When asserted (low input) TRI-STATE the outputs, ensuring low current at power down. |
| V _{CC} | I | 3 | Power supply pins for LVTTL inputs. |
| GND | I | 5 | Ground pins for LVTTL inputs. |
| PLL V _{CC} | I | 1 | Power supply pin for PLL. |
| PLL GND | I | 2 | Ground pins for PLL. |
| LVDS V _{CC} | I | 1 | Power supply pin for LVDS outputs. |
| LVDS GND | I | 3 | Ground pins for LVDS outputs. |

Pin Diagram for TSSOP Package



**Order Number DS90C385AMT
DGG Package**

APPLICATION INFORMATION

The DS90C385A is backward compatible with the DS90C385, DS90C383A, DS90C383 in TSSOP 56-lead package, and it is a pin-for-pin replacements.

This device DS90C385A also features reduced variation of the TCCD parameter which is important for dual pixel applications. (See AN-1084)

This device may also be used as a replacement for the DS90CF583 (5V, 65MHz) and DS90CF581 (5V, 40MHz) FPD-Link Transmitters with certain considerations/modifications:

1. Change 5V power supply to 3.3V. Provide this 3.3V supply to the V_{CC} , LVDS V_{CC} and PLL V_{CC} of the transmitter.
2. The DS90C385A transmitter input and control inputs accept 3.3V LVTTTL/LVCMOS levels. They are not 5V tolerant.
3. To implement a falling edge device for the DS90C385A, the R_FB pin may be tied to ground OR left unconnected (an internal pull-down resistor biases this pin low). Biasing this pin to V_{CC} implements a rising edge device.

TRANSMITTER INPUT PINS

The TxIN and control input pins are compatible with LVCMOS and LVTTTL levels. These pins are not 5V tolerant.

TRANSMITTER INPUT CLOCK/DATA SEQUENCING

Unlike the DS90C385, DS90C(F)383A/363A, the DS90C385A does not require any special requirement for sequencing of the input clock/data and PD (PowerDown) signal. The DS90C385A offers a more robust input sequencing feature where the input clock/data can be inserted after the release of the PD signal. In the case where the clock/data is stopped and reapplied, such as changing video mode within Graphics Controller, it is not necessary to cycle the PD signal. However, there are in certain cases where the PD may need to be asserted during these mode changes. In cases where the source (Graphics Source) may be supplying an unstable clock or spurious noisy clock output to the LVDS transmitter, the LVDS Transmitter may attempt to lock onto this unstable clock signal but is unable to do so due the instability or quality of the clock source. The PD signal in these cases should then be asserted once a stable clock is applied to the LVDS transmitter. Asserting the **PWR DOWN** pin will effectively place the device in reset and disable the PLL, enabling the LVDS Transmitter into a power saving standby mode. However, it is still generally a good practice to assert the PWR DOWN pin or reset the LVDS transmitter whenever the clock/data is stopped and reapplied but it is not mandatory for the DS90C385A.

SPREAD SPECTRUM CLOCK SUPPORT

The DS90C385A can support Spread Spectrum Clocking signal type inputs. The DS90C385A outputs will accurately track Spread Spectrum Clock/Data inputs with modulation frequencies of up to 100kHz (max.) with either center spread of $\pm 2.5\%$ or down spread -5% deviations.

POWER SOURCES SEQUENCE

In typical applications, it is recommended to have V_{CC} , LVDS V_{CC} and PLL V_{CC} from the same power source with three separate de-coupling bypass capacitor groups. There is no requirement on which VCC entering the device first.

Typical Application

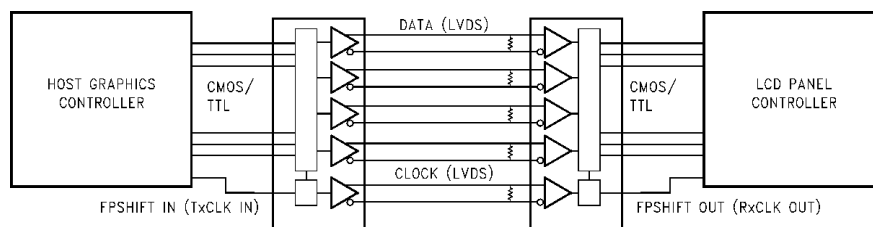


Figure 14. Typical Application

**Table 1. Truth Table – Programmable Transmitter
(DS90C385A)**

| Pin | Condition | Strobe Status |
|------|------------------------|---------------------|
| R_FB | R_FB = V _{CC} | Rising edge strobe |
| R_FB | R_FB = GND or NC | Falling edge strobe |

REVISION HISTORY

| Changes from Revision J (April 2013) to Revision K | Page |
|--|--------------------|
| • Changed layout of National Data Sheet to TI format | 11 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| DS90C385AMT/NOPB | ACTIVE | TSSOP | DGG | 56 | 34 | RoHS & Green | SN | Level-2-260C-1 YEAR | -10 to 70 | DS90C385AMT | Samples |
| DS90C385AMTX/NOPB | ACTIVE | TSSOP | DGG | 56 | 1000 | RoHS & Green | SN | Level-2-260C-1 YEAR | -10 to 70 | DS90C385AMT | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

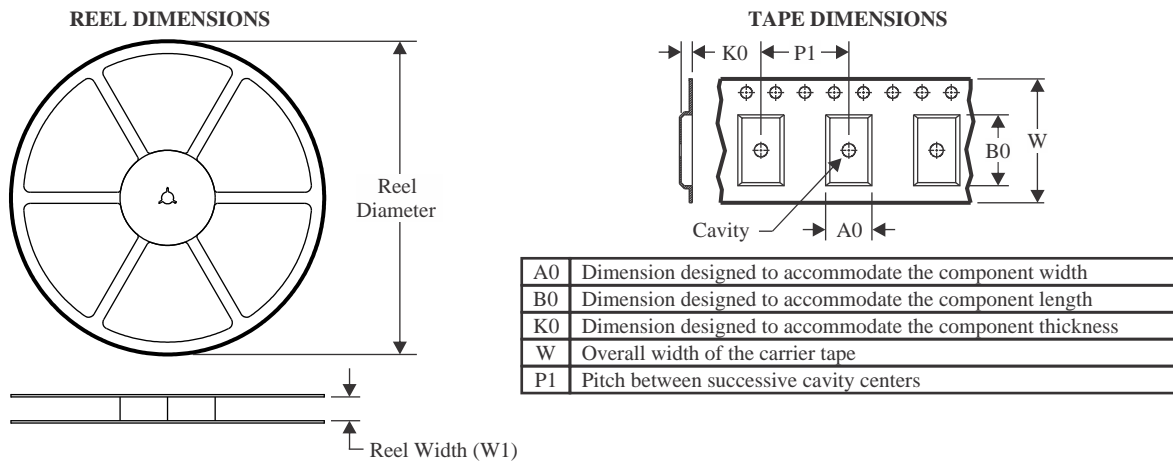
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

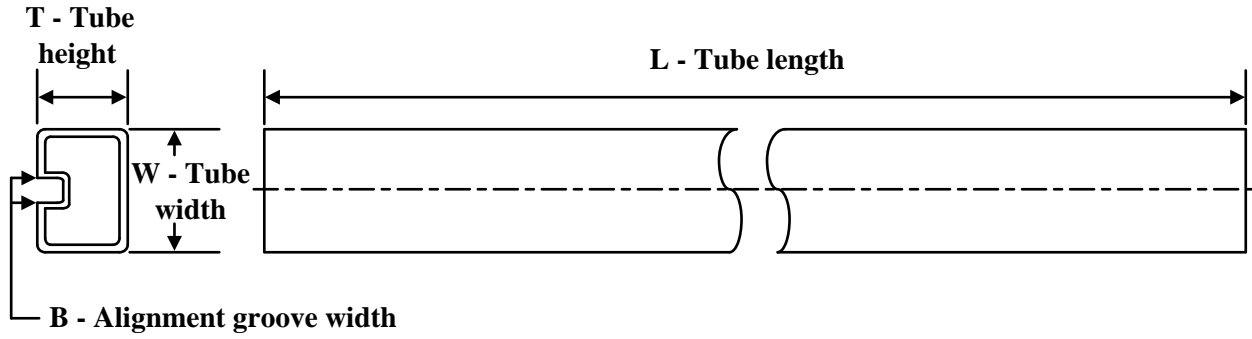

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS90C385AMTX/NOPB | TSSOP | DGG | 56 | 1000 | 330.0 | 24.4 | 8.6 | 14.5 | 1.8 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

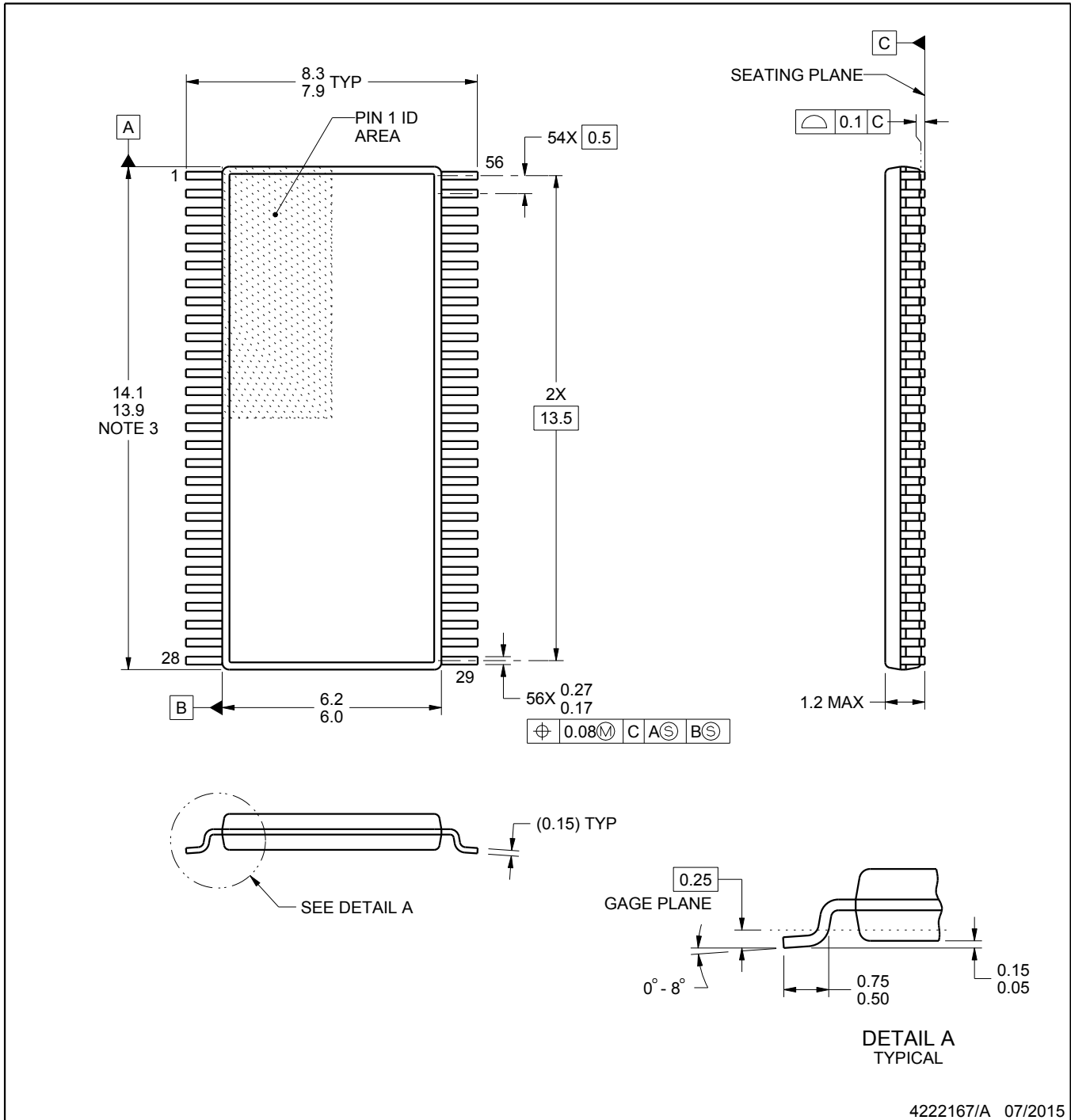

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS90C385AMTX/NOPB | TSSOP | DGG | 56 | 1000 | 367.0 | 367.0 | 45.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| DS90C385AMT/NOPB | DGG | TSSOP | 56 | 34 | 495 | 10 | 2540 | 5.79 |



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NOTES:

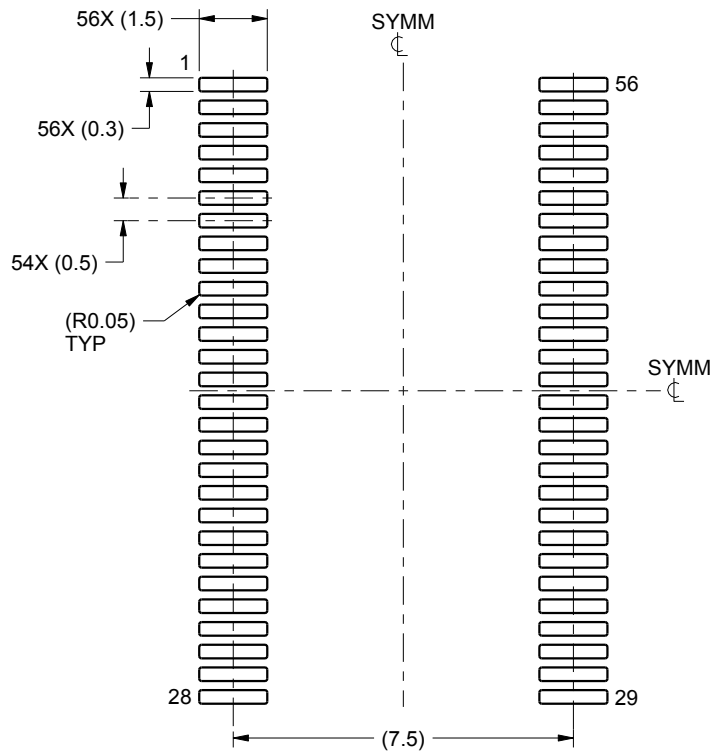
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

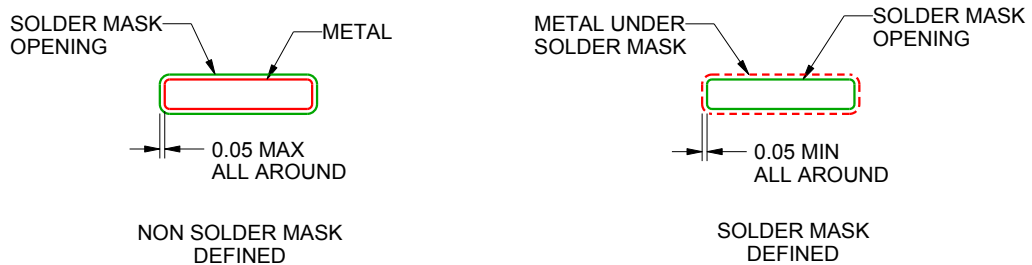
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

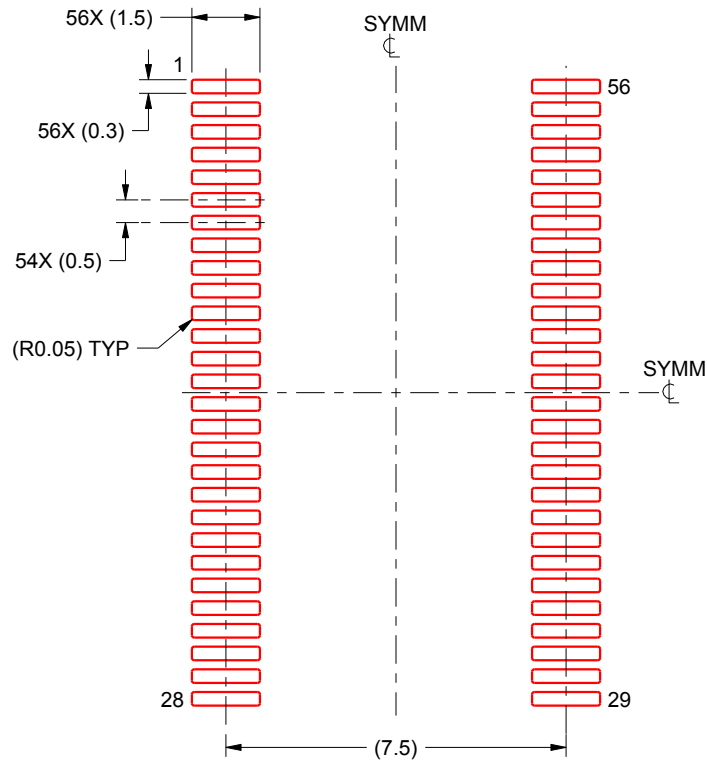
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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