ADS62PXXEVM

User's Guide

Literature Number: SLAU237A
May 2008–Revised April 2009

Contents

List of Figures

List of Tables

ADS62PXXEVM

1 Overview

This user's guide gives a general overview of the evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module. This manual is applicable to the ADS62P42/43/44/45/48/49, ADS62P22/23/24/25/28/29 and ADS62C15/17 analog to digital converters (ADC), which will be collectively referred to as ADS62PXX. This document should be used in combination with respective ADC data sheet. The ADS62PXX EVM provides a platform for evaluating the analog-to-digital converter (ADC) under various signal, clock, reference and power supply conditions.

1.1 ADS62PXX EVM Quick-Start Procedure

The ADS62PXXEVM provides numerous options for providing clock, input frequency and power to the ADC under evaluation. The quick start procedure describes how to quickly get initial results using the default configuration of the EVM as it was shipped. The EVM can be put back to default configuration by setting all jumpers to the default positions as described in Table 1. The default configuration of the EVM is for the Input Frequency (IF) and the clock input, each to be a single ended input that is transformer-coupled to the ADC. The default configuration for the power supply is to provide a single 5V supply to the red banana jack J10, PWR IN. The default configuration for the EVM is to control the modes of operation by jumper settings for parallel input control pins rather than serial SPI control of the register space. The other modes of operation of the EVM are described in the latter sections of this document. If users modify the default jumper settings, this procedure does not apply.

A quick-setup procedure for the default configuration of the ADS62PXX follows:

1. Verify all the jumper settings against the schematic jumper list in Table 1.
2. Connect the 5V supply between J10 (PWR IN) and J12(GND). If you are using the TSW1200 for capture, it also can be used to source 5V for the EVM. To use the 5V output power of the TSW1200, configure JP8 to short 1-2, J22 to short 1-2, and jumper over 5V from the banana jacks on the TSW1200 to J10 on the ADC EVM. Do not connect a voltage source greater than 5.5V.
3. Switch on power supplies.
4. Using a function generator with 50Ω output impedance, generate a 0V offset, 1.5V_{PP} sine-wave clock into J19. The frequency of the clock must be within the specification for the device speed grade.
5. Use a frequency generator with a 50Ω output impedance, generate a 0V offset, –1 dBFS-amplitude sine-wave signal into J6 (Channel A) or J3 (Channel B).This provides a transformer-coupled differential input signal to the ADC.
6. Connect the TSW1200 or suitable logic analyzer to J8 to capture the resulting digital data. If a TSW1200 is being used to capture data, follow the additional alphabetically labeled steps. For more details, see Connecting to FPGA Platforms, located in this document.
   a. After installing the TSW1200 software and connecting the TSW1200 to the USB port, open the TSW1200 software.
   b. Depending on the ADC under evaluation, select from the TI ADC Selection pull-down menu.
   c. Change the ADC Sample rate and ADC Input frequency to match those of the signal generator.
   d. After selecting a Single Tone FFT test, press the Capture Data button.

Table 1. Jumper List

Jumper	Function	Default Jumper Setting
Interface Circuit Operational Amplifier THS4509 (Bypassed)		
SJP1	AMP_OUT+	1-2
SJP2	AMP_OUT-	1-2
JP3	THS4509_PD	2-3
SJP5	AMPIN-	1-2
SJP3	AMPIN+	No Shunt
ADC Circuit		
JP11	Parallel	1-2
JP9	SDATA	1-2
JP10	SEN	1-2
JP12	MODE (Internal or External reference and Gain selection)	1-2
JP8	SCLK	1-2
JP5	CTRL3	1-2
JP6	CTRL2	1-2
JP7	CTRL1	1-2
JP13		No Shunt
JP14	DFS (Data Format and LVDS/CMOS output interface)	3-4
JP22	SDOUT/SPI-MISO Selection	No Shunt
Clock Interface Circuit		
J18	VCXO EN	No Shunt
SJP4	CLOCKIN	1-2
SJP7	CLOCKIN, Y0, Y1P SELECT	1-2
SJP6	YIN SELECT	1-2
SJP8	PLL LOCK	1-2
J15	RST (CDC Reset)	No Shunt
J14	CDC_PWRDWN	1-2
JP20	AUX SEL	1-2
JP21	MODE_SEL	1-2
Power Supply		
JP15	ADC VA	1-2
JP18	ADC VD	1-2
JP16	TPS79501 INPUT SELECT	1-2
JP19	5V_AUX	1-2
JP17	TPS5420 INPUT SELECT	No Shunt

2 Circuit Description

2.1 Schematic Diagram

The schematic diagram for the this EVM is attached at the end of this document. See the schematic or relevant section of this user's guide before changing any jumpers.

2.2 ADC Circuit Function

Selection of various modes of operation of the ADS62PXX EVM is most often controlled by jumpers on the EVM, either by placing shunts on 0.025-inch square jumper posts or by installation of surface mount 0Ω resistors. In general, the use of 0Ω resistors as jumpers are used in the clock or signal path where signal integrity is critical, and jumper posts are used for static or low-speed control paths. Figure 1 shows the relative location of the jumpers, connectors, and switches used on the ADS62PXX EVM. Figure 2 shows the relative locations of most of the resistors and surface-mount 0Ω jumper locations used on the EVM. In the description of the circuit options in the following sections, each operational mode is accompanied by a table entry that details the jumper or resistor changes that enable that option. Figure 1 and Figure 2 can assist the user to quickly identify where these jumpers are located on the EVM.

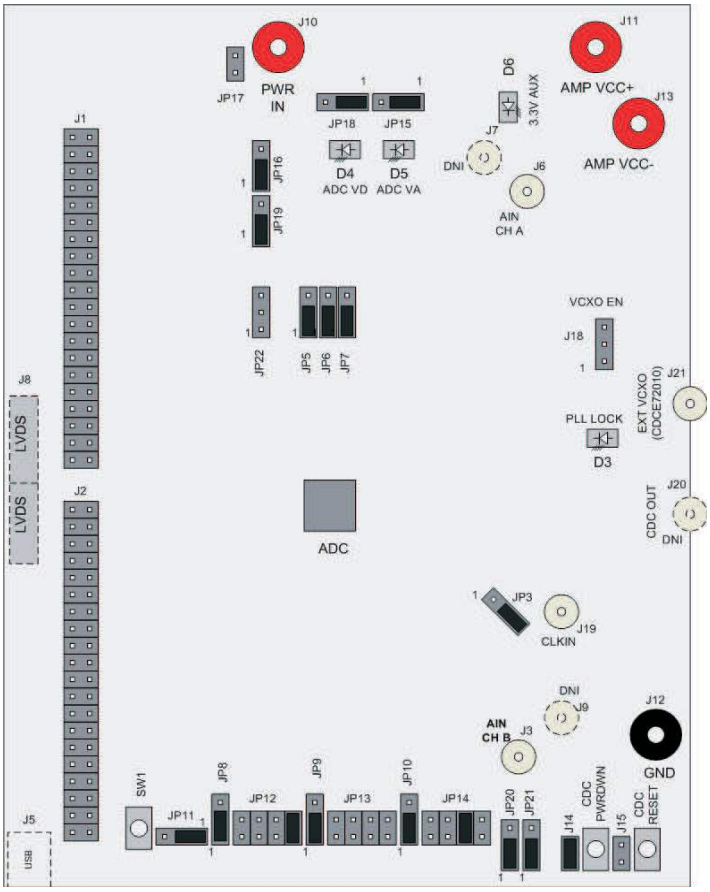

Figure 1. ADS62PXX Jumpers

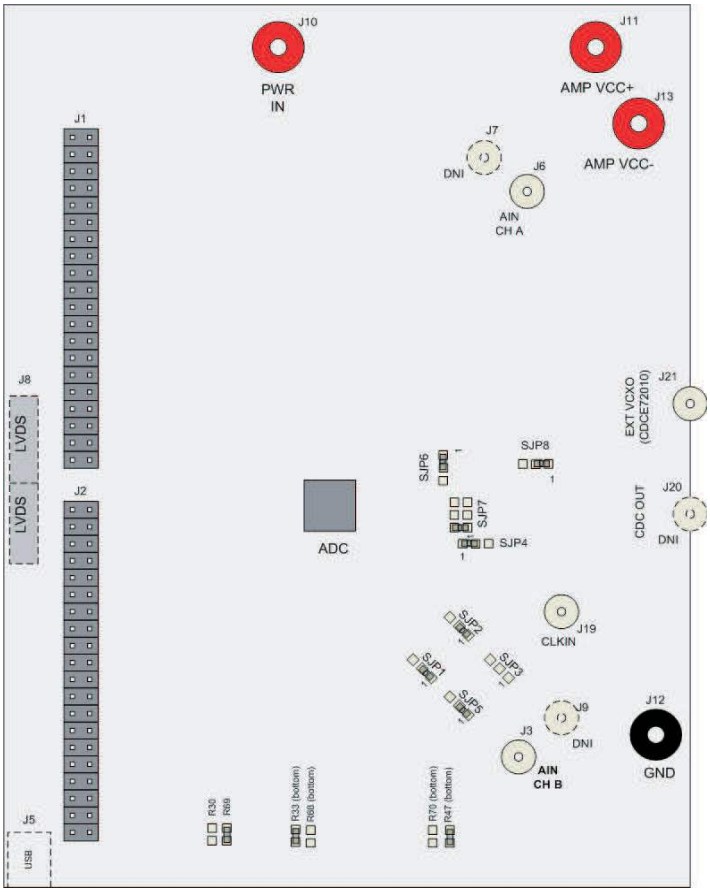

Figure 2. ADS62PXX Surface Jumpers

2.2.1 ADC Operational Mode

By default, the ADC is configured to operate in parallel-mode operation, since jumper (JP11) asserts a 3.3V state to the ADC reset pin. Consequently, the SW1 reset pushbutton must be pressed only when the device is configured in serial operation mode. Since the ADC is in parallel operation mode, voltages are used to set the ADC configuration modes. Users can use the information printed on the EVM silkscreen to set the operation modes.

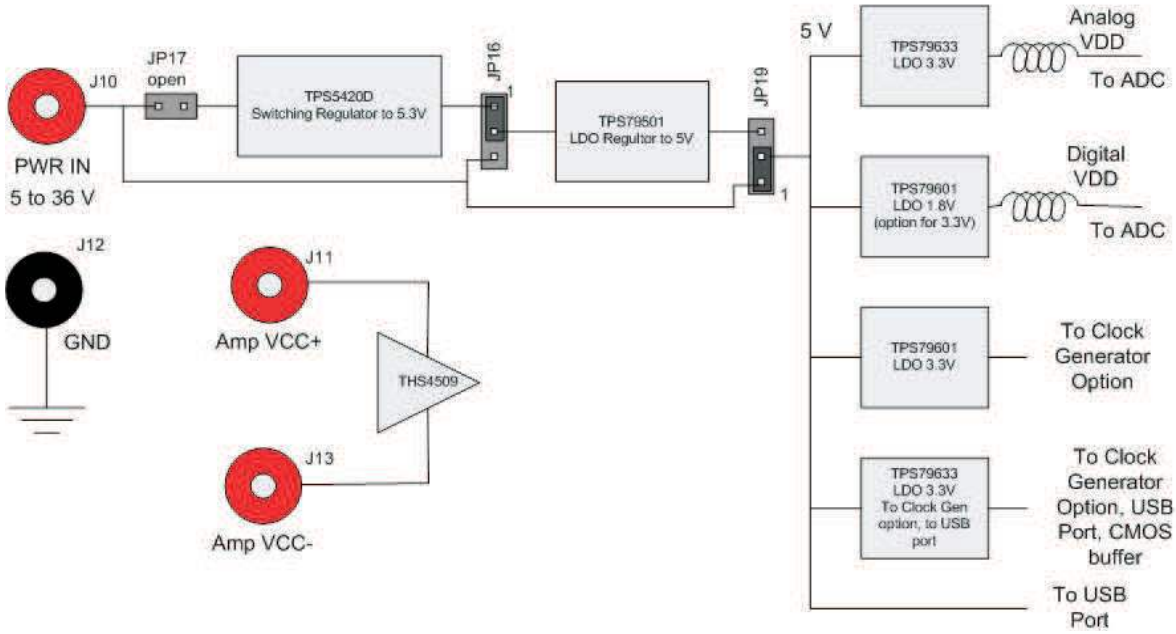

Figure 3. ADS62PXXEVM Power Distribution

2.2.2 EVM Power Connections

Power is supplied to the EVM through banana jacks. From this input power, several different ways of delivering power to the ADC and other EVM functions are available. Figure 3 shows a simplified representation of the power options available for the ADS62PXXEVM. The default option is to provide 5V to the red banana jack J10, and from there, the EVM generates 3.3V for the analog supply to the ADC and the necessary digital supply voltage for the populated ADC. The EVM also generates the proper voltages for optional features of the EVM such as the Clock Generation circuitry, the USB circuitry, and the CMOS output buffer.

Some ADC devices that may be evaluated on the ADS62PXXEVM platform do not take 1.8V for the digital supply, but rather require 3.3V for the digital supply. For this reason, an adjustable voltage regulator was chosen for the digital supply; the output may be changed to 3.3V by changing the value of a resistor, R269 and capacitor C148. The resistor and capacitor need not to be changed in the field unless the ADC is being changed, because the EVM ships with the correct digital supply voltage for the ADC that is installed. For reference, ADS62P42/43/44/45,ADS62P22/23/24/25 and ADS62C15 use 3.3V as digital supply for the ADC whereas ADS62P48/49,ADS62P28/29 and ADS62C17 use 1.8V as digital supply for the ADC.

Power for the optional THS4509 operational amplifier is supplied by banana jacks J11 and J13. If the amplifier is being evaluated in AC coupled configuration, 5V is supplied to J11, and J13 is connected to ground. In DC-coupled configuration, 4V is supplied to J11 and –1V is supplied to J13. Otherwise, these inputs may be left unconnected.

Although various power options are available on this EVM, care must be taken while applying power on J10 as different options have different voltage ranges specified. Table 2 displays the general jumper setting information; Table 3 displays the various power option settings. Prior to making any jumper settings, see the schematics located at the end of this document.

CAUTION

Voltage limits: Exceeding the maximum input voltages can damage EVM components. Undervoltage can cause improper operation of some or all of the EVM components.

Table 2. EVM Power Supply Jumper Description

EVM Banana Jack	Description	Jumper
J10	Input	Setting 6V to 36V power supply default-apply just 5V
JP16	TPS79501 INPUT SELECT	1-2 → Connects 5.3V to input of TPS79501 2-3 → TPS79501 Input connected to J10
JP19	5V_AUX	2-3 → TPS79501 output as 5V_AUX rails 1-2 → 5V_AUX rail connected to J10
JP17	TPS5420 INPUT SELECT	Shunt → J10 connected to TPS5420D

Table 3. EVM Power Supply Options

EVM Option	Evaluation Goal	Jumper Changes Required	Voltage on J10	Comments
1	Evaluate ADC performance using a cascaded switching power supply (TPS5420D) and LDO solution (TPS79501DCQ)	JP16 → 1-2 JP19 → 2-3 JP17 → 1-2 JP15 → 1-2 JP18 → 1-2	6V - 36V	Maximum performance and efficiency
2	Evaluate ADC performance using a LDO based solution	JP16 → 1-2 JP19 → 1-2 JP17→ No Shunt JP15 → 1-2 JP18 → 1-2	5.1V - 5.5V	Maximum Performance
3	Evaluate ADC performance using an isolated ADC AVDD and DVDD for current consumption measurements	JP16 → No Shunt; JP19 → No Shunt JP17 → No Shunt JP15 → Connect 3.3V to pin 2 of jumper JP18 → Connect 1.8V to pin 2 of jumper	Do not apply power on J10	Isolated power supply for current consumption measurements

2.2.2.1 Power Supply Option 1

Option 1 supplies the power to the ADC using cascaded topology of the TPS5420D switching power regulator and the TPS79501DCQ Low Drop-Out regulator. The TPS5420 is a step-down converter which works with the input voltage in the range 6V to 36V. The switching supply increases efficiency for higher input voltages but does create noise on the voltage supplies. To reduce the noise, an ultra-low-noise, high-PSSR LDO TPS79501DCQ is used to clean the power supply. The TPS5420D is designed for 5.3V output, which acts as a supply for the TPS79501. The TPS79501 is designed to output 5V, which is the AVDD for the ADC. This voltage rail is input to the LDO TPS79633, which outputs 3.3V, used for DVDD for the ADC. A separate TPS79633 is designed to output 3.3V for the CDCE72010 supply rail. This solution adds two features to the EVM: one is to increase the range of the power supply on jumper J10 from 6V to 36V, allowing the user to choose any power supply source in the specified range without causing significant power dissipation. The other feature is that the output-voltage rail has a much lower ripple, allowing better performance of the part even when the power source is fluctuating.

2.2.2.2 Power Supply Option 2

Option 2 supplies power to the ADC using the LDOs TPS79633DCQ and TPS79601DCQ. The LDOs take a maximum input of 5.5V. When using this option, take care powering up the EVM, because higher voltage or reverse polarity can damage it. This is the default power-supply configuration for the ADS62PXXEVM.

2.2.2.3 Power Supply Option 3

Option 3 is used to evaluate ADC performance using an isolated AVDD and DVDD power supply for current-consumption measurements. This option must be used with caution, because reversing the power supply or connecting to the wrong connector can damage the EVM. One common use of this option is to measure the separate current consumption of the relative supplies under particular operating conditions. For this option, the shunts on jumpers JP18 and JP15 are removed and the input power is supplied to the center post of the jumper. For convenience, a ground post is provided next to the center post for header connections that contain power and ground on 0.1" centers.

2.2.3 ADC Analog Inputs

The EVM can be configured to use either a transformer-coupled input or a TH4509 amplifier input, both from a single-ended source. The SMA connector J6 (for Channel A) and J3 (for Channel B) provide the single-ended analog input to the transformer-coupled input circuit to the ADC. The SMA connector J7 and J9 are not installed by default, but can be used to bring a differential input clock to the transformer-coupled input or to bring a single ended input to the THS4509 input circuit. To use the transformer for one of these options, the EVM must be configured for one of the options listed in Table 5. See the schematic located at the end of this document prior to making any jumper changes.

Table 4. Analog Input Jumper description

EVM Banana Jack	Description	Jumper Setting
J6	Analog Input single-ended	
J3	Analog Input single-ended	
J7	Analog input, can be used with J6 for differential input	Not populated
J9	Analog input, can be used with J3 for differential input	Not populated
SJP1	AMPOUT+, +ve terminal of T4	2-3 → AMPOUT+ is selected as source of input to ADC 1-2 → Use analog input from J3 as signal source to ADC (use with appropriate SJP5 setting)
SJP2	AMPOUT-, -ve terminal of T4	2-3 → AMPOUT- is selected as source of input to ADCC 1-2 → Use analog input from J9 as signal source to AD (use with appropriate SJP3 setting
SJP5	INPUT -ve select	1-2 → J3 supplies the analog signal to ADC 2-3 → -ve input to amplifier
SJP3	INPUT +ve select	1-2 → J9 supplies the analog signal to ADC 2-3 → +ve input to amplifier DEFAULT is no shunt
SP3	Power down for amplifier THS4509	1-2 → Pulls up the pin (Normal operation or amplifier is ON) 2-3 → Grounds the pin (Low-power mode or amplifier is off)

Table 5. EVM Analog Input Options

EVM Option	Evaluation Goal	Jumper Changes Required	Voltage on J11 and J13	Analog signal to ADC	Comments
1	Evaluate ADC performance using direct input to ADC	SJP1→ 1-2 SJP2 → 1-2 SJP3 → No shunt SJP5 → 1-2 JP3 → 2-3	Do not connect	From J6 (Channel A) or J3 (Channel B)	Default
2	Evaluate ADC performance using input through THS4509	SJP1→ 2-3 SJP2 → 2-3 SJP3 → 2-3 SJP5 → 2-3 JP3 → 1-2 Install J9 Remove R63 Install R62	J11 → 5V J13 → GND	Signal from J3 and J9 is amplified by THS4509	Used if input signal requires amplification

2.2.3.1 Analog Input Option 1

Option 1 supplies the transformer-coupled input from J6 or J3 to the ADC. This configuration is the default on the EVM. The test result using this option is shown in Figure 10. A double-transformer input circuit is used to provide better differential to single-ended conversion than a single transformer can provide. The transformers used are both of a 1:1 turns ratio, so termination of the 50Ω input signal path after the transformers can be two 25Ω resistors terminated to the Common Mode Voltage (VCM) provided by the ADC.

Following the transformer coupling, surface mount pads are provided for several input circuits. By default, the input circuit is configured as shown in the ADS62PXX data sheet under the recommended input circuit for high-bandwidth (>100 MHz IF) inputs. However, the recommended low-bandwidth input circuit for the ADS62PXX can be implemented on the surface mount pads provided.

2.2.3.2 Analog Input Option 2

Option 2 allows the use of an amplifier to provide input to the ADC. TI has a range of wideband operational amplifiers such as THS4508/09/11/13/20. On this EVM, THS4509 is used as an example to amplify the input from J3 or J9. The THS4509 is powered up by applying 5 V to J11 and GND to J13 (for AC coupled configuration). A differential power supply (4V applied to J11 and -1V applied to J13) may also be used to power up the amplifier if common-mode biasing is an issue for DC-coupled applications. See the THS4509 data sheet (SLOS547). The output of the THS4509 is filtered through a band-pass filter before ADC input. The band-pass filter can be designed depending on the end application. By default, the band-pass filter components are not populated because the filter design depends on the end application. The TI schematic provides an example of a filter that is designed for the frequency band of 10 MHz to 58 MHz. When using the suggested filter, be sure to consider the proper value for R5, R6, R11 and R12 resistors, because the ADC may impose limits on how large these resistors may be while the amplifier may impose limits on how low an impedance it can drive. A key point when designing a filter is to design it for proper load termination. Care must be taken when supplying the input to the board; the source impedance must be 50 Ω. Results can vary due to mismatching of the various source and termination impedances.

2.2.4 ADC Clock Input

The clock can be supplied to the ADC in one of several ways. The default clocking option is to supply a single ended clock directly to the SMA connecter J19 directly, and this clock is converted to differential and AC coupled to the ADC by transformer coupling. The clock input must be from a clean, low-jitter source and is commonly filtered by a narrow bandpass filter. The clock amplitude is commonly set to about 1.5V peak to peak, and the amplitude offset is not an issue due to the AC coupling of the clock input. The clock source is commonly synchronized with the input frequency signal generator to keep the clock and IF coherent for meaningful FFT analysis.

Alternatively, the clock may be supplied by an onboard VCXO and CDCE72010 clock buffer. The CDCE72010 Clock Buffer has been factory programmed to output a clock to the ADC that is 1/4 the rate of the on-board VCXO. While using this clock option, a separate 20MHz reference clock must be supplied to the CDCE72010 by way of the Clock Input SMA connector J19 (Surface jumper SJP4 should be shorted to position 2-3 for this case). From the CDCE7201 two clocking options to the ADC are possible. A differential LVPECL clock output may be connected to the ADC clock input or a single-ended CMOS clock from the CDCE72010 may be routed to the ADC transformer-coupled clock input through an on-board crystal filter. For better performance, selecting the CMOS clock through a crystal output is recommended. Prior to making any jumper settings, see the schematic located at the end of this document. Table 6 displays the various clock option settings. The VCXO and crystal filter do not come populated on the EVM by default, although the CDCE72010 Clock buffer is installed.

Table 6. Clock Input Jumper Description

EVM Banana Jack	Description	Jumper Setting
J18	ENABLE VCXO TCO-2111	1-2 → VCXO enabled 2-3 → VCXO disabled Default is no shunt
J19	Clock Input	
J14	CDCE72010 power down	1-2 → CDCE72010 is power down Open → CDCE72010 is on
J15	CDCE72010 Reset	1-2 → Reset Open → Normal operation (Default)
SJP4	Clock In or CDC reference Jumper	1-2 → J19 supplies clock directly to ADC 2-3 → Reference clock for CDCE72010
SJP7	Clock input +ve terminal of T6 for ADC clock	1-2 → Connects J19 to ADC 3-4 → Connects Yo output of CDCE72010 (This path has crystal filter) to ADC 5-6 → Connects Y1P (Differential LVPECL clock output of CDCE72010)
SJP6	Clock input +ve terminal of T4 for ADC clock	1-2 → Connects to ground (default) 2-3 → Connects to Y1N (Differential clock output of CDCE72010) only to be used with Y1P
JP21	Mode select pin for CDCE72010	1-2 → High (Default), see data sheet of CDCE72010 (SCAS858) 2-3 → Ground
SJP8	PLLLOCK LED	1-2 → Connects to D3 diode 2-3 → Ground through 10nF capacitor
JP20	AUX_SEL pin for CDCE72010	1-2 → High, see data sheet of CDCE72010 2-3 → Ground (Default)

Table 7. EVM Clock Input Options

EVM Option	Evaluation Goal	Jumper Changes Required	Frequency Input on J19	CDC Configuration Description	Comments
1	Evaluate ADC performance using a sinusoid clock	J18 → 2-3 SJP4 → 1-2 SJP7 → 1-2 SJP6 → 1-2 J14 → 1-2 J15 → No shunt	ADC's Sampling Frequency	NA	Default
2	Evaluate ADC performance using a crystal filtered LVCMOS clock derived from CDCE72010	J18 → 1-2 SJP4 → 2-3 SJP7 → 3-4 SJP6 → 1-2 J14 → No Shunt J15 → No Shunt	20M for VCXO at 983.04 MHz	Divide VCXO frequency by 4, output on Y0	Maximum performance
3	Evaluate ADC performance using a differential LVCEPL clock	J18 → 1-2 SJP4 → 2-3 SJP7 → 5-6 SJP6 → 2-3 J14 → No Shunt J15 → No Shunt	20M for VCXO at 983.04 MHz	Divide VCXO frequency by 4, differential LVPECL Clock output on Y1P and Y1N	Not recommended for most applications

2.2.4.1 Clock Option 1

The Clock Option 1 provides a clock to ADC directly from an external source. For the direct supply of the clock to the ADC, a single-ended square or sinusoidal clock input must be applied to J19. The clock frequency must be within the maximum frequency specified for the ADC. The clock input is converted to a differential signal by a Mini-Circuits™ ADT4-1WT, which has an impedance ratio of 4, implying that voltage applied on J19 is stepped up by a factor of 2. ADC performance in this case depends on the clock source quality. This option is also the default configuration on the EVM, when it is shipped from the factory. The test result using this option is shown in Figure 10.

2.2.4.2 Clock Option 2

Option 2 uses the onboard VCXO and CDCE72010 to provide a clock to the ADC. The CDCE72010 is used in SPI mode which uses the internal EEPROM to configure the CDCE72010. The EEPROM is programmed in the factory for a divide-by-4 configuration. The EEPROM configuration is shown in Figure 4. The clock at J19 is the reference clock for CDCE72010. The VCXO frequency can be calculated as Fvcxo = Fout x 4 (Fout is the frequency output U0 and U1). The reference clock for CDCE72010 is calculated from Ref Clock = (Fvcxo x 125)/(48 x 128). This is the clock-to-M divider. When VCXO of frequency 983.04 MHz is used, the calculation results in a reference clock of 20 MHz; the clock output on Y0 pin of CDCE72010 is 245.76 MHz. This clock is filtered using the crystal filter with center frequency of 245.76 MHz. By default, the VCXO and the crystal filter are not populated on the EVM, so that the user can populate the components depending on the end application and sampling rate. This configuration is recommended for applications requiring an onboard clock generation scheme. The test result using this option is shown in Figure 11.

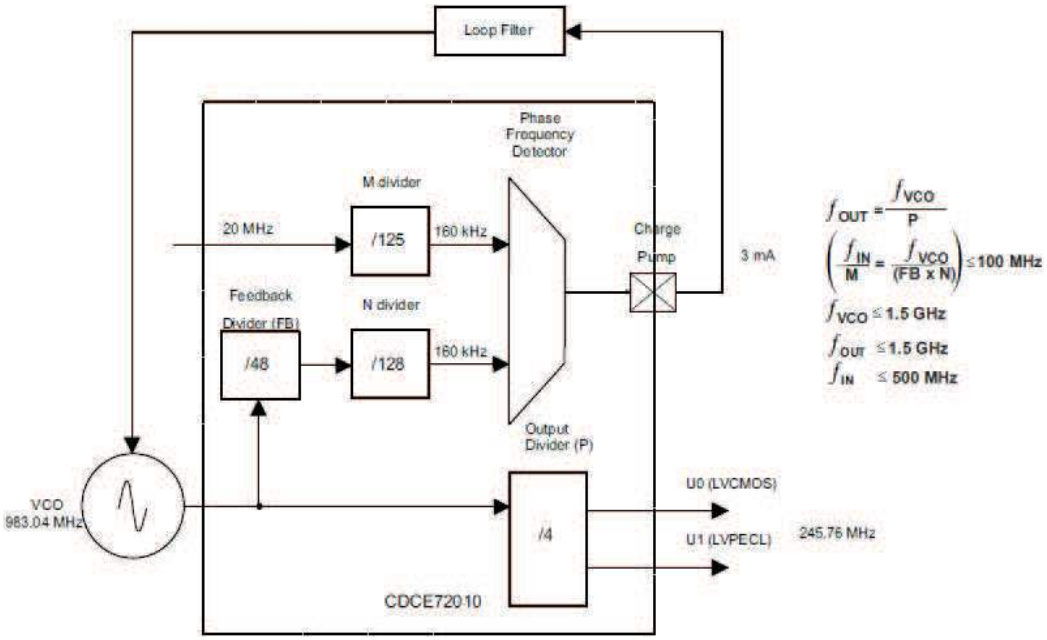

Figure 4. CDCE72010 EEPROM Configuration Block Diagram

2.2.4.3 Clock Option 3

Option 3 is used for a differential LVPECL clock. This configuration eliminates the need for a crystal filter. It uses the same EEPROM configuration as Option 2, but in this case, the ADC clock pins are connected to Y1N and Y1P. The jumper setting uses the clock output Y1P and Y1N from CDCE72010, to clock ADC. This configuration is not recommended for SNR critical applications. Notice that the clock frequency does not change. The frequency remains the same as in Clock Option 2. The test result using this option is shown in Figure 12.

2.2.5 ADC Digital Outputs

The LVDS digital outputs can be accessed through the J8 output connector. A parallel 100-Ω termination resistor must be placed at the receiver to properly terminate each LVDS data pair. These resistors are required if the user wants to analyze the signals on an oscilloscope or a logic analyzer. The ADC performance also can be quickly evaluated using the TSW1200 boards as explained in the next section. The TSW1200 will automatically terminate the LVDS outputs once the TSW1200 is connected to J8.

The ADS62PXX and most other ADCs that may be evaluated on this EVM also have an option to output the digitized parallel data in the form of single-ended CMOS. If single-ended CMOS is desired, header post connectors J1 and J2 are provided for the CMOS output. In order to use the header J1, a CMOS buffer U12 must be installed in place of a bank of 0-ohm resistors that by default steer the outputs to the LVDS connector J8. And in order to use the header J2, a CMOS buffer U13 must be installed in place of a bank of 0-ohm resistors that by default steer the outputs to the LVDS connector J8.

2.2.6 LEDs on the EVM

There are four LEDs on the EVM. LED D4 is named as ADC VD; this LED illuminates when the 3.3V digital supply is available to the ADC by setting jumper JP18 to position 1-2. Similarly, LED D5 (ADC VA) illuminates when the 3.3V analog supply is available to the ADC by setting jumper JP15 to position 1-2. LED D6 is 3.3V AUX, which illuminates when the 33V auxiliary supply is available from TPS79633. LED D3 is the PLL LOCK LED. This LED illuminates when the CDC72010 PLL is locked.

3 TI ADC SPI Control Interface

This section describes the software features of the EVM kit. The TI ADC SPI control software provides full control of the SPI interface, allowing users to write to any of the ADC registers found in the data sheet. For most ADS62PXX performance evaluations, users do not need to use the TI SPI control software. Users only need to use the ADC SPI control software when the desired feature is inaccessible through the ADC parallel interface mode.

3.1 Installing the ADC SPI Control Software

The ADC SPI control software can be installed on a personal computer by running the setup.exe file located on the CD. This file installs the graphical user interface (GUI) along with the USB drivers needed to communicate to the USB port that resides on the EVM. When prompted, users should allow the Windows® operating system to search for device drivers by checking "Yes, this time only", as seen in Figure 5. It will find the TI ADC SPI interface drivers automatically. After the software is installed, insert the USB cable to the EVM to finish the installation . The "Found New Hardware" wizard will start, and you must acknowledge that the TI ADC SPI Interface has not passed the Windows® Logo testing as shown in Figure 6. After completion, the TI ADC SPI Interface should show up in the Hardware Device Manager. Figure 7 shows the SPI interface in the Hardware Manager which indicates that it is ready for use.

Note: Before plugging in the USB cable for the first time, install the TI ADC SPI software. The software installs the drivers necessary for USB communication.

Figure 5. Found New Hardware

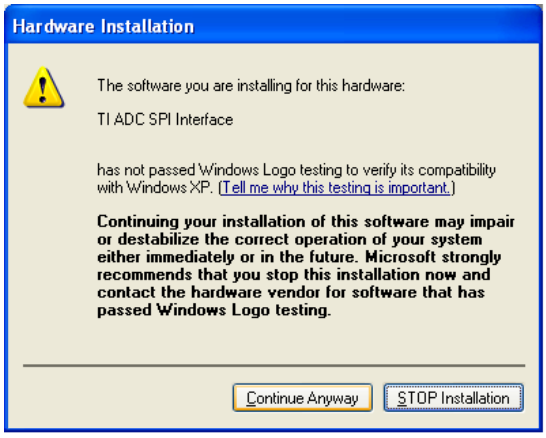

Figure 6. Window Logo Testing

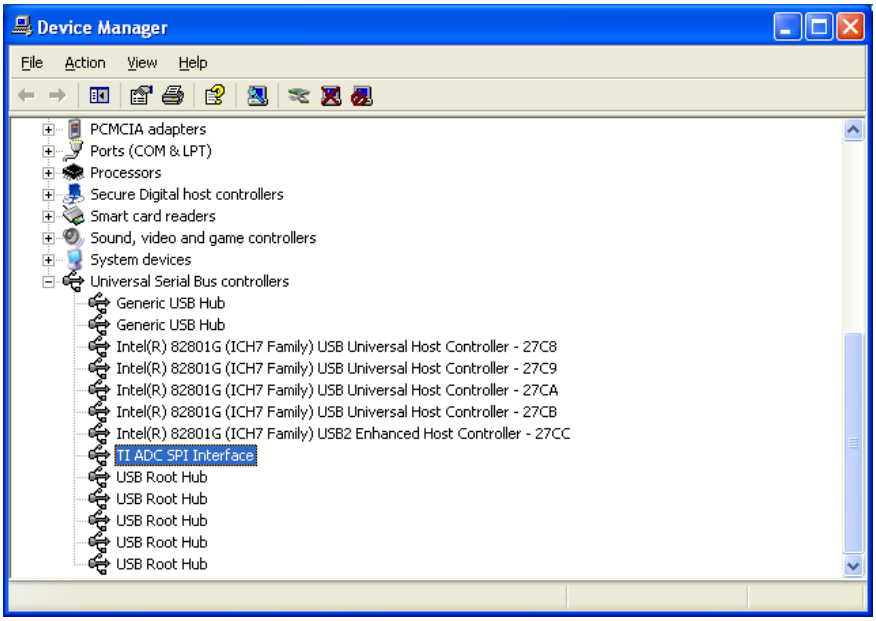

Figure 7. Hardware Device Manager

3.2 Setting Up the EVM for ADC SPI Control

Users who wish to use the ADC SPI interface must supply 5 VDC to P5, which provides power to the USB circuit. By default, the EVM comes with the ADC configured in parallel mode. In order to use the SPI interface to control the ADC modes of operation, users must move several jumpers.

- Move jumper JP11 to short positions 2–3, which places the ADC into serial operation mode.
- Move jumper JP8 to short positions 2–3, which allows the USB circuit to control SCLK.
- Move jumper JP9 to short positions 2–3, which allows the USB circuit to control SDATA.
- Move jumper JP10 to short positions 2–3, which allows the USB circuit to control SEN.

3.3 Using the TI ADC SPI Interface Software

Once the software is installed and the USB cable is connected, three primary modes of operating the software are available: SPI Register Writes, SPI Register Write Using a Script File, and ADS62PXX Frequently Used Registers.

Note: Before beginning an ADC evaluation, users are required to reset the ADC. This can easily be done by pressing the ADS62PXX Reset button found on the ADS62PXX tab. For most ADS62PXX evaluations that make use of the SPI interface, users should also assert the Override Bit also found on the ADS62PXX tab. This will force the ADC to be configured by the SPI interface only and it will ignore any board-level settings that may have been set. Please consult the datasheet for a full list of available functions in SPI interface mode.

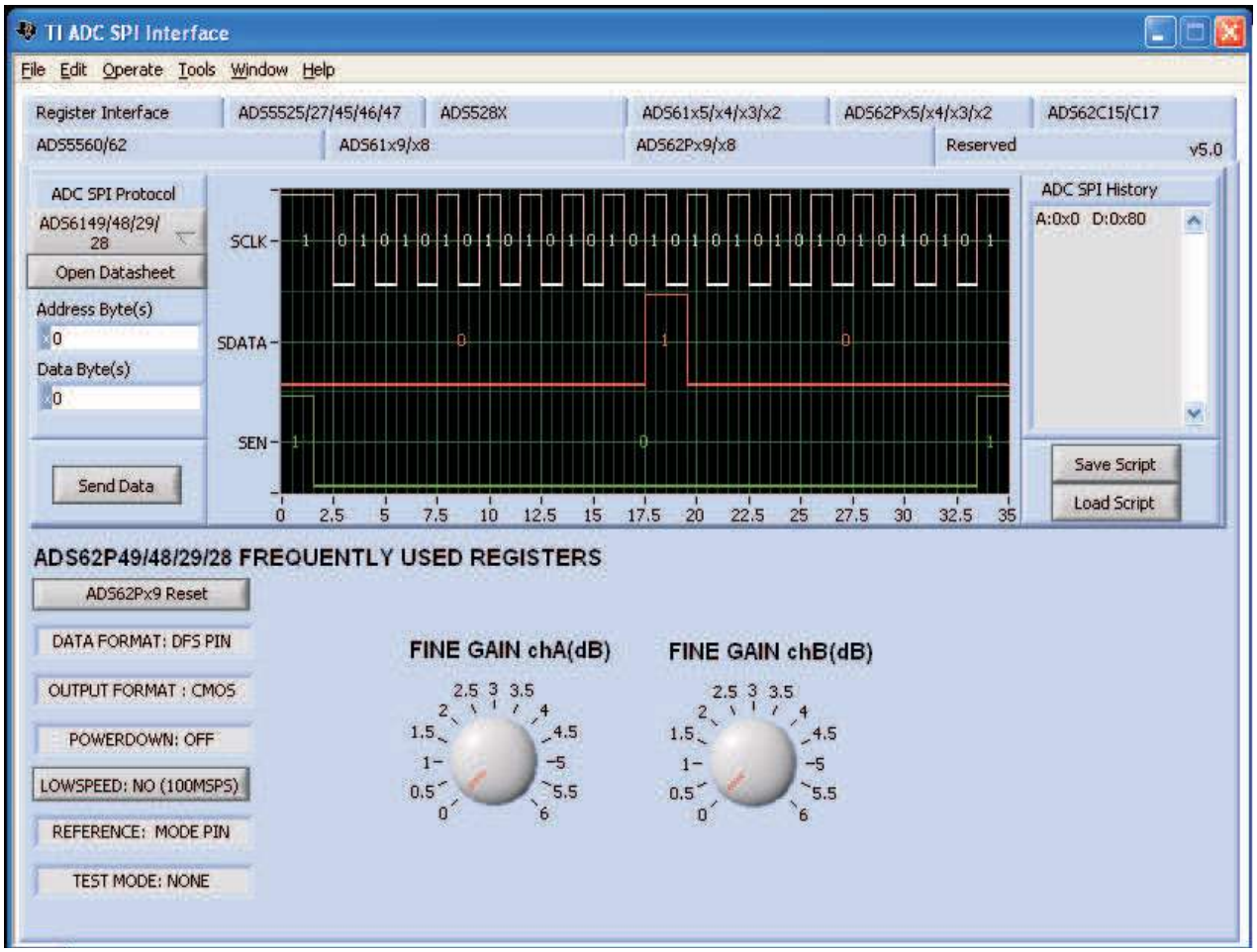

Figure 8. SPI Interface Screen

3.3.1 SPI Register Writes

The most basic mode of operation allows full control of writing to individual register addresses. From the tabs at the top of the interface screen (Figure 8), select the ADS62PXX ADC. Next, type the Address Bytes(s) in hexadecimal (hex) and Data Byte(s) in hex, which can be found in the device data sheet. When you are ready to send this command to the ADC, either press "Enter" on your keyboard or press the Send Data button. The graph indicator is updated with the patterns sent to the ADC. The default inputs to both the Address Byte(s) and Data Byte(s) fields are hex inputs as designated by the small *x* in the control. Users can change the default input style by clicking on the "x" to binary, decimal, octal, or hex. Multiple register writes can be written simply by changing the contents of the Address Byte(s) and Data Byte(s) field and pressing "Enter" or Send Data again. The ADC SPI History window will keep track of the register writes performed in a session.

3.3.2 SPI Register Write Using a Script File

After the ADC is configured to the desired usage, users can save time in future ADC configurations by saving a script file. By pressing the Save Script button, it dumps ADC SPI History window contents into a text file. Alternatively, users can edit the script file in a text editor. An example script file is located in the \\Install Directory\Script Files\ADS62PXX_LVDS_oBinary.txt which configures the ADC for use with the TSW1200. When ready to write the contents of the script file to the ADC, users can press the Load Script button and they will be prompted for the file location of their script file. The commands are sent to the ADC when the user acknowledges the selection of the file, however the graph indicator does not show multiple writes. The ADC SPI History will update to show the register writes executed in the script file.

3.3.2.1 ADS62PXX Frequently Used Registers

For ease of use, several buttons have been added that allow one-click register writes of commonly used features found in Table 8. These are found in the ADS62PXX tab (note that there is one tab for ADS62PX5/X4/X3/X2,one tab for ADS62Px9/X8 and one tab for ADS62C15/17, because these commands are specific to the ADS62PXX ADC only. The software writes to the ADC both the contents of the associated address and data when the button is clicked. When the ADS62PXX Reset button is pressed, it issues a software reset to the ADC, and it resets the button values to match the contents inside of the ADC. The graph indicator plots the SPI commands written to the ADC when a button has been pressed.

Table 8. ADS62PXX Frequently Used Registers

Default Value	Alternate Value
ADS62PXX Reset	
Over-ride bit: Off	Over-ride bit: On
2s Complement	Straight Binary
CMOS	DDR LVDS
Powerdown: OFF	Multiple Powerdown Options
No Course Gain	3.5-dB Course Gain
INT Reference	EXT Reference
Bit-Wise (LVDS Only)	Byte-Wise
Test Mode: None	Multiple Options
Fine Gain	Multiple Options

4 Connecting to FPGA Platforms

The ADS62PXX EVM provides several connection options to use the EVM with various FPGA development platforms and FPGA-based capture boards. The ADC features two output options, a DDR LVDS which interfaces with a TSW1200 capture card, and a CMOS output which interfaces with a TSW1100 capture card.

4.1 TSW1200 Capture Board

The TSW1200 board can be used to analyze the performance of the EVM. The TSW1200EVM is a circuit board that assists designers in prototyping and evaluating the performance of high-speed ADCs that feature parallel or serialized LVDS outputs. The TSW1200 has the LVDS 100Ω termination resistor on the input interface for ADC outputs. To start the TSW1200 software, note the following points. Users should consult the TSW1200 documentation for configuration details.

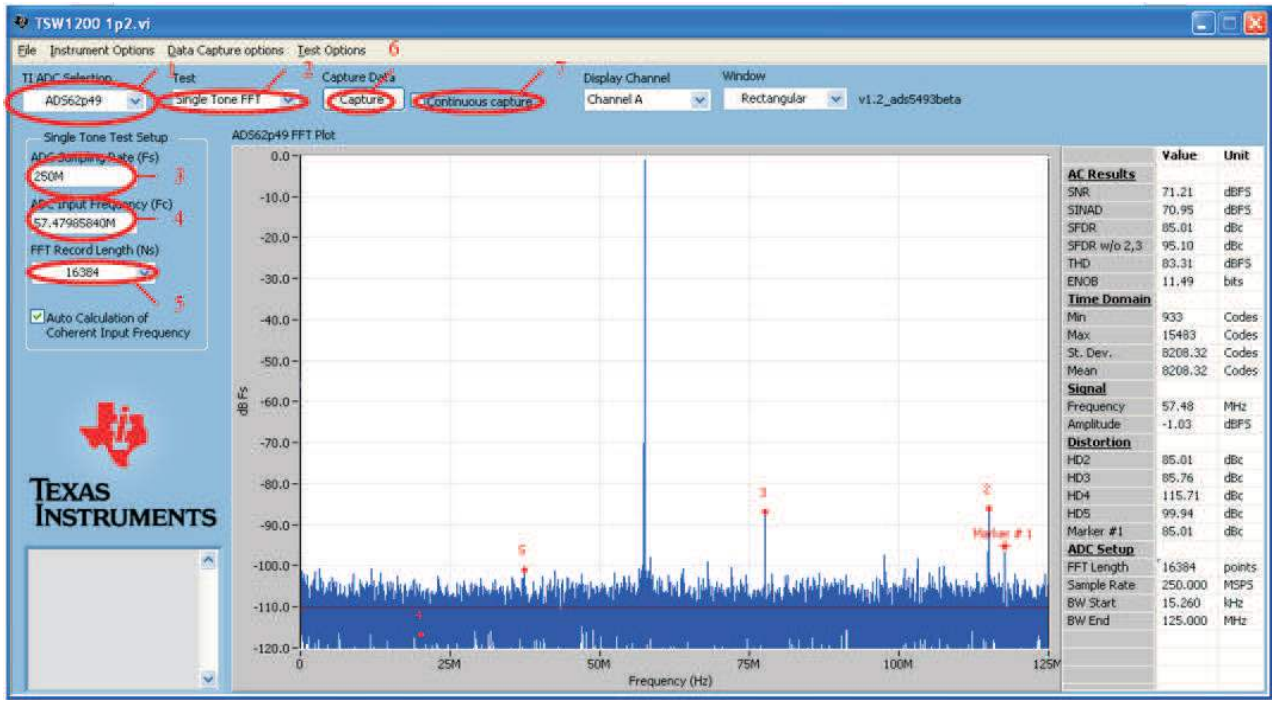

Figure 9. TSW1200 GUI Introduction

1. Select the ADC type to be used before capturing.
2. For test, select Single Tone FFT plot.
3. For the ADC Sampling Rate, type in the value.
4. Type in the ADC Input Frequency. Auto calculation of the input frequency depends on the FFT record length. As soon as the number is entered, the software calculates the coherent input frequency corresponding to that FFT length. This frequency signal must be supplied through the signal generator.
5. Select the FFT Record Length.
6. Select Capture to obtain the plot
7. The Continuous Capture option is used if the user wants to continuously capture the FFT.

Adjust the input level signal to attain a dBFS value of approximately –1.

4.1.1 Quick-Test Results

The user can make the jumper setting as mentioned in Table 1. In this configuration, the EVM uses an external clock source from J19 and a direct input signal J6 (Channel A) or J3 (Channel B) to the ADC. This setup uses Power Option 2 (Table 3), Analog Input Option 1 (Table 5), and Clock Option 1 (Table 7), which is the default on the EVM. Figure 10 shows the ADC performance capture using TSW1200 with the input signal of a 57.6-MHz frequency and clock frequency of 250 MHz with ADS62PXX.

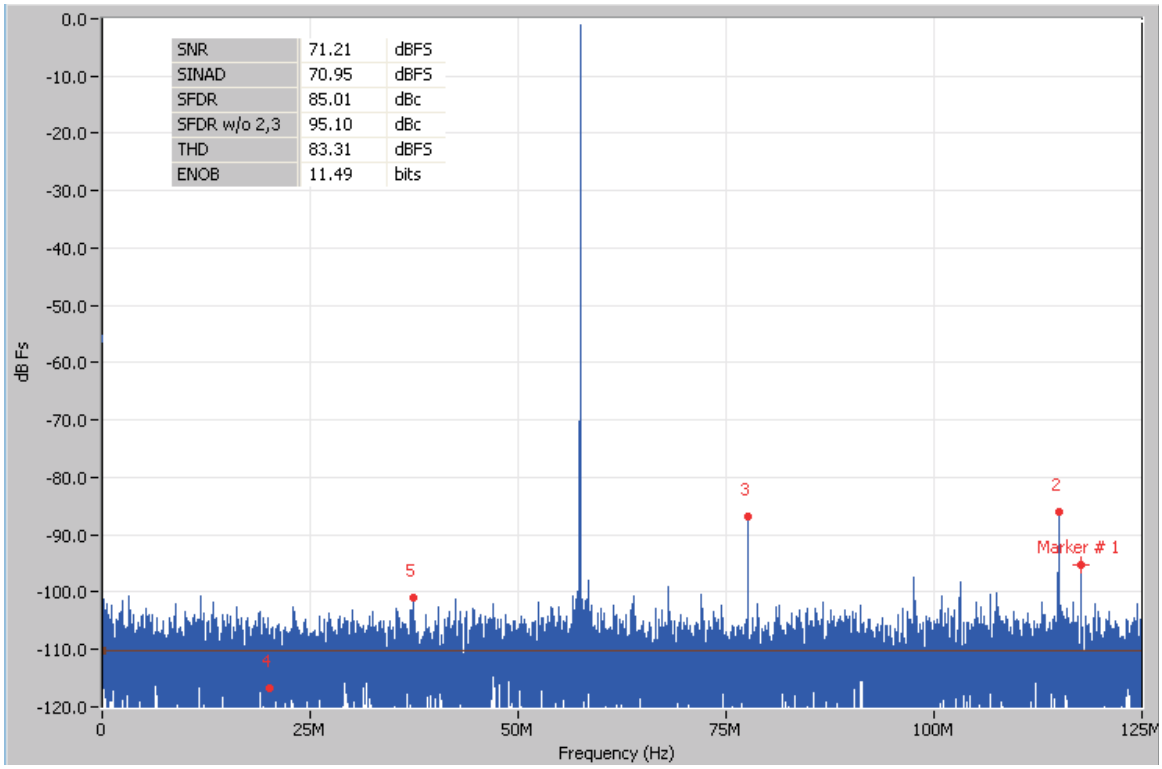

Figure 10. Quick-Setup Test Result

4.1.2 Test Result With Onboard VCXO and Clock Through Crystal Filter

This test uses the VCXO of frequency 983.04 MHz. This setup uses the Power Option 2 (Table 3), Analog Input Option 1 (Table 5), and Clock Option 2 (Table 7). For this test, the CDCE72010 crystal filter path was chosen to provide the clock to the ADC. The CDCE72010 provides a single-ended clock through output Y0 (Table 7), which is passed through a crystal filter of center frequency 245.76 MHz. This was the example setup; the VCXO and the crystal filter are not populated on the EVM because the values depend on the end application sampling rate. The capture result for ADS62PXX is as shown in Figure 11.

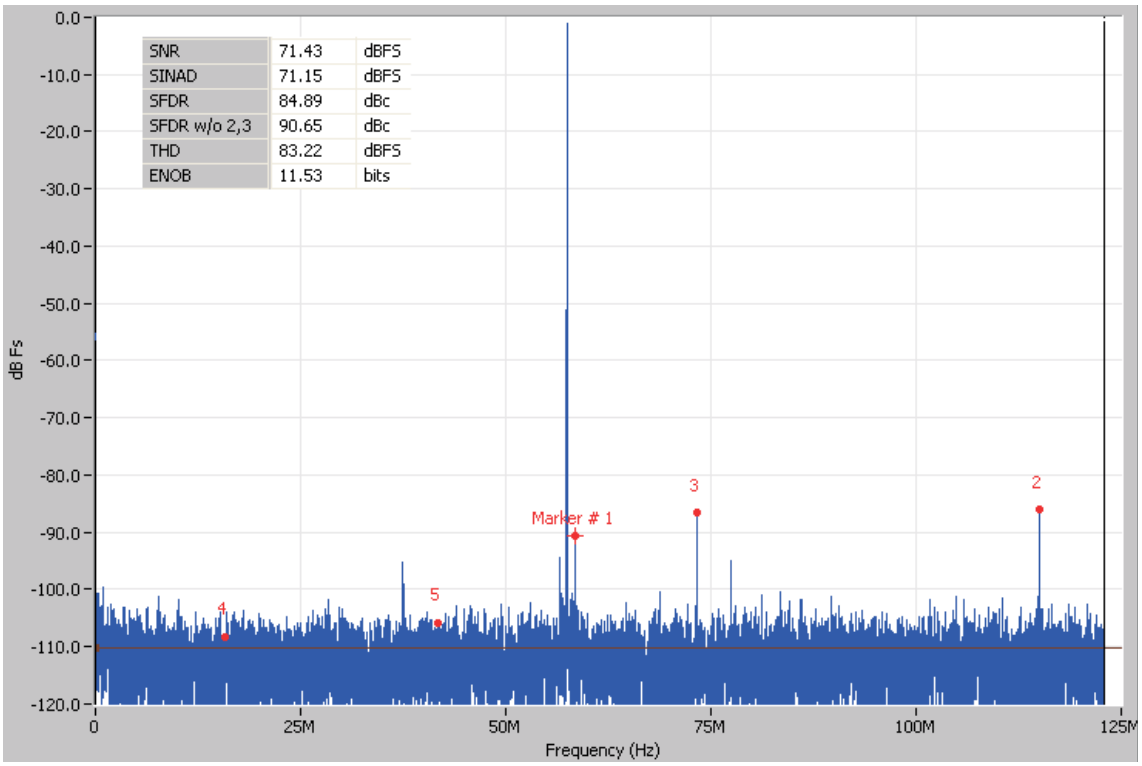

Figure 11. ADC Performance With Clock Through Onboard VCXO, CDCE72010 and Crystal Filter

4.1.3 Test Result With Onboard VCXO and Differential LVPECL Clock

For the same setup as explained in the previous section, when Clock Option 3 (Table 7) was used, the FFT was captured as shown in Figure 12. The test results with Clock Option 2 are better than with Clock Option 3. That is why Option 2 (clock with crystal filter) is recommended over the differential LVPECL output.

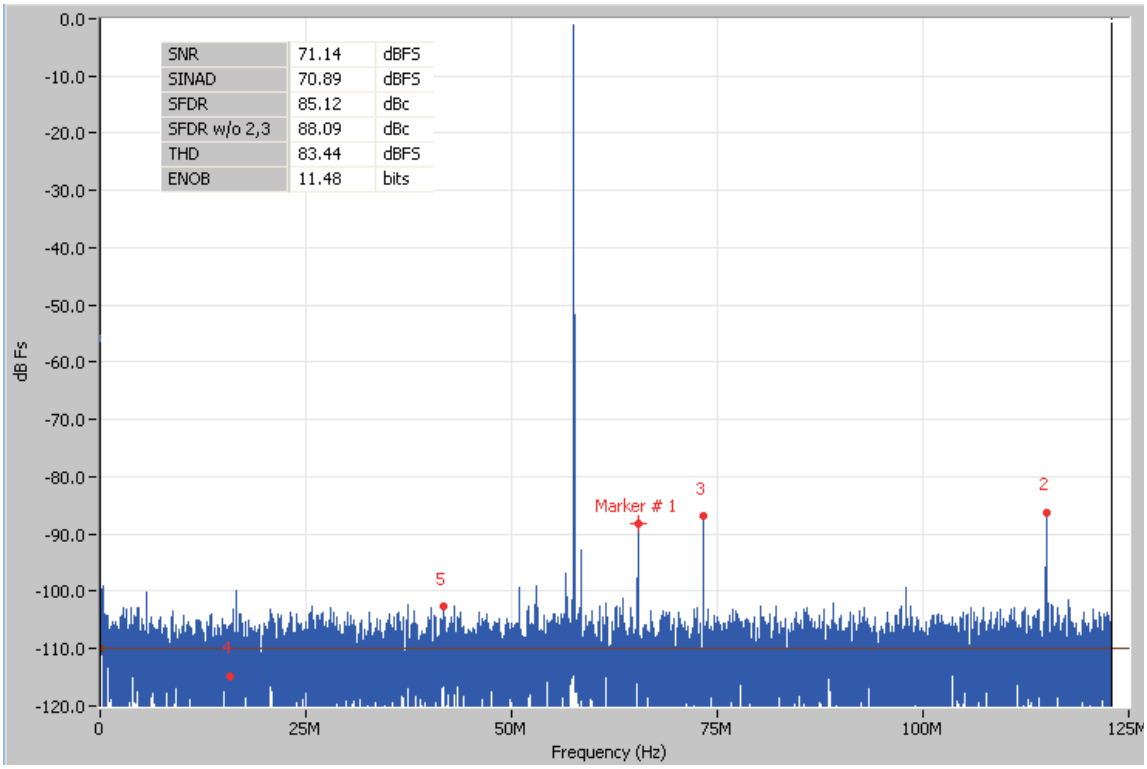

Figure 12. ADC Performance With Clock Through Onboard VCXO, CDCE72010 Configured for Differential LVPECL Output

4.2 TSW1100

When the ADS62PXX is configured in CMOS output mode users can use TI's TSW1100 capture board. Several additional board configuration steps are required before using this option.

- Remove resistor packs with the following reference designators: RN7, RN8, RN9, RN10, RN11, RN12, RN13 and RN14.
- Install TI's SN74AVC16244 buffer into U12 and U13.
- If using the parallel interface mode (JP11=1-2), configure the ADC in CMOS output mode using the silkscreen on JP14.

5 ADC Evaluation

This section describes how to set up a typical ADC evaluation system that is similar to what TI uses to perform testing for data-sheet generation. Consequently, the information in this section is generic in nature and is applicable to all high-speed, high-resolution ADC evaluations. This section covers signal tone analysis, which yields ADC data sheet figures of merit such as signal-to-noise ratio (SNR) and spurious free dynamic range (SFDR).

5.1 Hardware Selection

To reveal the true performance of the ADC under evaluation, great care should be taken in selecting both the ADC signal source and ADC clocking source.

5.1.1 Analog Input Signal Generator

When choosing the quality of the ADC analog input source, consider both the harmonic distortion performance of the signal generator and the noise performance of the source.

In many cases, the harmonic distortion performance of the signal generator is inferior to that of the ADC, and additional filtering is needed if users expect to reproduce the ADC SFDR numbers found in the data sheet. Users can easily evaluate the harmonic distortion of the signal generator by connecting it directly to a spectrum analyzer, measuring the power of the output signal, and comparing that to the power of the integer multiples of the output signal frequency. If the harmonic distortion is worse than the ADC under evaluation, the ADC digitizes the performance of the signal generator and the true SFDR of the ADC is masked. To alleviate this, it is recommended that users provide additional LC filtering after the signal-generator output.

Another important metric when deciding on a signal generator is its noise performance. As with the distortion performance, if the noise performance is worse than that of the ADC under evaluation, the ADC digitizes the performance of the source. Noise can be broken into two components, broadband noise and close-in phase noise. Broadband noise can be improved by adding an LC filter to improve distortion performance; however, the close-in phase noise typically cannot be improved by additional filtering. Therefore, when selecting an analog signal source, it is important to review the manufacturer's phase noise plots and take care to choose a signal generator with the best phase-noise performance.

5.1.2 Clock Signal Generator

Equally important in the high-performance ADC evaluation setup is the selection of the clocking source. Most modern ADCs, the ADS62PXX included, accept either a sinusoidal or a square-wave clock input. The key metric in selecting a clocking source is selecting a source with the lowest jitter. This becomes increasingly important as the ADC input frequency (f_{in}) increases, because the ADC SNR evaluation setups can become jitter-limited (t_j) as shown by the following equation.

$$\text{SNR (dBc)} = 20 \log [2\pi \times f_{in} \times t_j(\text{rms})]$$

In theory, a square-wave source with femtosecond jitter would be ideal for an ADC evaluation setup. However, in practical terms, most commercially available square-wave generators offer jitter measured in picoseconds, which is too great for high-resolution ADC evaluation setups. Therefore, most evaluation setups rely on the ADC internal clock buffer to convert a sinusoidal input signal into a ultra-low-jitter square wave. When selecting a sinusoidal clocking source, it has been shown that phase noise has a direct impact on jitter performance. Consequently, great scrutiny should be applied to the phase-noise performance of the clocking signal generator. TI has found that high-Q monolithic crystal filters can improve the phase noise of the signal generator, and these filters become essential elements of the evaluation setup when high ADC input frequencies are being evaluated.

5.2 Coherent Input Frequency Selection

Typical ADC analysis requires users to collect the resulting time-domain data and perform a Fourier transform to analyze the data in the frequency domain. A stipulation of the Fourier transform is that the signal must be continuous-time; however, this is impractical when looking at a finite set of ADC samples, usually collected from a logic analyzer. Consequently, users typically apply a window function to minimize the time-domain discontinuities that arise when analyzing a finite set of samples. For ADC analysis, window functions have their own frequency signatures or lobes that distort both SNR and SFDR measurements of the ADC.

TI uses the concept of coherent sampling to work around the use of a window function. The central premise of coherent sampling entails that the input signal into the ADC is carefully chosen such that when a continuous-time signal is reconstructed from a finite sample set, no time-domain discontinuities exist. To achieve this, the input frequency must be an integer multiple of the ratio of the ADC sample rate (f_s) and the number of samples collected from the logic analyzer (N_s). The ratio of f_s to N_s is typically referred to as the fundamental frequency (f_f). Determining the ADC input frequency is a two-step process. First, select the frequency of interest for evaluating the ADC; then, divide this by the fundamental frequency. This typically yields a non-integer value, which should be rounded to the nearest odd, preferably prime, integer. Once that integer, or frequency bin (f_{bin}), has been determined, multiply this with the fundamental frequency to obtain a coherent frequency to program into their ADC input signal generator. The procedure is summarized as follows.

$f_f = f_s/N_s$

$f_{bin} = \text{Odd\_round}(f_{desired}/f_f)$

Coherent frequency $= f_f \times f_{bin}$

6 Physical Description

This section describes the physical characteristics and PCB layout of the EVM.

6.1 PCB Layout

The EVM is constructed on a four-layer, 0.062-inch thick PCB using FR-4 material. The individual layers are shown in Figure 13 through Figure 18. The layout features a split ground plane; however, similar performance can be obtained with careful layout using a common ground plane.

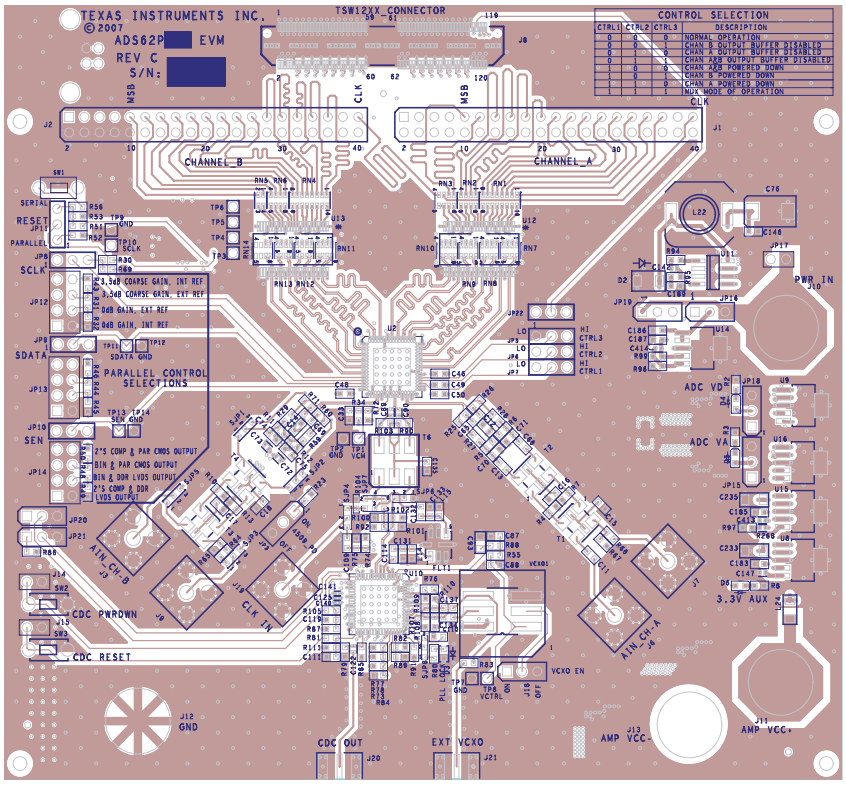

Figure 13. Top Silkscreen

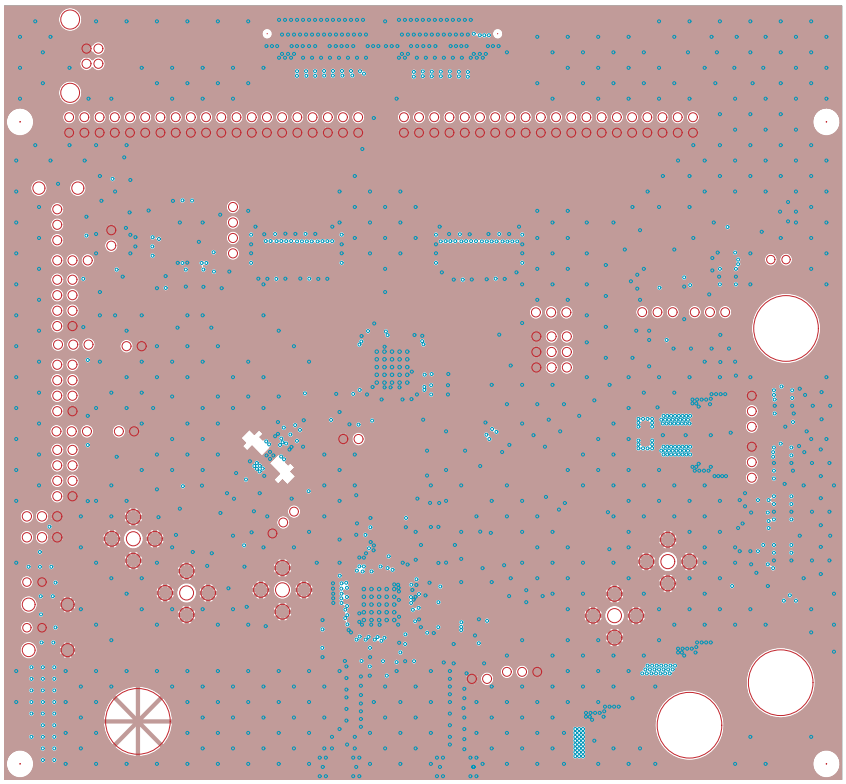

Figure 14. Component Side

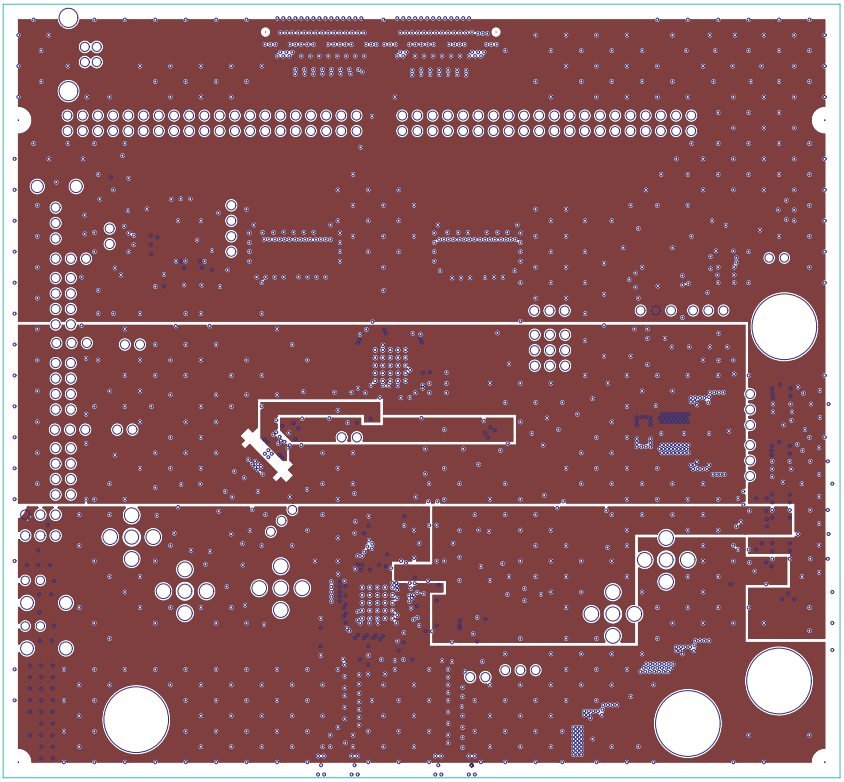

Figure 15. Power Plane 1

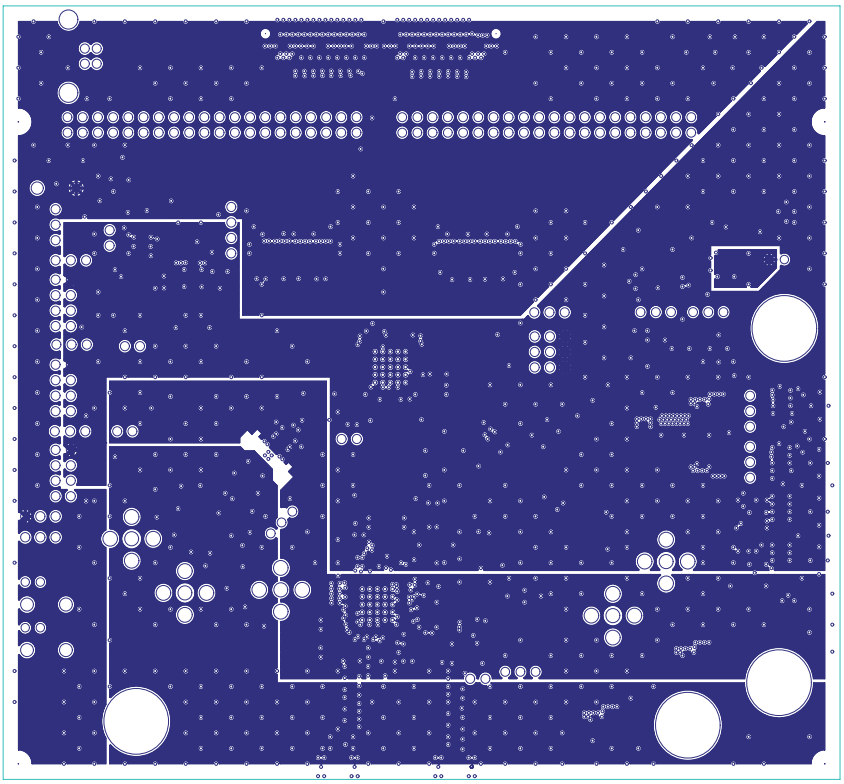

Figure 16. Layer 2

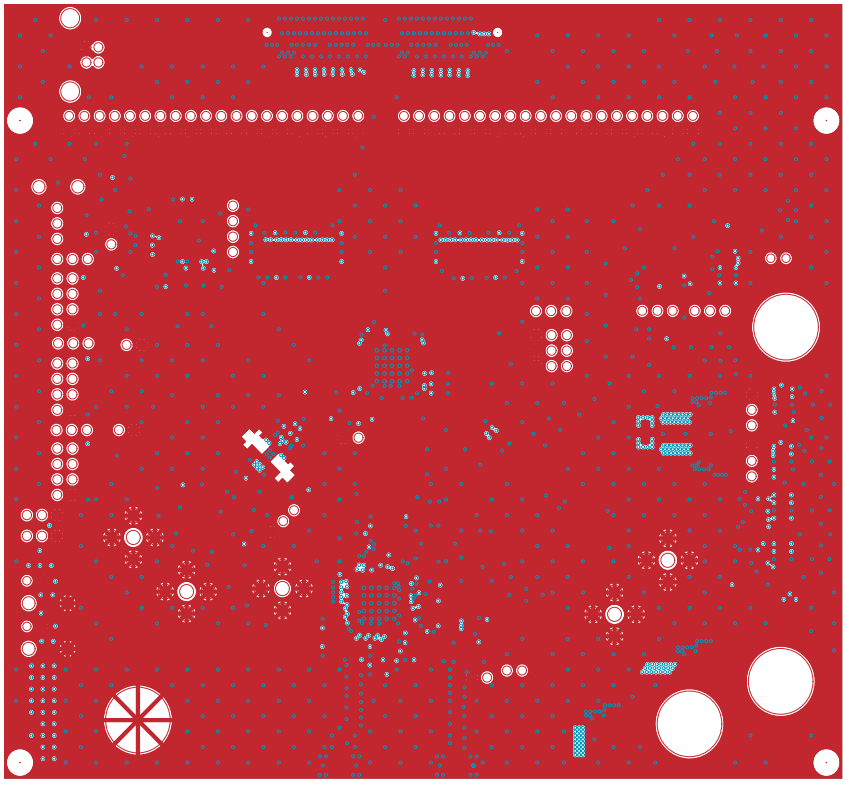

Figure 17. Layer 3

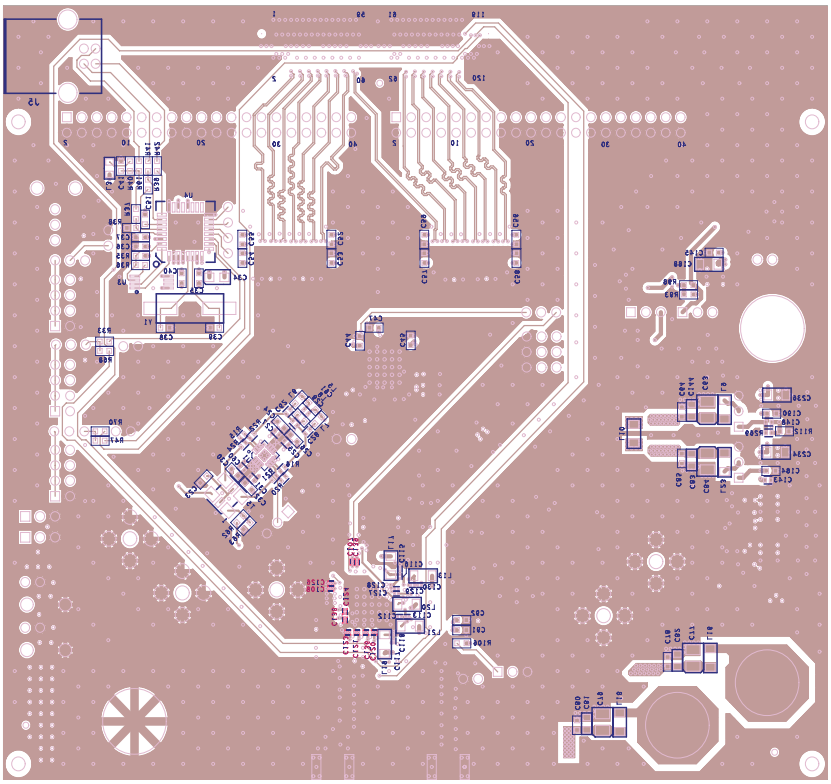

Figure 18. Bottom Side

6.2 Bill of Materials

Table 9. Bill of Materials

Qty	Reference	Value	Footprint	MFR	Part Number	DNI = Do Not Install
4	C1,C6,C43,C64	1µF	603	Panasonic	ECJ-1VB1A105K	
15	C2, C8, C19–C23, C52–C59	0.1µF	603	Panasonic	ECJ-1VB1C104K	
4	C3, C5, C7, C10	22µF	smd_cap_1210_pol	Kemet	T491A226M010AT	
2	C4, C9	10µF	smd_cap_1210_pol	Kemet	B45197A3106K209	
23	C11–C18, C33,C35–C37, C40,C44–C50, C66–C68	0.1µF	603	Murata	GRM188R71H104KA93D	
4	C24, C26, C30, C32	10µF	603	Murata	GRM188R60J106ME47D	
6	C25, C27, C31, C60, C72,C73	0.1µF	402	Panasonic	ECJ-0EB1C104K	
2	C28, C62	4.7pF	402	Panasonic	ECD-G0E4R7C	
2	C29, C61	5pF	402	Panasonic	ECJ-0EC1H050C	
1	C34	10µF	TANT_A	Kemet	T491A106M006AS	
2	C38, C39	27pF	603	Murata	GRM1885C2A270JA01D	
1	C41	0.01µF	603	Kemet	C0603C103K1RACTU	
2	C42, C63	33µF	TANT_B	Kemet	B45196H1336K209	
1	C51	33nF	603	AVX	06035C333KAT2A	
0	C65, C69	3.3pF	603	Panasonic	ECJ-1VC1H3R30C_DNI	DNI
4	C70, C71, C74, C75	5.6pF	603	AVX	06035A5R6CAT2A_DNI	DNI
2	C119, C120	0.01µF	402	Panasonic	ECJ-0EB1E103K	
2	C183, C184	1µF	603	Panasonic	ECJ-1V41E105M	
2	C233, C234	2.2µF	1206	Panasonic	ECJ-HVB1A225K	
2	D1, D2	GREEN	603	Panasonic	LNJ312G8TRA	
3	JP3, JP15, JP16	HEADER_1x3_100_430L		Samtec	HMTSW-103-07-G-S-.240	(SHUNT 2-3)
7	JP5–JP11	HEADER_1x3_100_430L		Samtec	HMTSW-103-07-G-S-.240	(SHUNT 1-2)
1	JP13	HEADER 4x2		Molex	90131-0124	
2	JP12, JP14	HEADER 4x2		Molex	90131-0124	(SHUNT 1-2)
2	J1, J2	HMTSW-120-07-G-D-.240		Samtec	HMTSW-120-07-G-D-.240	
4	J3, J4, J6, J9	SMA		Johnson Components	142-0701-201	
1	J5	CONN USB TYP B FEM		Milmax	897-43-004-90-000	
0	J7	SMA		Johnson Components	142-0701-201	DNI
1	J8	CONN_QTH_30X2-D-A		Samtec	QTH-060-02-F-D-A	
2	L1,L2	68 at 100MHz	603	Steward	MI0603J680R-10	
1	L3	1K at 100MHZ	805	Murata	BLM21AG102SN1D	
2	L4,L9	68 at 100MHz	603	Steward	MI0603J680R-10	
2	L5,L8	47nH	603	Coilcraft	0603CS-47NXJL	
2	L6,L7	150	805	API Delavan Inc	0805-151J	
1	P1	3.3VD		Allied Electronics	ST-351A	
1	P2	DGND		Allied Electronics	ST-351B	
1	P3	3.3VA		Allied Electronics	ST-351A	
1	P4	AGND		Allied Electronics	ST-351B	
1	P5	5V_AUX_IN		Allied Electronics	ST-351A	
1	P6			Allied Electronics	ST-351A	
2	RN1,RN4	22	rnet8_16_0603	CTS	742C163220JTR	
2	RN2,RN6	22	rnet4_8_0603	Panasonic	EXB-38V220JV	
2	RN3,RN5	22	rnet2_4_0603	Panasonic	EXB-34V220JV	
4	RN7–RN10	0 Ω	rnet8_16_0603	CTS	742C163000X	
2	R1,R2	750	603	Panasonic	ERJ-3EKF7500V	
8	R4–R7, R10–R13	49.9	603	Panasonic	ERJ-3EKF49R9V	
2	R15, R20	348	402	Panasonic	ERJ-2RKF3480X	
2	R16, R22	68	402	Yageo Corporation	RC0402FR-0768RL	
0	R17, R18	121	603	Panasonic	ERJ-3EKF1210V	DNI
1	R19	49.9	603	Panasonic	ERJ-3EKF49R9V	
2	R21, R24	100	402	Panasonic	ERJ-2RKF1000X	
1	R23	10K	603	Panasonic	ERJ-3EKF1002V	

Table 9. Bill of Materials (continued)

Qty	Reference	Value	Footprint	MFR	Part Number	DNI = Do Not Install
0	R25, R26, R60, R71	49.9	603	Panasonic	ERJ-3EKF49R9V_DNI	DNI
4	R27, R28, R29, R59	4.99	603	Yageo	RC0603FR-074R99L	
8	R30, R33, R34, R47, R54, R55, R61, R72	0 Ω	603	Panasonic	ERJ-3GEY0R00V	
9	R31, R32, R43–R46, R48–R50	1K	603	Panasonic	ERJ-3EKF1001V	
1	R35	10K	603	Panasonic	ERJ-3GEYJ103V	
1	R36	2.21K	603	Panasonic	ERJ-3EKF2211V	
1	R37	4.7K	603	Panasonic	ERJ-3GEYJ472V	
0	R38	10K	603	Panasonic	ERJ-3EKF1002V_DNI	DNI
1	R39	1.5K	603	Panasonic	ERJ-3EKF1501V	
0	R40, R68–R70	0 Ω	603	Panasonic	ERJ-3GEY0R00V_DNI	DNI
2	R41, R42	26.7	603	Panasonic	ERJ-3EKF26R7V	
2	R51, R56	10	603	Panasonic	ERJ-3EKF10R0V	
2	R52, R53	10K	603	Panasonic	ERJ-3EKF1002V	
2	R57, R58	22	603	Yageo	RC0603FR-0722RL	
0	R62, R64 ,R66	0 Ω	603	DALE	CRCW06030000Z0EA_DNI	DNI
3	R63, R65, R67	0 ohm	603	DALE	CRCW06030000Z0EA	
0	SJP1, SJP2	JUMPER_1x3_SMT	SMD_BRIDGE_1x3_0603	DNI	DNI	(SHUNT 2-3)
0	SJP3	JUMPER_1x3_SMT	SMD_BRIDGE_1x3_0603	DNI	DNI	(NO SHUNT)
0	SJP5	JUMPER_1x3_SMT	SMD_BRIDGE_1x3_0603	DNI	DNI	(SHUNT 1-2)
1	SW1	SW PUSHBUTTON	SW_RESET_PTS635	C & K Switch	PTS635SL43	
4	TP1, TP10, TP11, TP13	Test Point White	testpoint	Keystone	5002	
4	TP2, TP9, TP12,TP14	Test Point Black	testpoint	Keystone	5001	
4	TP3–TP6	T POINT R	TESTPOINT	Keystone	5002	
5	T1–T5	WBC1-1TL	XFMR_TC4-1W	Coilcraft	WBC1-1TL	
1	T6	TC1-1T	XFMR_TC4-1W	Minicircuits	TC1-1T	
1	U1	THS4509	QFN16	Texas Instruments	THS4509RGTT	
1	U2	ADS62PXX	QFN64	Texas Instruments	ADS62PXX	
1	U3	93C66B	TSSOP8	Microchip	93C66B	
1	U4	FT245BM	PQFP32	Future Technology Devices	FT245BM	
2	U5, U7	TPS79633DCQ	SOT_223_6_TG	Texas Instruments	TPS79633DCQ	
0	U12, U13	SN74AVC16244DGGR	TSSOP_48_496x244_20	Texas Instruments	SN74AVC16244DGGR_DNI	DNI
1	Y1	6.0000MHz	smd_csm-7_xtal	ECS	ECS-60-32-5PDN-TR	
10	Z_SH-H1	SHUNT-HEADER		Keltron	MJ-5.97-G or equivalent	SHUNT FOR HEADER
3	Z_SH-J1, Z_SH-J2, Z_SH-J5	SHUNT-JUMPER-0603		Panasonic	ERJ-3GE0R00X	SHUNT FOR JUMPER
4	Z_STANDOFF SCREW1,Z_STANDOFF SCREW2,Z_STANDOFF SCREW3,Z_STANDOFF SCREW4	PANHEAD SCREW 4-40 x 3/8		Building Fasteners	PMS 440 0038 PH	SCREW FOR STANDOFF
4	Z_STANDOFF1, Z_STANDOFF2,Z_STANDOFF3, Z_STANDOFF4	STANDOFF ALUM HEX 4-40 x .500		Keystone	2203	STANDOFF

6.3 EVM Schematics

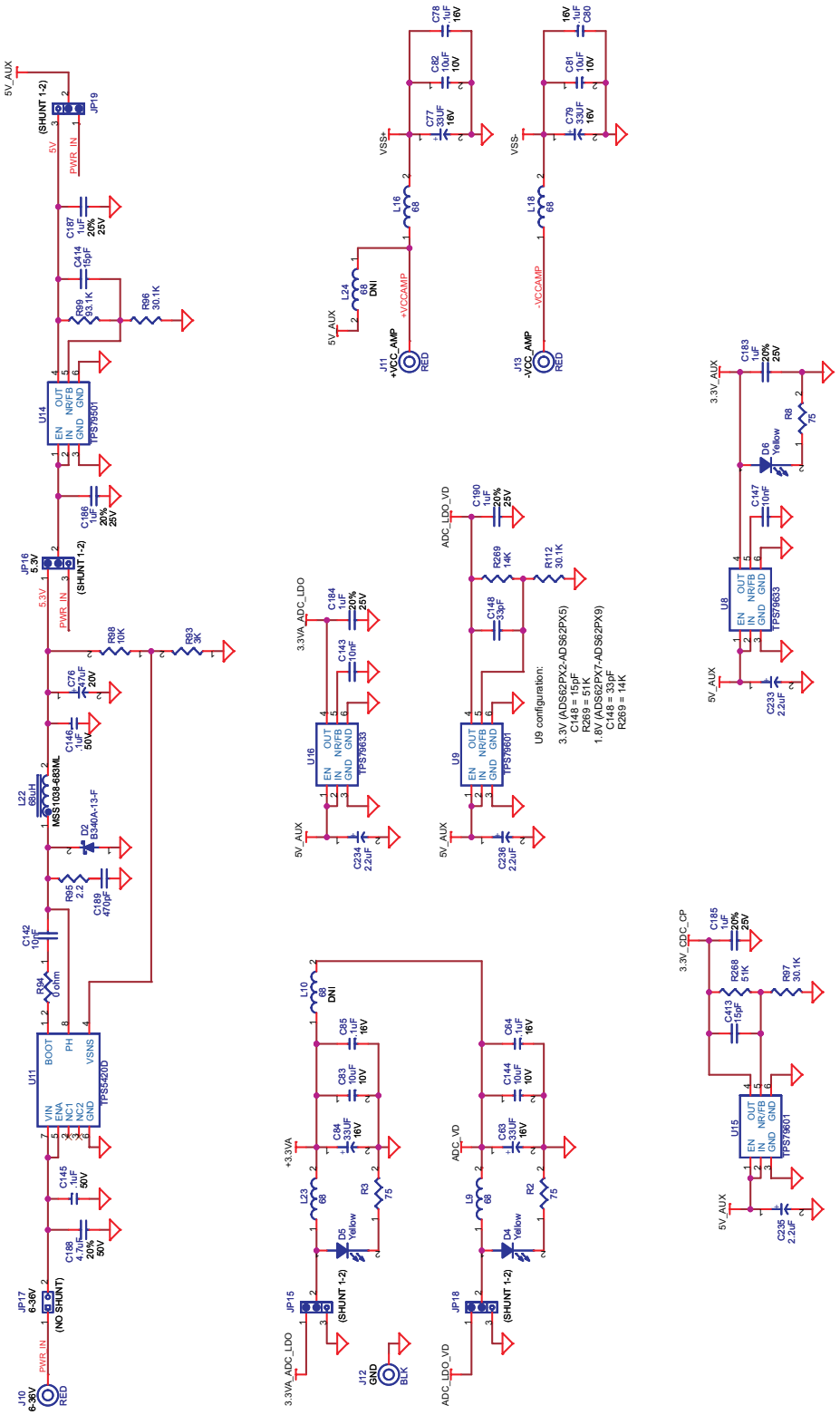

Figure 19. EVM Schematic, Sheet 1

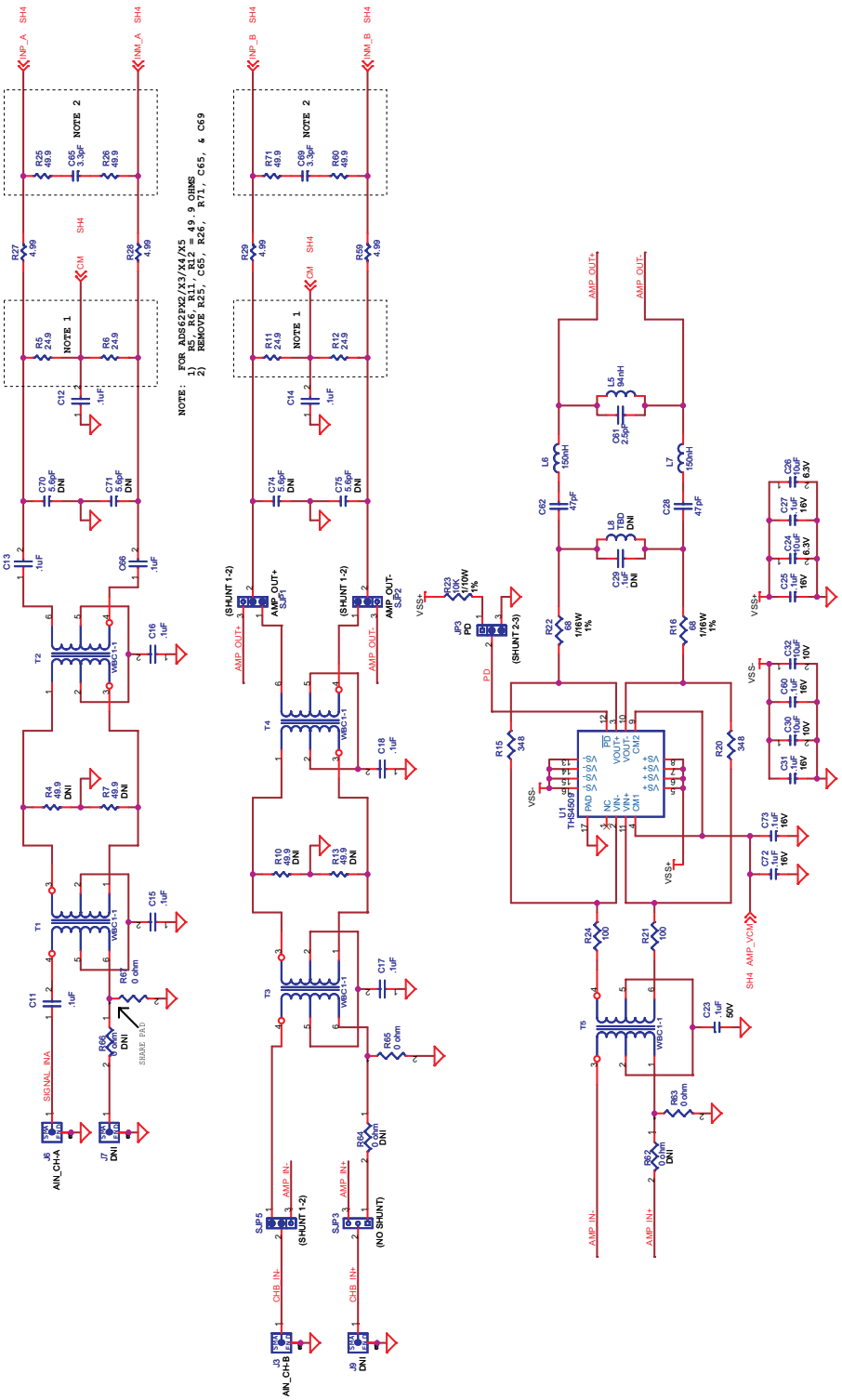

Figure 20. EVM Schematic, Sheet 2

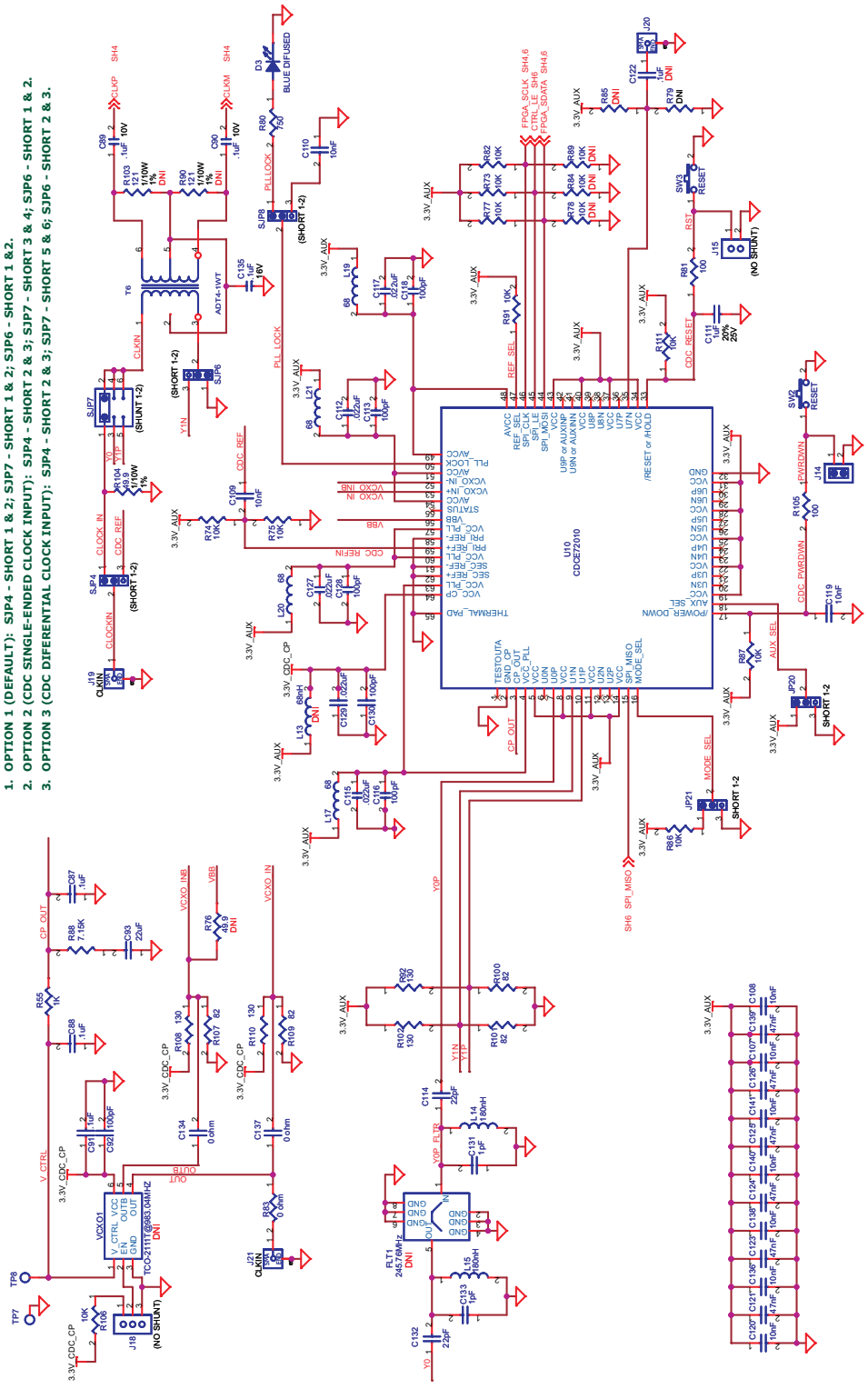

Figure 21. EVM Schematic, Sheet 3

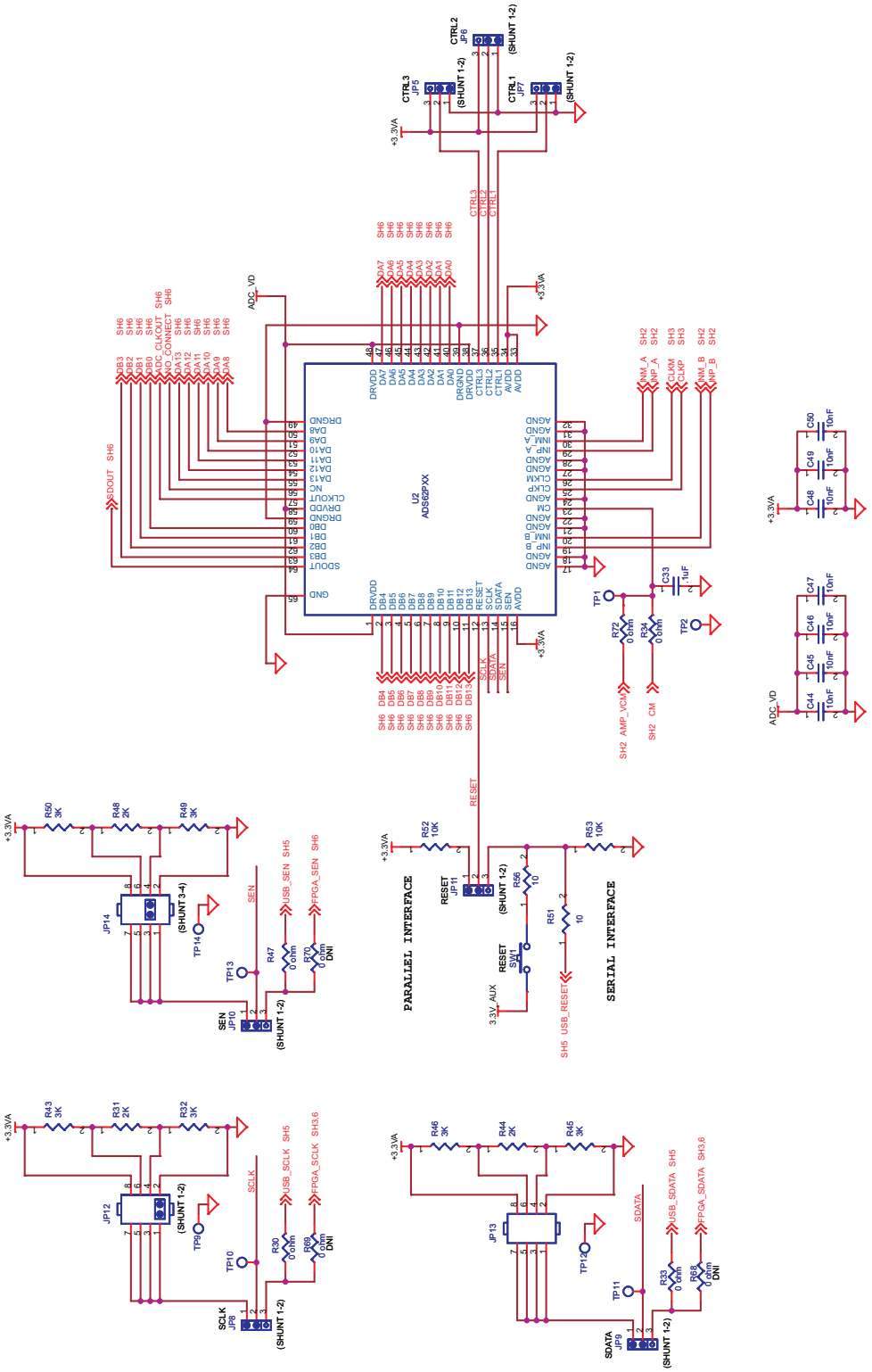

Figure 22. EVM Schematic, Sheet 4

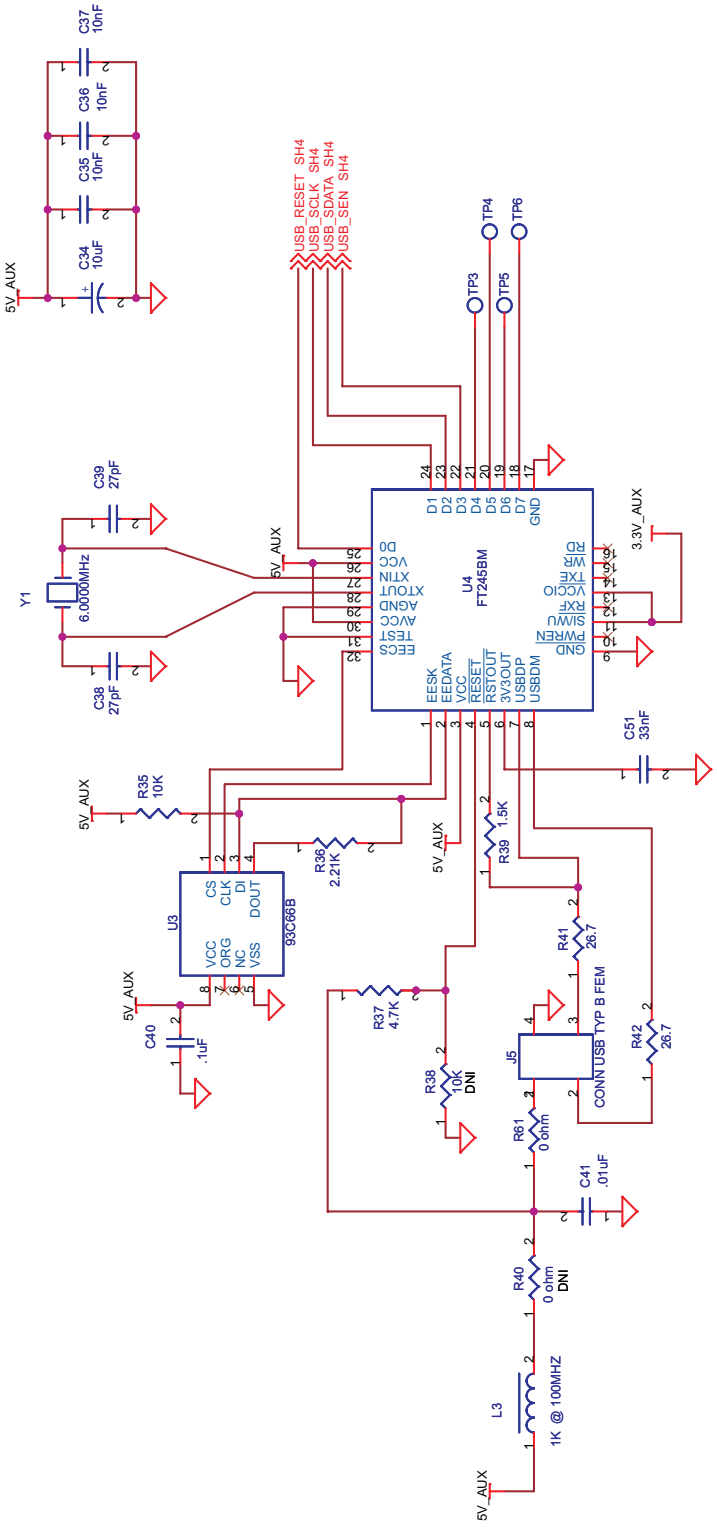

Figure 23. EVM Schematic, Sheet 5

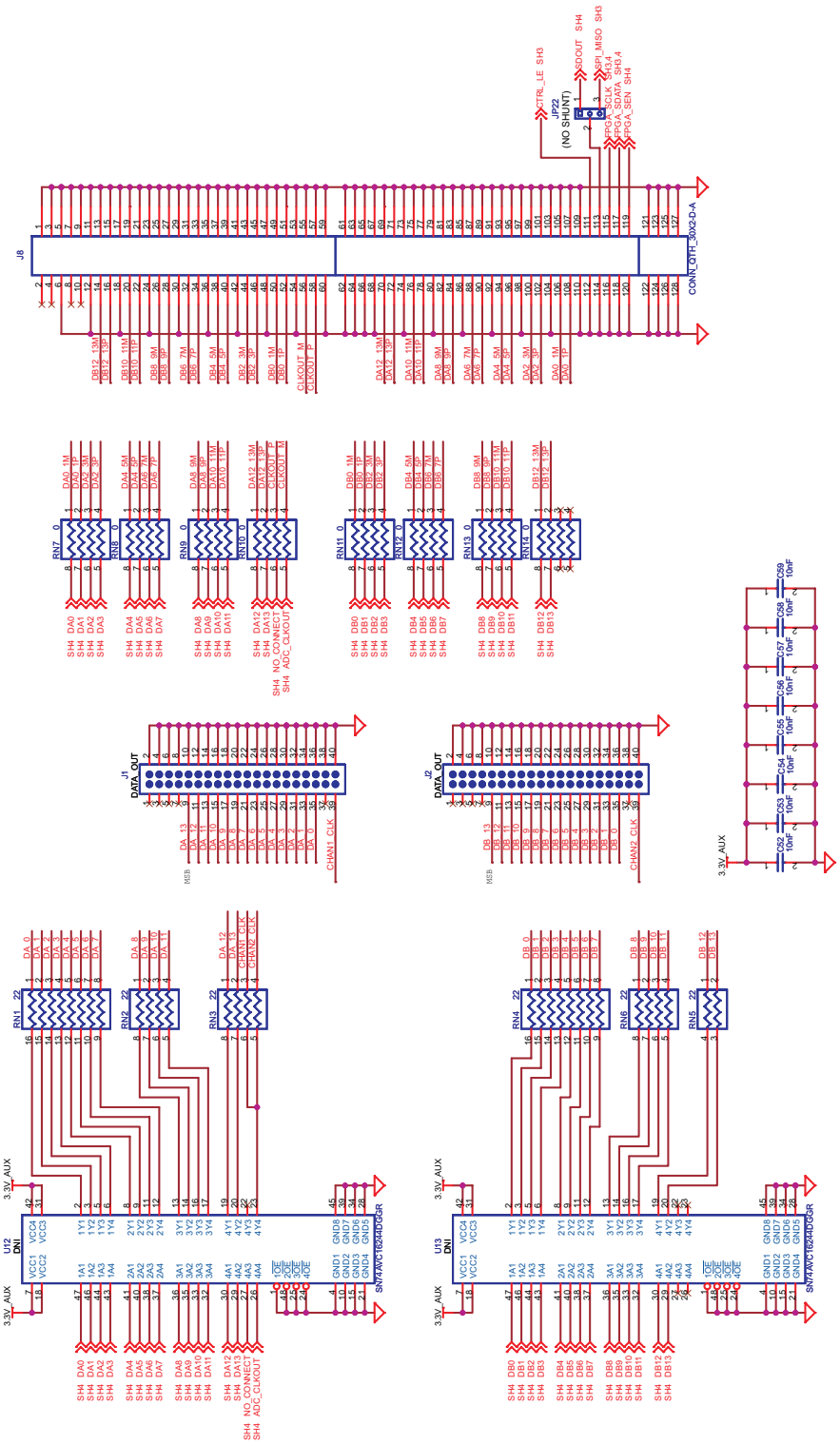

Figure 24. Breakout Board Schematic, Sheet 6

EVALUATION BOARD/KIT IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of –0.3 V to 5.6 V and the output voltage range of –0.3 V to 5.6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 25°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265