FAST CMOS OCTAL BUS TRANSCEIVER (OPEN DRAIN)

IDT74FCT621T/AT

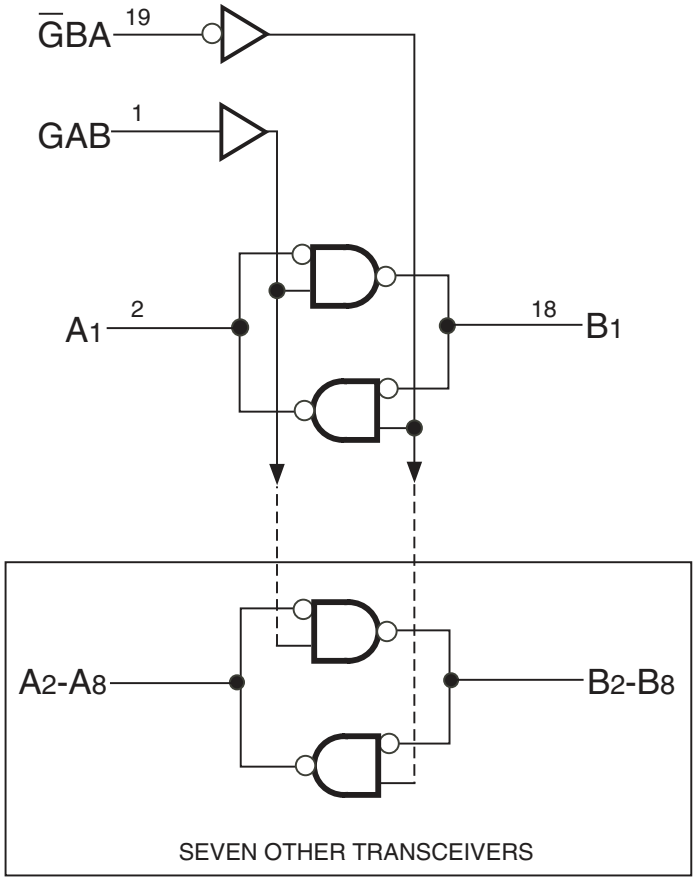
FEATURES:

- Std. and A grades
- Low input and output leakage ≤1µA (max.)
- CMOS power levels
- True TTL input and output compatibility:
  - *V_{OH} = 3.3V (typ.)*
  - *V_{OL} = 0.3V (typ.)*
- Meets or exceeds JEDEC standard 18 specifications
- Power off disable outputs permit "live insertion"
- Available in SOIC package

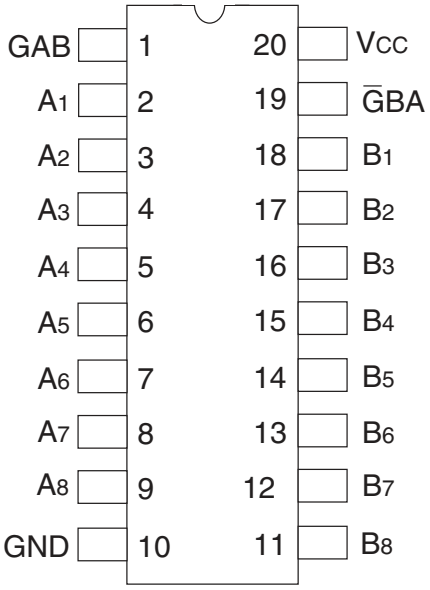
DESCRIPTION:

The IDT74FCT621T is an octal transceiver with non-inverting Open-Drain bus compatible outputs in both send and receive directions. The B bus outputs are capable of sinking 64mA providing very good capacitive drive characteristics. These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
$\overline{G}$BA, GAB	Enable Inputs
A_1 – A_8	A Inputs or Open-drain Outputs
B_1 – B_8	B Inputs or Open-drain Outputs

FUNCTION TABLE(1)

Enable Inputs		
$\overline{G}$BA	GAB	Function
L	L	B data to A bus
H	H	A data to B bus
H	L	OFF
L	H	B data to A bus A data to B bus

NOTE:
1. H = HIGH Voltage Level.
L = LOW Voltage Level.
OFF = HIGH if pull-up resistor is connected to Open-Drain output.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max., V_I = 2.7V		—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max., V_I = 0.5V		—	—	±1	µA
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OH}	Output HIGH Current	V_{CC} = Max. V_{IN} = V_{IH} or V_{IL}	V_{OH} = Vcc (Max.)	—	—	20	µA
V_{OL}	Output LOW Voltage (B Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA [3]	—	0.3	0.55	V
V_{OL}	Output LOW Voltage (A Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA [3]	—	0.3	0.5	V
I_{OFF}	Input/Output Power Off Leakage[4]	V_{CC} = 0V, V_{IN} or V_O - 4.5V		—	—	±1	µA
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = max., V_{IN} = GND or Vcc		—	0.01	1	mA

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.
4. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current[4]	Vcc = Max. Outputs Open $\overline{G}BA$ = GAB = GND or V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6,7]	Vcc = Max. Outputs Open $\overline{G}BA$ = GAB = GND or V_{CC} One Bit Toggling at f_i =10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.5	
		Vcc = Max. Outputs Open $\overline{G}BA$ = GAB = GND or V_{CC} Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3	6[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5	14[5]	

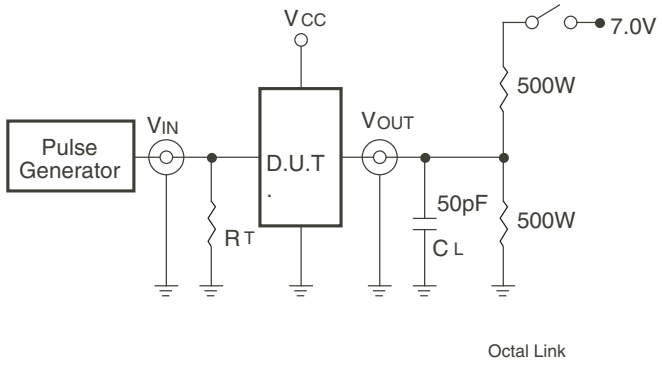
NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.
7. This test is performed with outputs tied to GND through a pull-down resistor.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT74FCT621T		IDT74FCT621AT		Unit
			Min.[2]	Max.	Min.[2]	Max.	
t_{PLH}	Propagation Delay, A to B	C_L = 50pF	5.5	13	5.5	12	ns
t_{PHL}		R_L = 500Ω	1.5	8.5	1.5	6.8	
t_{PLH}	Propagation Delay, B to A		5.5	12.5	5.5	12	ns
t_{PHL}			1.5	8	1.5	6.4	
t_{PLH}	Propagation Delay, $\overline{G}$BA to A		5.5	14	5.5	13	ns
t_{PHL}			1.5	8.5	1.5	6.8	
t_{PLH}	Propagation Delay, $\overline{G}$AB to B		5.5	14	5.5	13	ns
t_{PHL}			1.5	8	1.5	6.4	

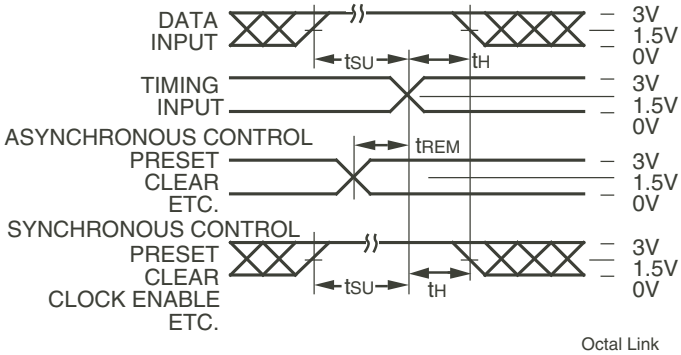
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS



Octal Link

Test Circuits for All Outputs



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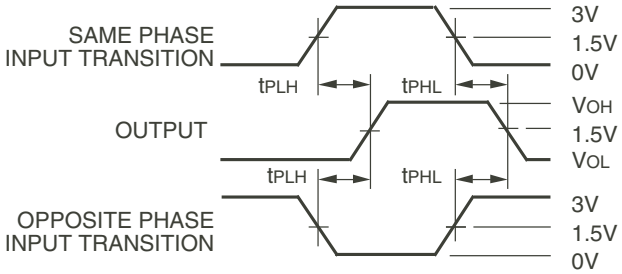
Set-Up, Hold, and Release Times



Octal Link

Propagation Delay

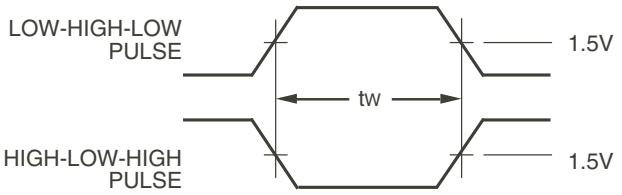
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

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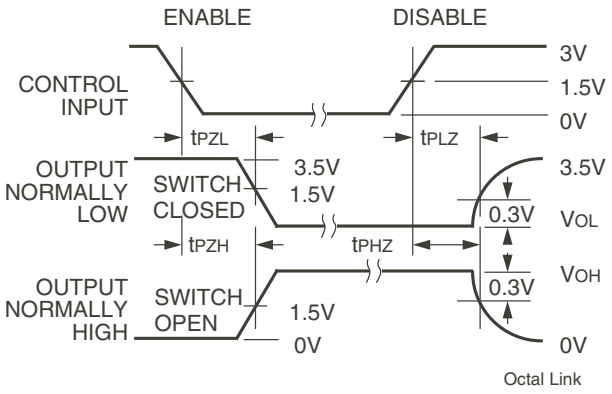

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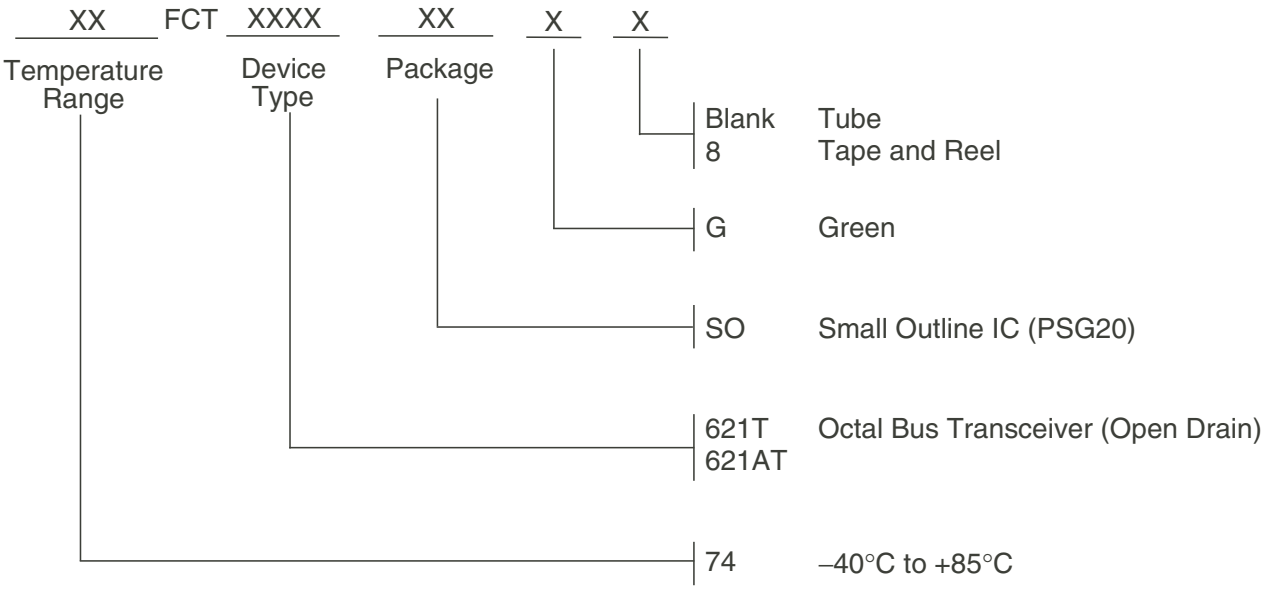
Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



Datasheet Document History

10/10/2009	Pg. 6	Updated the ordering information by removing the "IDT" notation and non RoHS part.
10/22/2014	Pg. 6	Added Tape & Reel to ordering information.
11/26/2016	Pg. 6	Updated ordering information diagram temperature symbol, removed tray and created Green option in greater detail.

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