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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

December 2014

FCD2250N80Z

N-Channel SuperFET® II MOSFET

800 V, 2.6 A, 2.25 Ω

Features

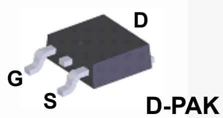
- $R_{DS(on)}$ = 1.8 Ω (Typ.)
- Ultra Low Gate Charge (Typ. Q_g = 11 nC)
- Low E_{oss} (Typ. 1.1 uJ @ 400V)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 51 pF)
- 100% Avalanche Tested
- RoHS Compliant
- ESD Improved Capability

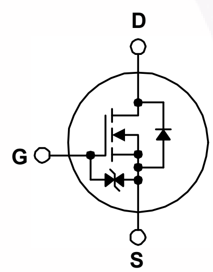
Applications

- AC - DC Power Supply
- LED Lighting

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as Audio, Laptop adapter, Lighting, ATX power and industrial power applications.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FCD2250N80Z	Unit
V_{DSS}	Drain to Source Voltage		800	V
V_{GSS}	Gate to Source Voltage	- DC	±20	V
		- AC (f > 1 Hz)	±30	
I_D	Drain Current	- Continuous (T_C = 25°C)	2.6	A
		- Continuous (T_C = 100°C)	1.7	
I_{DM}	Drain Current	- Pulsed (Note 1)	6.5	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		21.6	mJ
I_{AR}	Avalanche Current (Note 1)		0.52	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		0.39	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	(T_C = 25°C)	39	W
		- Derate Above 25°C	0.31	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FCD2250N80Z	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	100	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCD2250N80Z	FCD225080Z	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	800	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	-	0.85	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 800 V, V_{GS} = 0 V	-	-	25	μA
		V_{DS} = 640 V, V_{GS} = 0 V, T_C = 125°C	-	-	250	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±10	μA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 0.26 mA	2.5	-	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 1.3 A	-	1.87	2.25	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 1.3 A	-	2.28	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	-	440	585	pF
C_{oss}	Output Capacitance		-	16	22	pF
C_{rss}	Reverse Transfer Capacitance		-	0.75	-	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1 MHz	-	8.4	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	51	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 640 V, I_D = 2.6 A, V_{GS} = 10 V (Note 4)	-	11	14	nC
Q_{gs}	Gate to Source Gate Charge		-	2.2	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	4.3	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	2.8	-	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 2.6 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)	-	11	32	ns
t_r	Turn-On Rise Time		-	6.7	23	ns
$t_{d(off)}$	Turn-Off Delay Time		-	26	62	ns
t_f	Turn-Off Fall Time		-	8.7	27	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	2.6	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	6.5	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 2.6 A	-	-	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 2.6 A, dI_F/dt = 100 A/μs	-	260	-	ns
Q_{rr}	Reverse Recovery Charge		-	2.2	-	μC

Notes:

1. Repetitive rating: pulse width limited by maximum junction temperature.
2. I_{AS} = 0.52 A, R_G = 25 Ω, starting T_J = 25°C
3. I_{SD} ≤ 2.6 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C
4. Essentially independent of operating temperature typical characteristic.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

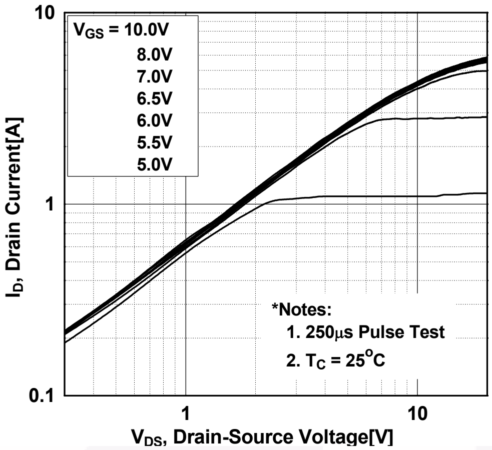


Figure 2. Transfer Characteristics

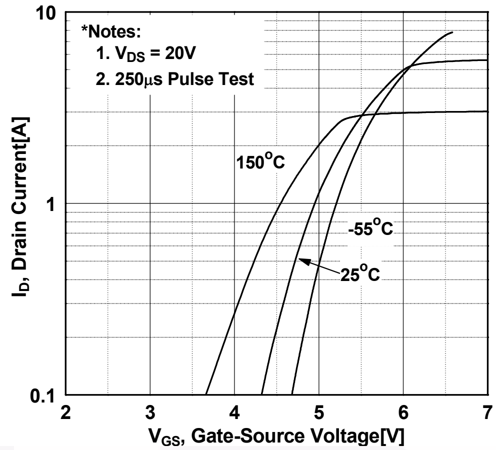


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

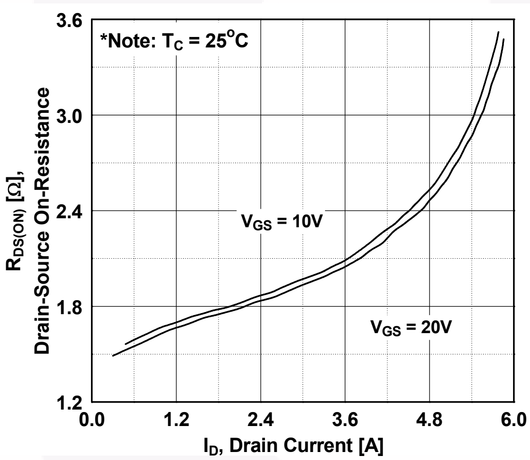


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

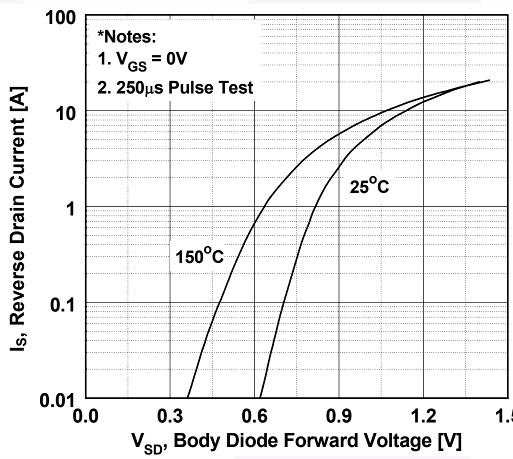


Figure 5. Capacitance Characteristics

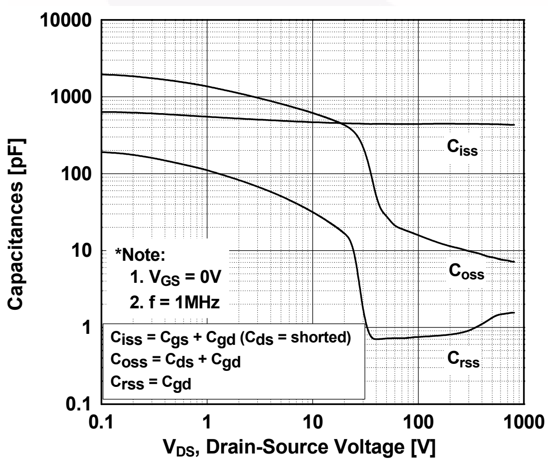
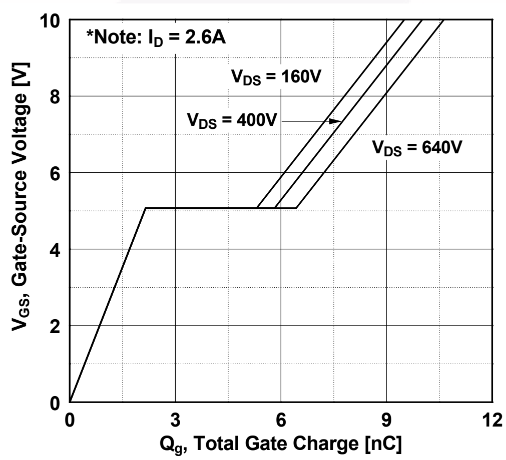


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

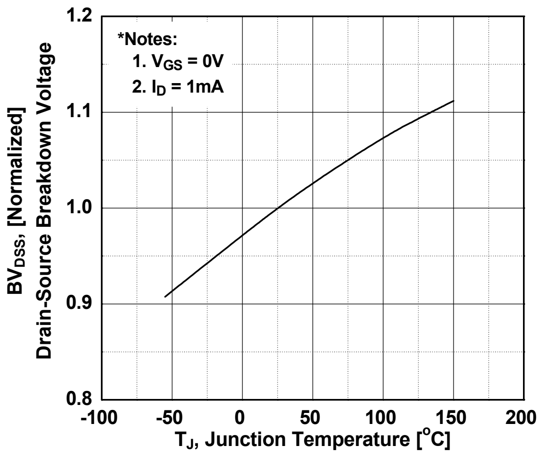


Figure 8. On-Resistance Variation vs. Temperature

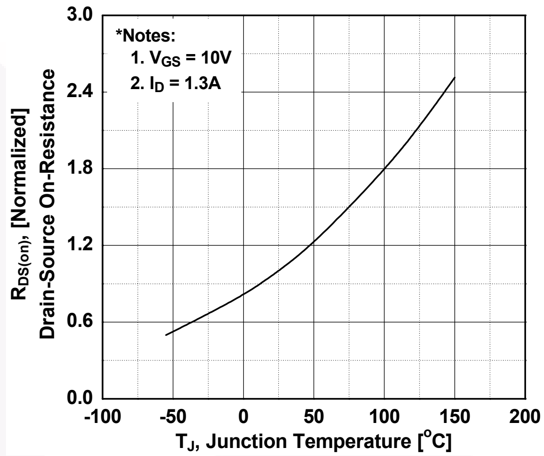


Figure 9. Maximum Safe Operating Area

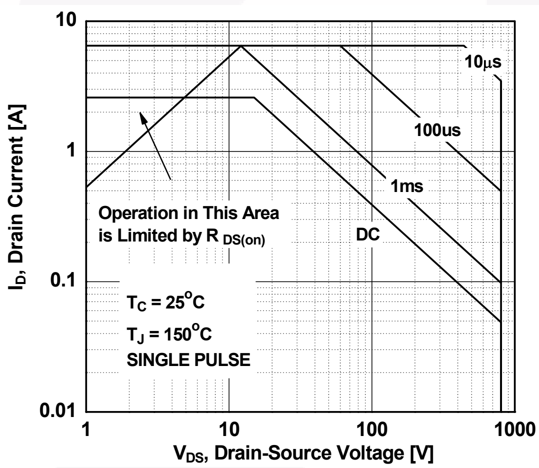


Figure 10. Maximum Drain Current vs. Case Temperature

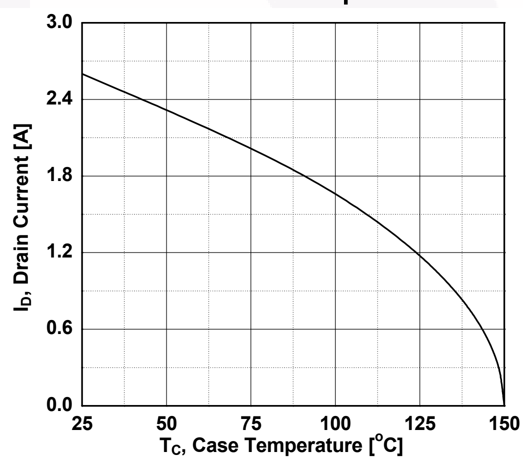
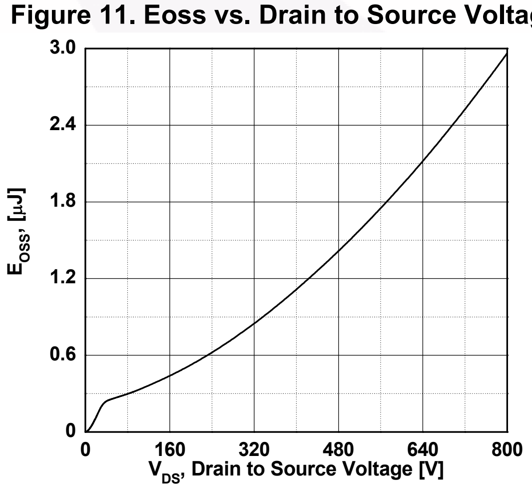
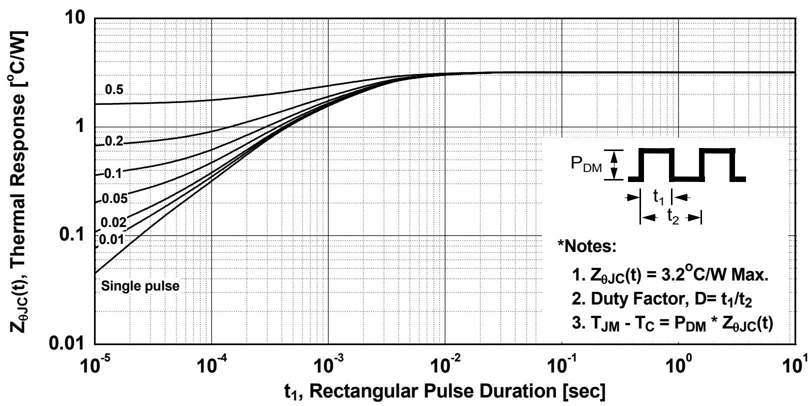


Figure 11. Eoss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



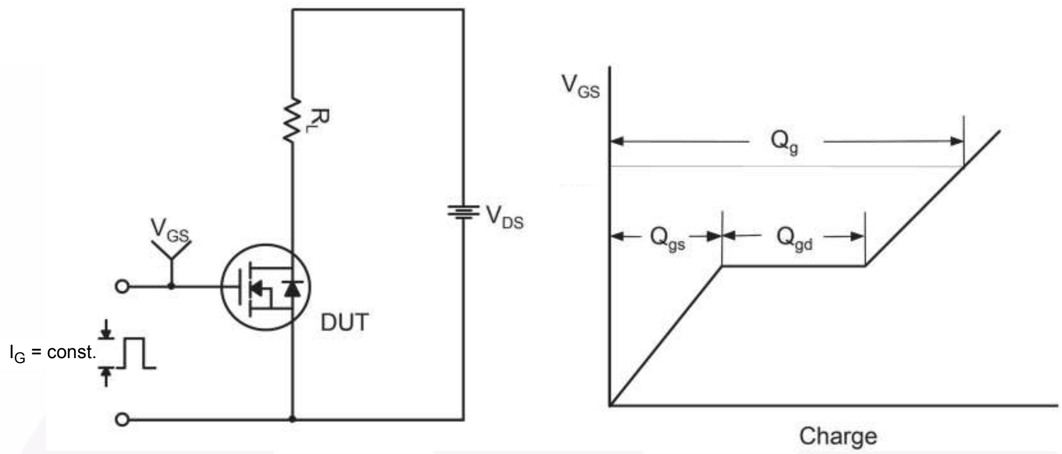


Figure 13. Gate Charge Test Circuit & Waveform

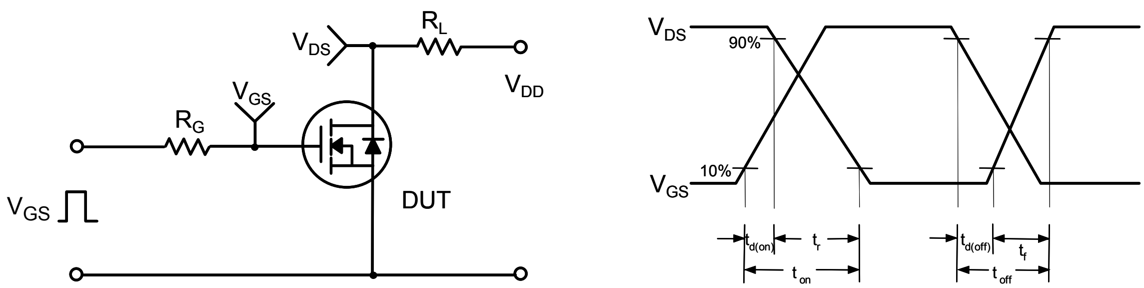


Figure 14. Resistive Switching Test Circuit & Waveforms

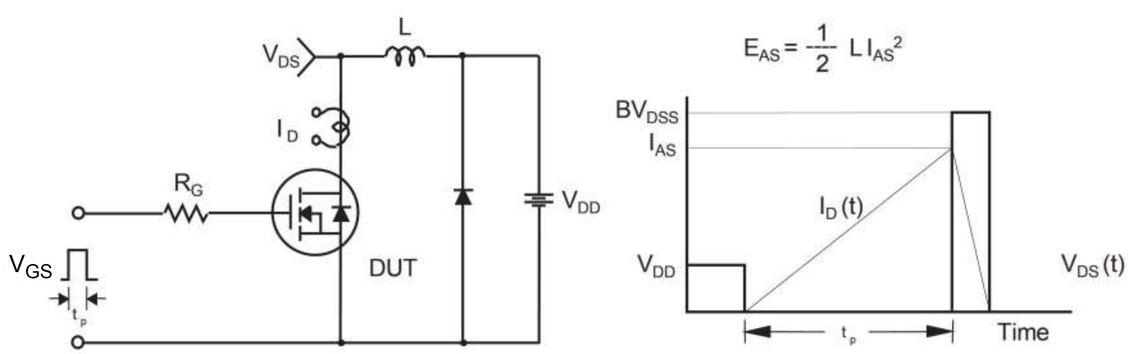


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

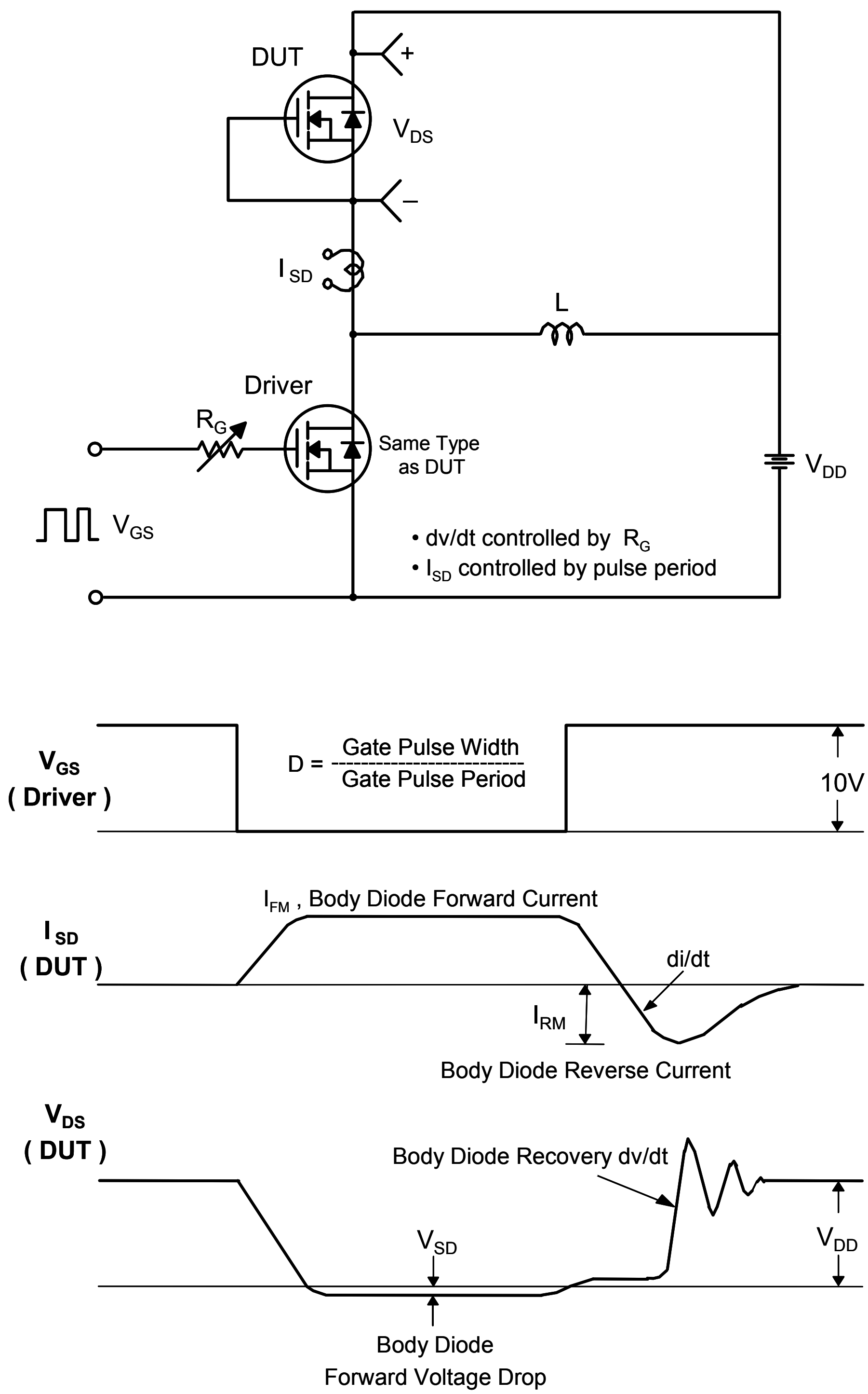
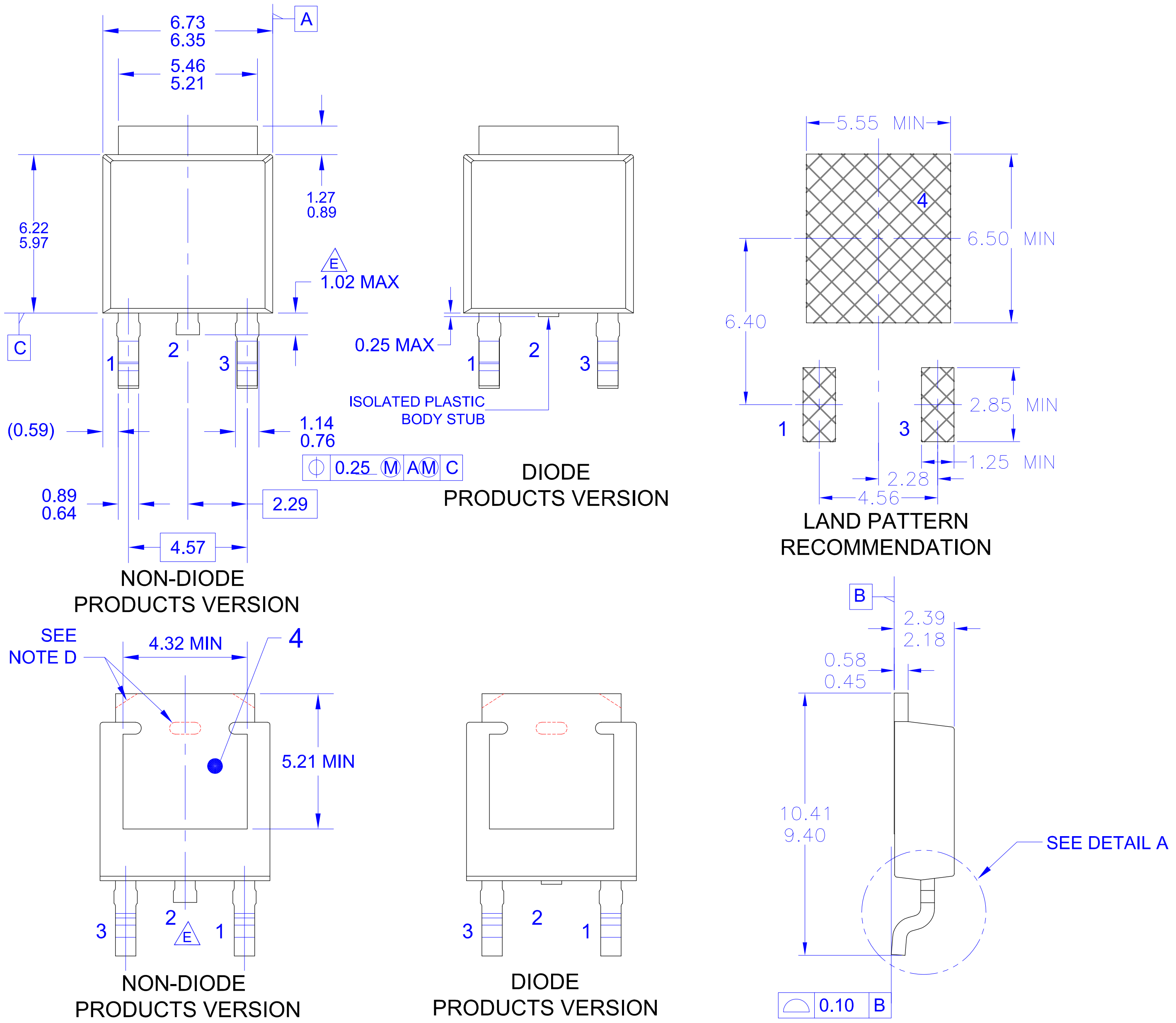
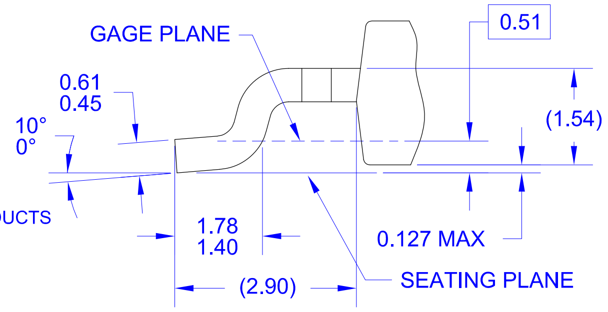


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



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FAIRCHILD

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