FPC202 Dual Port Controller With Expanded I/Os

1 Features

- Supports control signal management and I2C aggregation across two ports
- Four LED drivers and 12 general-purpose I/Os per port
- General-purpose outputs can be used to drive >4 LEDs per port
- Combine multiple FPC202s to control 28 total ports through a single host interface
- Eliminates need for discrete I2C multiplexers, LED drivers, and high-pin-count FPGA/CPLD control devices
- Reduces PCB routing complexity by handling all low-speed control signals close to the port
- Selectable I2C (up to 1 MHz) or SPI (up to 10 MHz) host control interface
- Automatic pre-fetching of critical, user-specified data from the modules
- Broadcast mode allows writes to all ports simultaneously across all FPC202 controllers
- Advanced LED features for port status indication, including programmable blinking and dimming
- Customizable interrupt events
- Separate host-side I/O voltage: 1.8 V to 3.3 V
- Small QFN package enabling placement on bottom side of PCB underneath ports

2 Applications

- ToR/aggregation/core switch and router
- Wireless infrastructure base band unit and remote radio unit
- Network Interface Card (NIC) and Host Bus Adapter (HBA)
- Storage cards and storage racks
- SFP, QSFP, QSFP-DD, OSFP, Mini-SAS HD port management

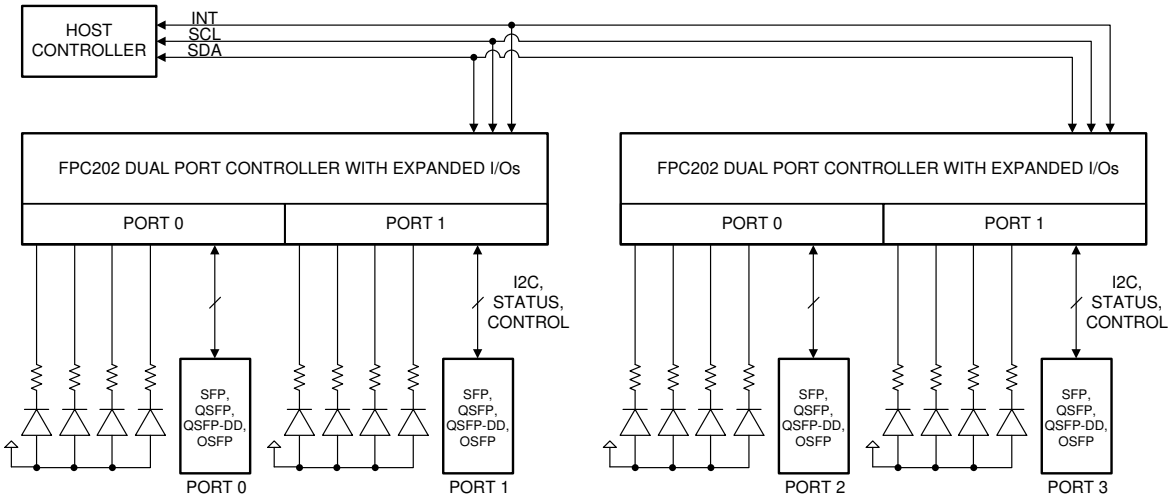
3 Description

The FPC202 dual port controller serves as a low-speed signal aggregator for common port types such as SFP, QSFP, Mini-SAS HD, and others. The FPC202 aggregates all low-speed control and I2C signals across two ports and presents a single easy-to-use management interface to the host (I2C or SPI). Multiple FPC202s can be used in high-port-count applications with one common control interface to the host.

Device Information(1)

DEVICE NUMBER	PACKAGE	BODY SIZE (NOM)
FPC202	QFN (56)	5.00 mm × 11.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2017) to Revision A (January 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

5 Description (continued)

The FPC202 is designed to allow placement on the bottom side of the PCB, underneath the press fit connector, to simplify routing. This localized control of the ports' low-speed signals cuts system bill of materials (BOM) cost by enabling the use of smaller I/O count control devices (FPGAs, CPLDs, MCUs) and by reducing routing layer congestion.

The FPC202 is compatible with standard SFF-8431, SFF-8436, and SFF-8449 low-speed management interfaces, including a dedicated 100/400-kHz I2C interface to each port. Additional general-purpose pins are available to perform functions such as driving port status LEDs or controlling power switches. The LED drivers have convenience features such as programmable blinking and dimming. The interface to the host controller can operate on a separate supply voltage between 1.8 V and 3.3 V to support low-voltage I/Os.

For each port, the FPC202 has a total of four LED drivers, 12 general-purpose I/Os, and two downstream I2C busses. This expanded set of I/Os allows for control of additional components and features within a system. The general-purpose outputs can be used to drive additional LEDs if more than four are required per port.

The FPC202 can pre-fetch data from user-specified registers in each module, making the data readily accessible to the host through a fast I2C (up to 1 MHz) or SPI (up to 10 MHz) interface. In addition, the FPC202 can trigger an interrupt to the host whenever critical, user-configurable events occur associated with any of the ports under its control. This eliminates the need to continuously poll the modules.

6 Device Comparison Table

PART NUMBER	PORTS	LED DRIVERS PER PORT	GPIOs PER PORT	ACCESSIBLE DOWNSTREAM ADDRESSES
FPC202	2	4	12	All valid I2C addresses
FPC402	4	2	6	All valid I2C addresses
FPC401	4	2	6	MSA addresses: 0xA0, 0xA2

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *FPC202 Programmer's Guide*
- Texas Instruments, *FPC401 Evaluation Module (EVM) User's Guide*

Click here to request access to these documents in the FPC202 MySecure folder.

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.4 Trademarks

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7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
FPC202RHUR	ACTIVE	WQFN	RHU	56	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	FPC2	Samples
FPC202RHUT	ACTIVE	WQFN	RHU	56	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	FPC2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

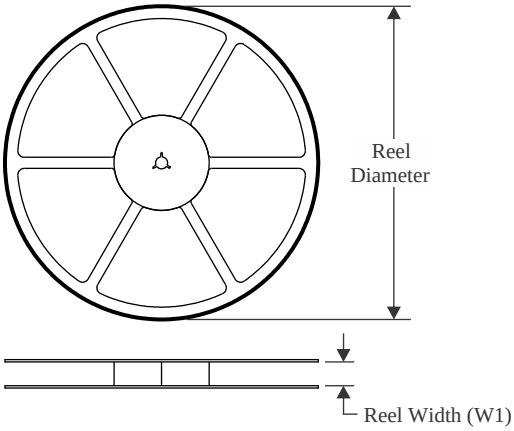
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

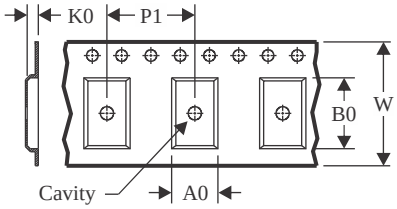
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

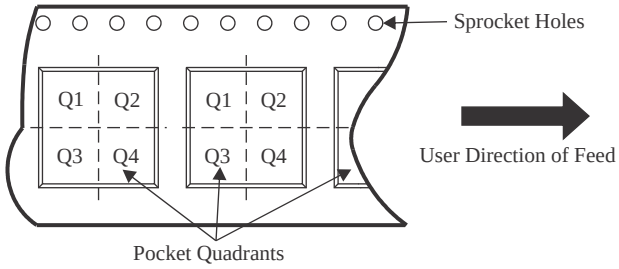


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

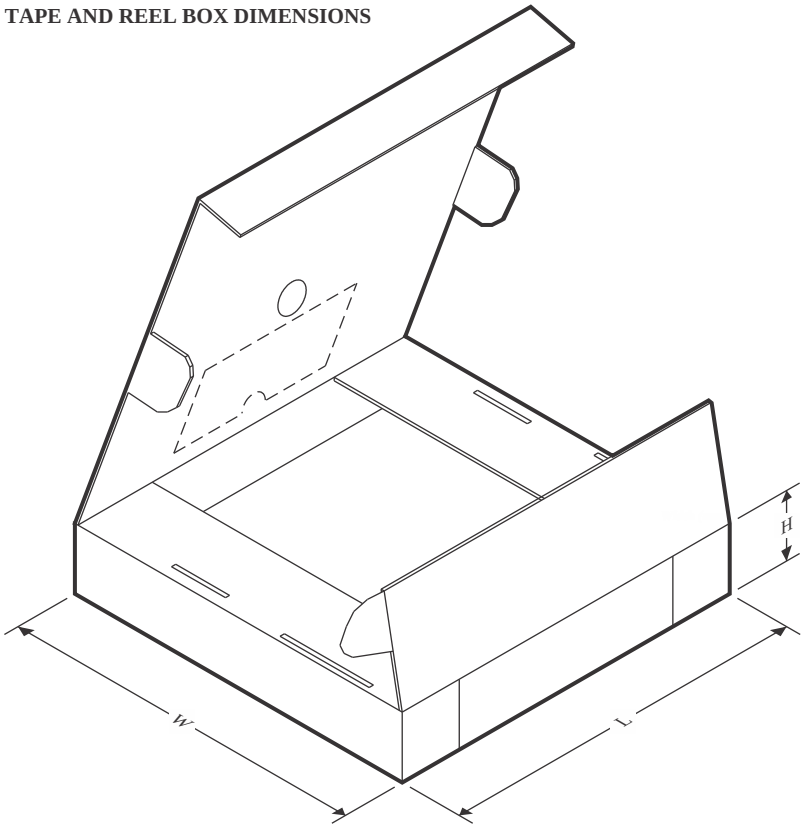
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
FPC202RHUR	WQFN	RHU	56	2000	330.0	24.4	5.3	11.3	1.0	8.0	24.0	Q1
FPC202RHUT	WQFN	RHU	56	250	178.0	24.4	5.3	11.3	1.0	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

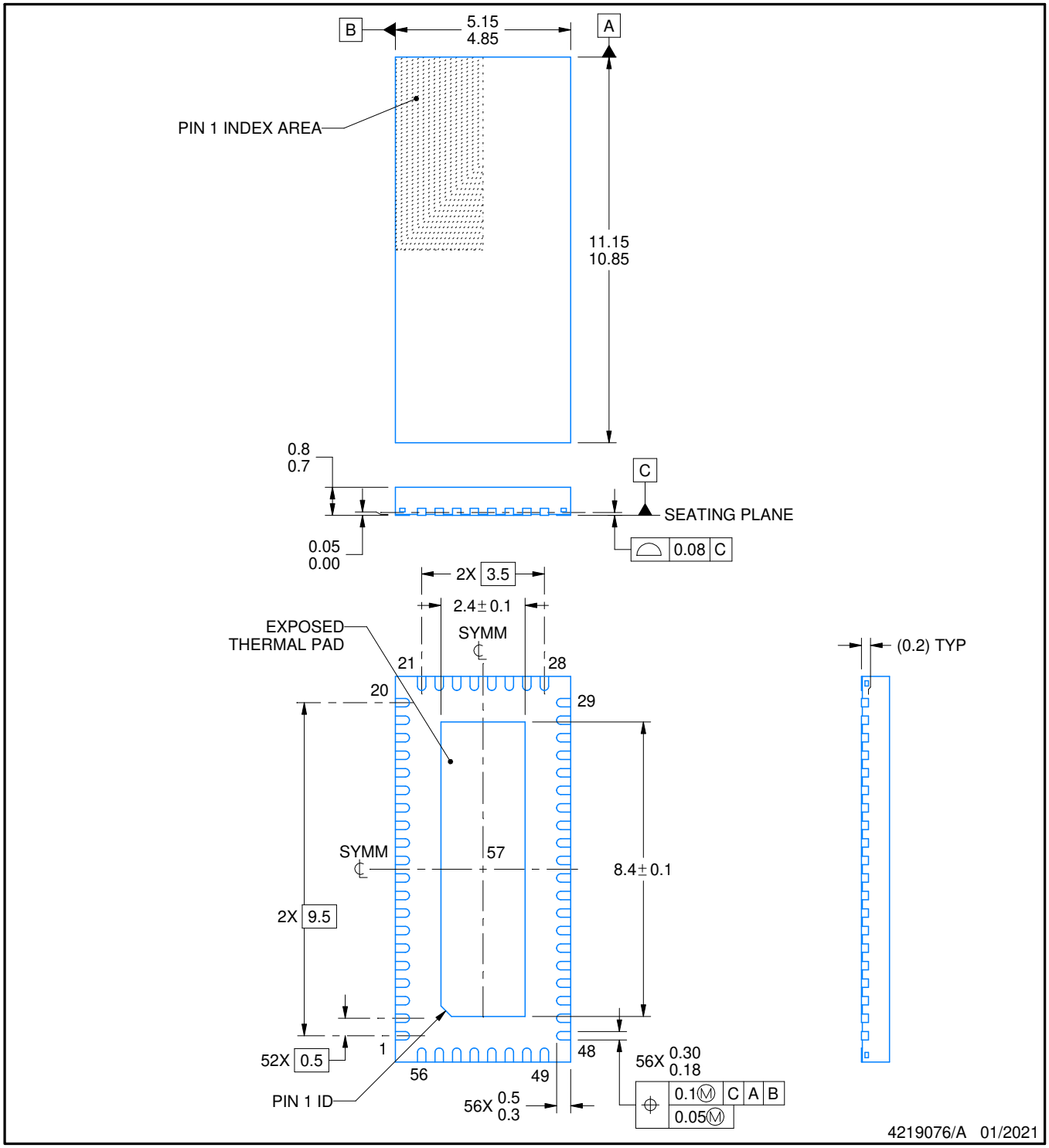
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
FPC202RHUR	WQFN	RHU	56	2000	367.0	367.0	45.0
FPC202RHUT	WQFN	RHU	56	250	213.0	191.0	55.0

PACKAGE OUTLINE

RHU0056A

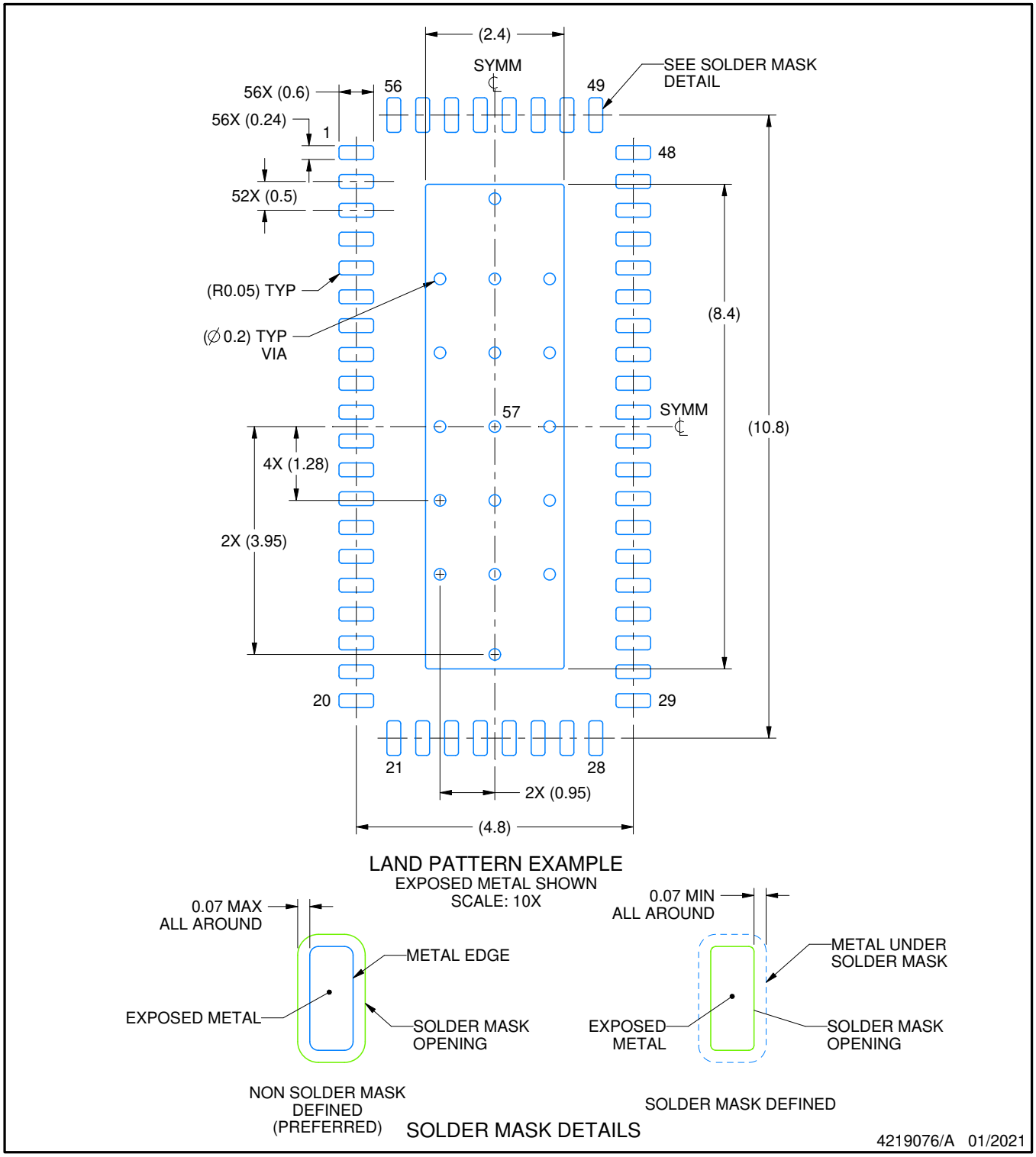
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



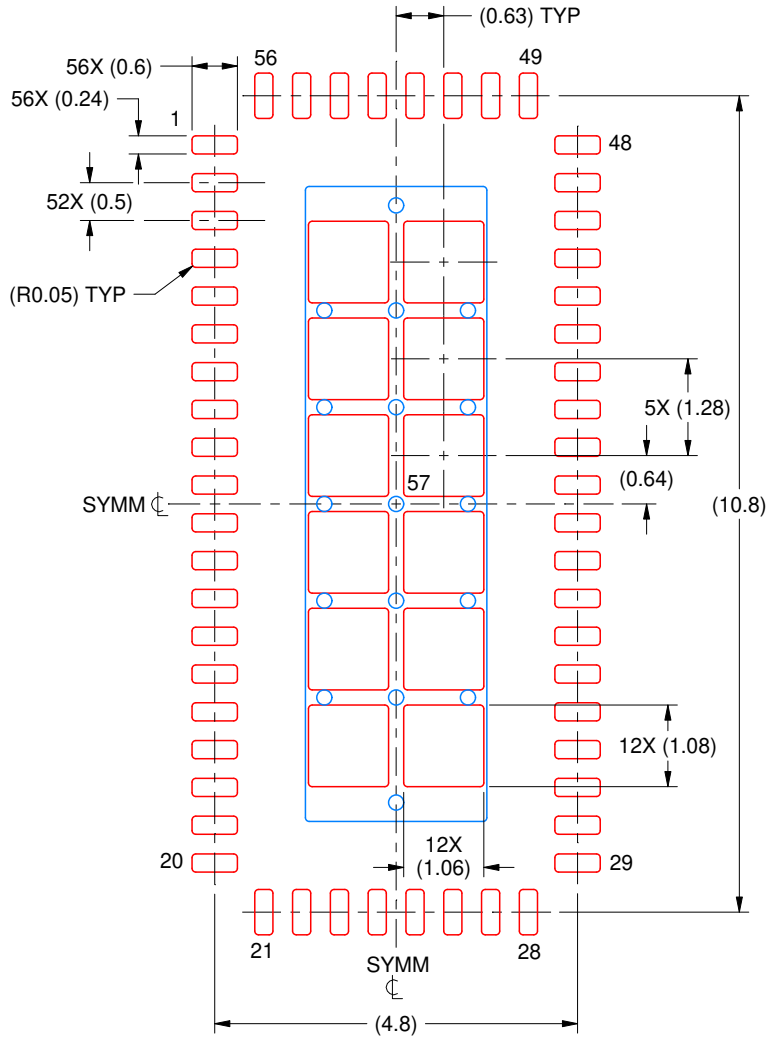
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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