EiceDRIVER™ 1EDN751x/1EDN851x

Single-channel low-side gate driver IC with 4 A source/8 A sink output stage

Description

The EiceDRIVER™ gate-driver IC family is offered in SOT23-5 and SOT23-6 with 5 pins and 6 pins respectively, as well as WSON-6 packages. The pinout meets de-facto industry standards. They are made to drive logic and normal level MOSFETs like OptiMOS™ and CoolMOS™, and GaN HEMT devices.

Product features

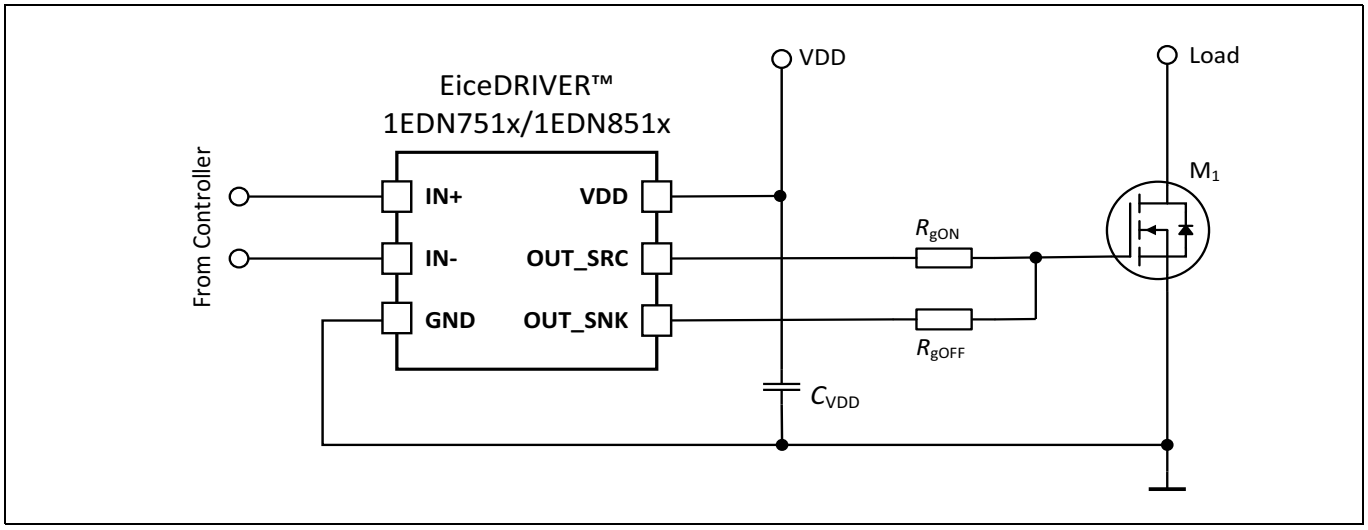
- 4 A source/8 A sink driving capability
- 19 ns typ. propagation delay
- +6/-4 ns propagation delay accuracy
- -10 V input voltage robustness
- 5 A reverse current robustness
- 4.2 V and 8 V UVLO options
- Industry standard package and pinout options:
  - → leaded SOT23-5 and SOT23-6
  - → leadless WSON-6
- Qualified for industrial applications according to JEDEC

Applications

- Switch-mode power supplies (SMPS)
- Power factor correction systems
- DC-DC power converters
- Low-voltage drives and power tools
- Industrial power supply (SMPS, UPS)
- EV off-board chargers
- Solar micro-inverters, solar optimizers

Available device configurations and typical application example

Part number	Package	UVLO ON/OFF	Output configuration	Output current
1EDN7511B	PG-SOT23-6	4.2 V/3.9 V	Separated source and sink	-8 A/+4 A
1EDN8511B		8.0 V/7.0 V	Separated source and sink	
1EDN7512B	PG-SOT23-5	4.2 V/3.9 V	Common OUT	
1EDN7512G	PG-WSON-6	4.2 V/3.9 V	Common OUT	



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1 Product versions

The EiceDRIVER™ 1EDN751x/1EDN851x is available in two different undervoltage lockout levels (4.2 V and 8.0 V) and three package versions.

1.1 Undervoltage lockout versions

Two undervoltage lockout versions of the product are available:

- EiceDRIVER™ 1EDN751x is designed to drive logic level MOSFETs (typ. $UVLO_{ON}$ = 4.2 V)
- EiceDRIVER™ 1EDN851x is designed to drive normal level and superjunction MOSFETs (typ. $UVLO_{ON}$ = 8.0 V)

Please refer to the functional description section for more details in **Chapter 4.5**

1.2 Package versions

The EiceDRIVER™ 1EDN family is available in three different package versions. The package type is identified by the last two characters in the product code:

- EiceDRIVER™ 1EDN7511B and 1EDN8511B are available in PG-SOT23-6-2 package
- EiceDRIVER™ 1EDN7512B is available in PG-SOT23-5-1 package
- EiceDRIVER™ 1EDN7512G is available in PG-WSON-6-1 leadless package

2 Pin configuration and description

2.1 Input configuration for PG-SOT23-6-2 package

The pin configuration for the PG-SOT23-6-2 package is shown in **Figure 1**. Pin description is given below in **Table 1**. For functional details, please read **Chapter 4**.

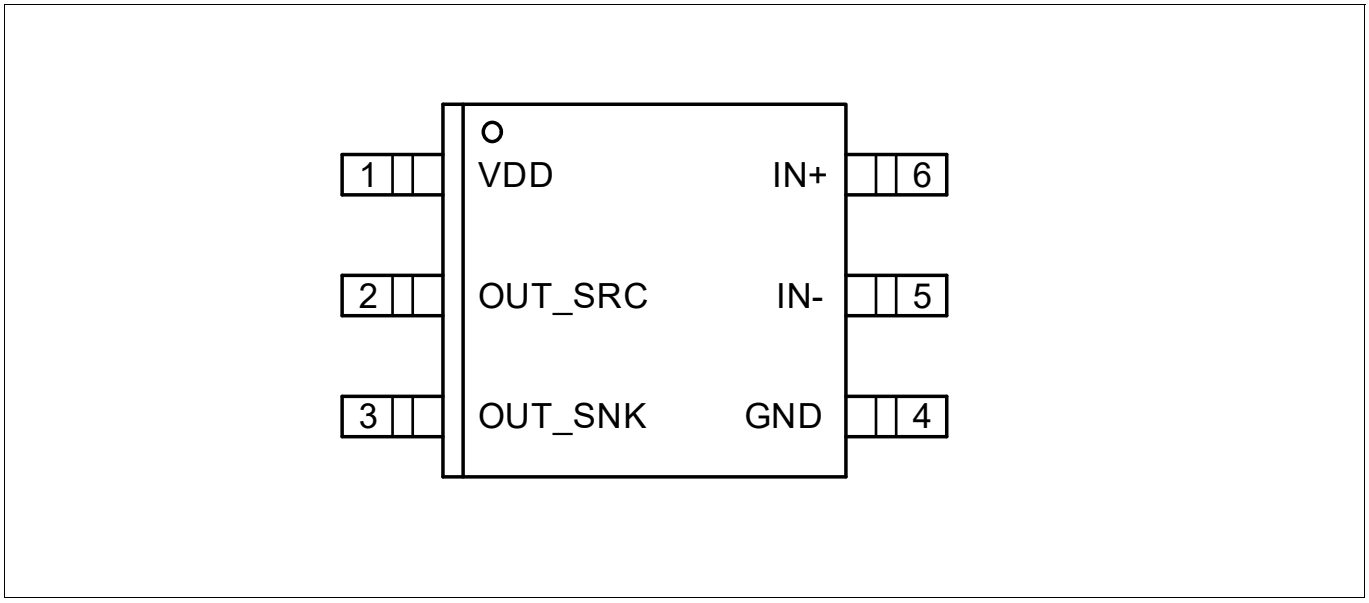

Figure 1 Pin configuration PG-SOT23-6-2 (top side view)

Table 1 Pin configuration

Pin Nr.	Symbol	Description
1	VDD	**Positive supply voltage** Operating range 4.5 V to 20 V
2	OUT_SRC	**Driver output source** Low-impedance output with source capability
3	OUT_SNK	**Driver output sink** Low-impedance output with sink capability
4	GND	**Ground**
5	IN-	**Inverting input** Logic Input; if IN- is high or left open, causes OUT low (See **Table 4**)
6	IN+	**Non-inverting input** Logic Input; if IN+ is low or left open causes OUT low (See **Table 4**)

2.2 Input configuration for PG-SOT23-5-1 package

The pin configuration for the PG-SOT23-5-1 package is shown in **Figure 2**. Pin description is given below in **Table 2**. For functional details, please read **Chapter 4**.

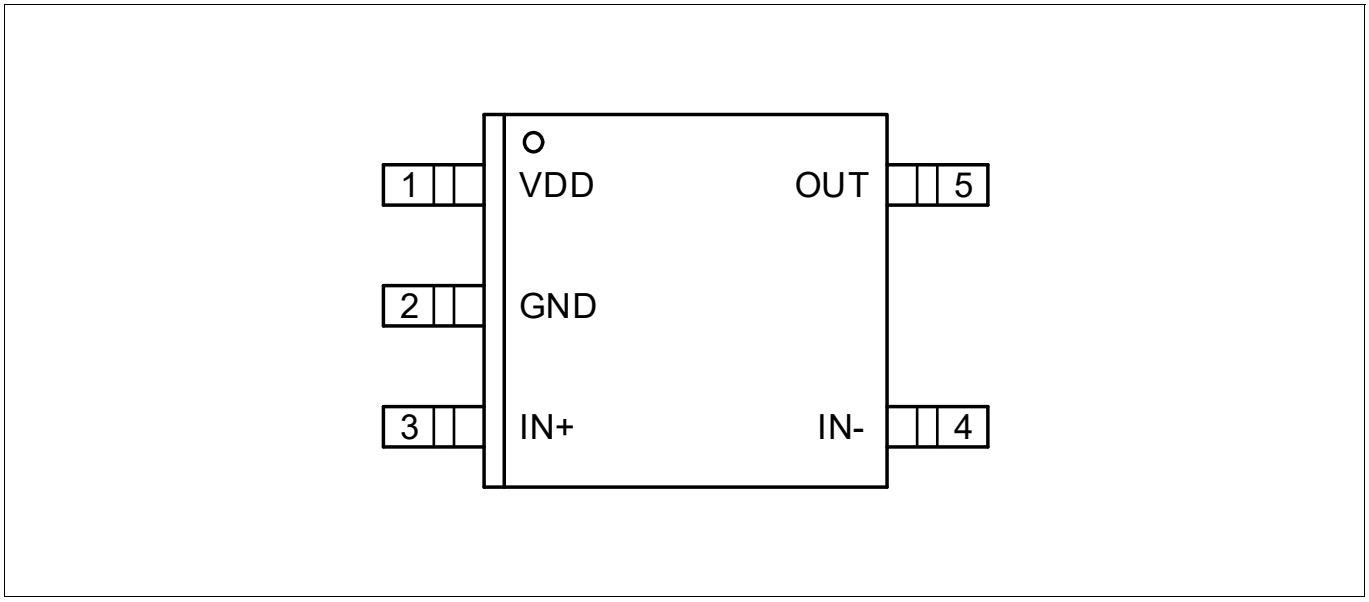

Figure 2 Pin configuration PG-SOT23-5-1 (top side view)

Table 2 Pin configuration

Pin Nr.	Symbol	Description
1	VDD	**Positive supply voltage** Operating range 4.5 V to 20 V
2	GND	**Ground**
3	IN+	**Non-inverting input** Logic Input; if IN+ is low or left open causes OUT low (See **Table 4**)
4	IN-	**Inverting input** Logic Input; if IN- is high or left open, causes OUT low (See **Table 4**)
5	OUT	**Driver output** Low-impedance output and sink capability

2.3 Input configuration for PG-WSON-6-1 package

The pin configuration for the PG-WSON-6-1 package is shown in **Figure 3**. Pin description is given below in **Table 3**. For functional details, please read **Chapter 4**.

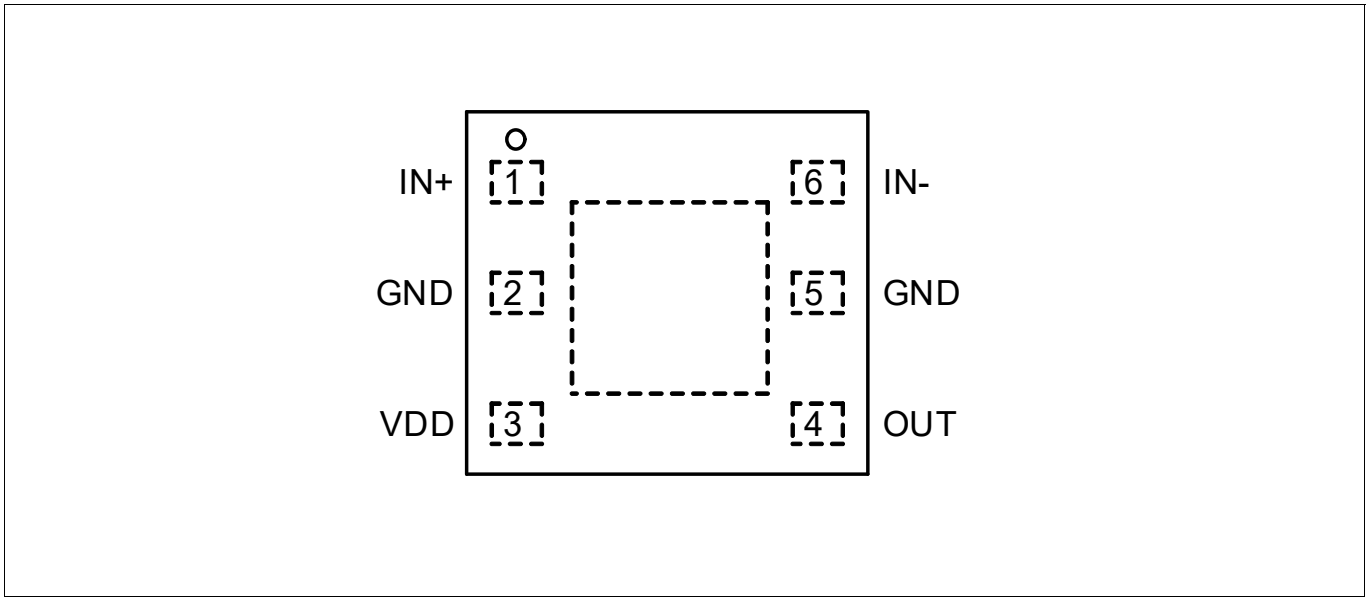

Figure 3 Pin configuration PG-WSON-6-1 (top side view)

Table 3 Pin configuration

Pin Nr.	Symbol	Description
1	IN+	**Non-inverting input** Logic Input; if IN+ is low or left open causes OUT low (See **Table 4**)
2; 5	GND	**Ground**
3	VDD	**Positive supply voltage** Operating range 4.5 V to 20 V
4	OUT	**Driver output** Low-impedance output with source and sink capability
6	IN-	**Inverting input** Logic Input; if IN- is high or left open, causes OUT low (See **Table 4**)

Note: Exposed pad of PG-WSON-6-1 package must be connected to GND pin

3 Block Diagram

A simplified functional block diagram of the PG-SOT23-6-2 package with separated sink and source outputs is given in **Figure 4**.

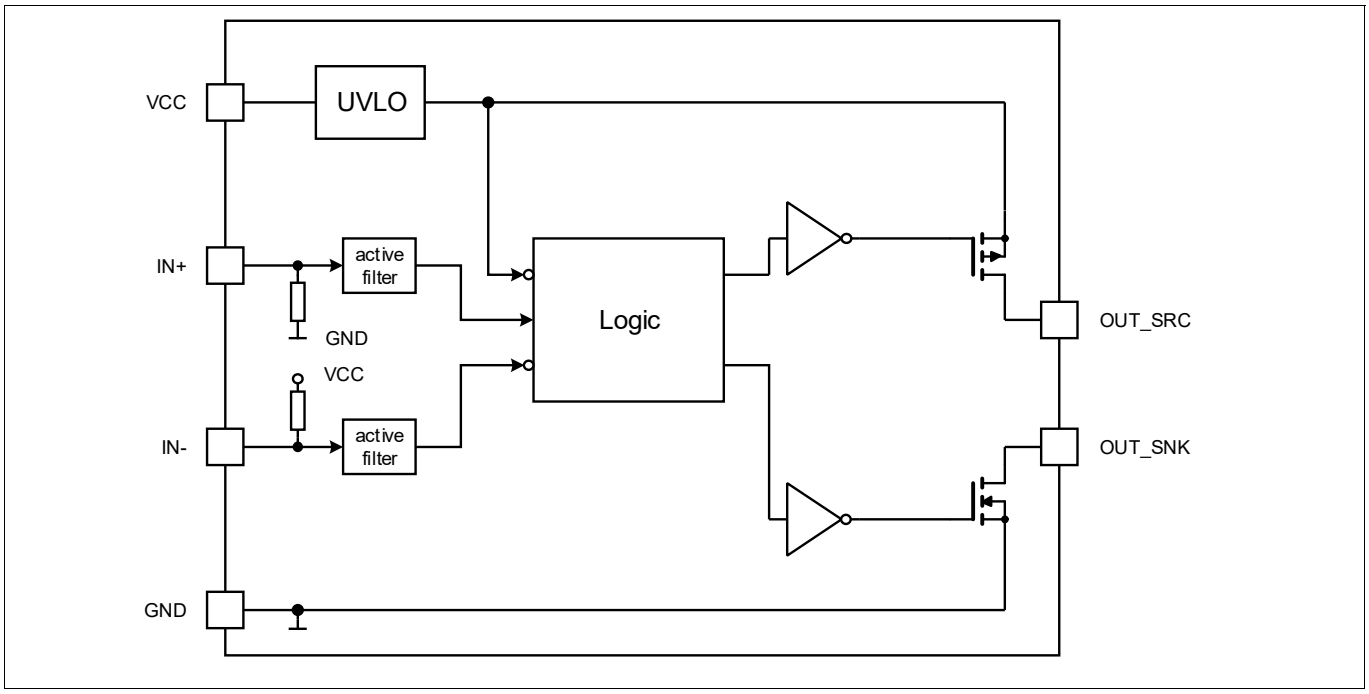

Figure 4 Simplified block diagram of EiceDRIVER™ 1EDN7511B and 1EDN8511B

A simplified functional block diagram of the PG-SOT23-5-1 and PG-WSON-6-1 with common output is depicted in **Figure 5**.

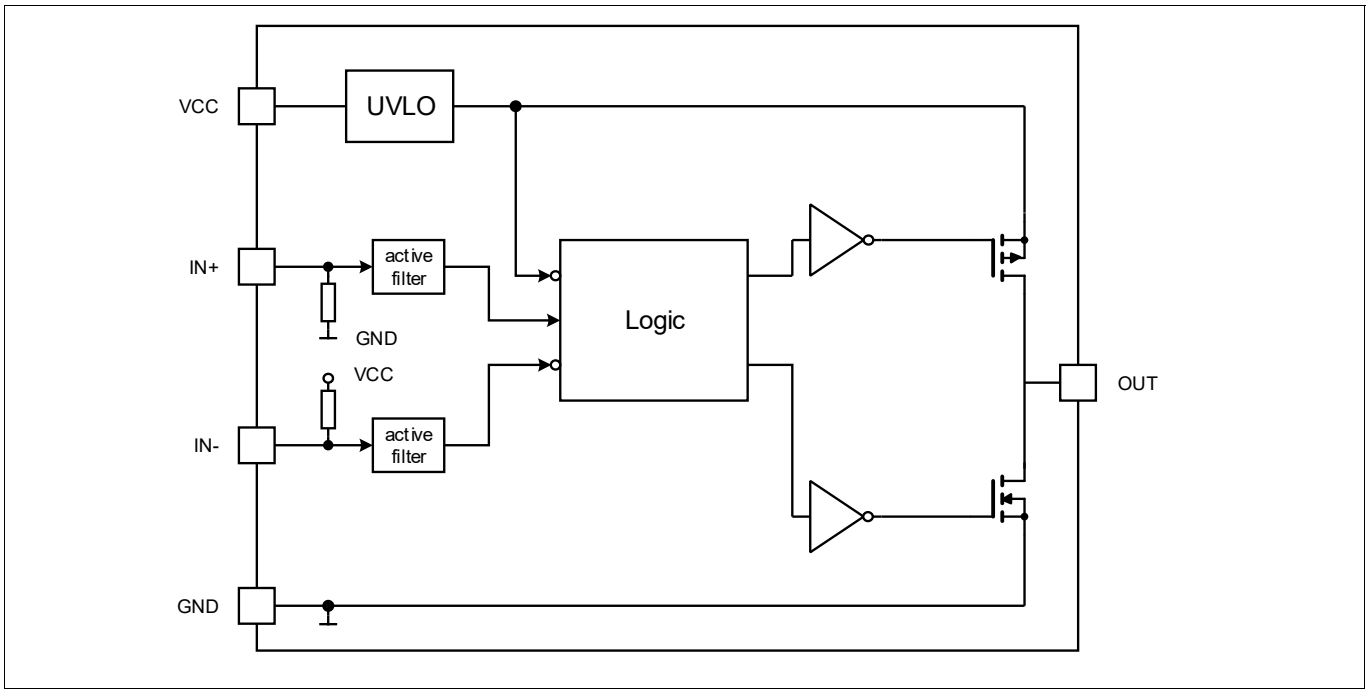

Figure 5 Simplified block diagram of EiceDRIVER™ 1EDN7512B and 1EDN7512G

4 Functional description

4.1 Introduction

The 1EDN751x/1EDN851x is a fast single-channel driver for low-side switches. Rail-to-rail output stages with very low output impedance and high current capability are chosen to ensure highest flexibility and cover a high variety of applications.

The focus on robustness at the input and output side gives this device an additional safety margin in critical abnormal situations. An extended negative voltage range (-10 V) protects input pins against ground shifts. No current flows over the ESD structure in the IC during a negative input level. Output is robust against reverse current (5 A). The interaction with the power MOSFET, even reverse reflected power will be handled by the strong internal output stage.

Inputs are compatible with LV-TTL signal levels. The threshold voltages with a typical hysteresis of 1.1 V are kept constant over the supply voltage range.

Since the 1EDN751x/1EDN851x aims particularly at fast-switching applications, signal delays and rise/fall times have been minimized to support low switching losses in the MOSFET.

4.2 Supply voltage

The maximum supply voltage is 20 V. This high voltage can be valuable in order to exploit the full current capability of 1EDN751x/1EDN851x when driving very large MOSFETs. The minimum operating supply voltage is set by the undervoltage lockout function to a typical default value of 4.2 V or of 8 V. This undervoltage lockout function protects power MOSFETs from running into linear mode with subsequent high power dissipation.

4.3 Driver inputs

The non-inverting input is internally pulled down to a logic low voltage. The inverting input is internally pulled up to a logic high voltage. This prevents a switch-on event during power-up and a not-driven input condition.

All inputs are compatible with LV-TTL levels and provide a hysteresis of typically 1.1 V. This hysteresis is independent of the supply voltage.

All input pins have a negative extended voltage range (-10 V). This prevents cross-current over signal wires when ground shifts between the signal source (controller) and driver input.

4.4 Driver outputs

The rail-to-rail output stage realized with complementary MOS transistors is able to provide typical 4 A sourcing and 8 A sinking current. This asymmetrical push-pull stage enables a perfect “brake before make” (turn-off is faster than turn-on) condition, which is needed in half-bridge power MOSFET stages.

This driver output stage has a shoot-through protection and current limiting behavior.

The output impedance is very low with a typical value below 0.85 Ω for the sourcing p-channel MOS and 0.35 Ω for the sinking n-channel MOS transistor. The use of a p-channel sourcing transistor is crucial for achieving true rail-to-rail behavior and avoiding a source follower’s voltage drop.

The gate drive output is actively held low in case of floating inputs, during startup, or power down triggered by the UVLO protection. In any situation (startup, UVLO, or shtudown) the output is held under defined conditions. Output states for EiceDRIVER™ 1EDN7511B and 1EDN8511B are listed in **Table 4**.

Table 4 Truth table

IN+	IN-	OUT_SRC	OUT_SNK
L	L	OPEN	L
L	H	OPEN	L
H	L	H	OPEN
H	H	OPEN	L

4.5 Undervoltage lockout (UVLO)

The undervoltage lockout function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO threshold voltage. Thus it can be guaranteed, that the switch transistor is not switched on if the driving voltage is too low to completely switch it on, thereby avoiding excessive power dissipation.

The UVLO level is set to a typical value of 4.2 V/8 V (with hysteresis). The 4.2 V UVLO threshold is typically used for logic level MOSFETs. For normal level and superjunction MOSFETS, a UVLO voltage of typically 8 V is available.

5 Electrical characteristics

The absolute maximum ratings are listed in **Table 5**. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 Absolute maximum ratings

Table 5 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Positive supply voltage	V_{VDD}	-0.3	–	22	V	–
Voltage at pins IN+, IN-	V_{IN}	-10	–	22	V	–
Voltage at pins OUT, OUT_SRC, OUT_SNK	V_{OUT}	-0.3	–	V_{VDD}+0.3	V	Note[1]
		-2	–	V_{VDD}+2	V	Repetitive pulse < 200ns[2]
Reverse current peak at pins OUT, OUT_SRC/OUT_SNK	I_{SNK_rev} I_{SRC_rev}	–	–	-5 5	A_{pk}	< 500 ns
Junction temperature	T_J	-40	–	150	°C	–
Storage temperature	T_S	-55	–	150	°C	–
ESD capability	V_{ESD}	–	–	1.5	kV	Charged Device Mode (CDM) [3]
ESD capability	V_{ESD}	–	–	2.5	kV	Human Body Model (HBM) [4]

1) Voltage spikes resulting from reverse current peaks are allowed.
2) Values are verified by characterization on bench.
3) According to ESD-CDM: ANSI/ESDA/JEDEC JS-002
4) According to ESD-HBM: ANSI/ ESDA/JEDEC JS-001

5.2 Thermal characteristics

Table 6 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
PG-SOT23-6-2, T_{amb}=25°C						
Thermal resistance junction-ambient [1]	R_{thJA25}	–	170	–	K/W	–
Thermal resistance junction-case (top) [2]	R_{thJC25}	–	81	–	K/W	–
Thermal resistance junction-board [3]	R_{thJB25}	–	52	–	K/W	–
Characterization parameter junction-case (top)[4]	Ψ_{thJC25}	–	14	–	K/W	–
Characterization parameter junction-board [5]	Ψ_{thJB25}	–	51	–	K/W	–

Table 6 Thermal characteristics (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
PG-SOT23-5-1, T_{amb}=25°C						
Thermal resistance junction-ambient [1]	R_{thJA25}	–	180	–	K/W	–
Thermal resistance junction-case (top) [2]	R_{thJC25}	–	76	–	K/W	–
Thermal resistance junction-board [3]	R_{thJB25}	–	60	–	K/W	–
Thermal resistance junction-bottom (heat sink)[6]	R_{thJB25}	–	16	–	K/W	–
Characterization parameter junction-case (top) [4]	Ψ_{thJB25}	–	14	–	K/W	–
Characterization parameter junction-board [5]	Ψ_{thJB25}	–	52	–	K/W	–
PG-WSON-6-1, T_{amb}=25°C						
Thermal resistance junction-ambient [1]	R_{thJA25}	–	63	–	K/W	–
Thermal resistance junction-case (top) [2]	R_{thJP25}	–	83	–	K/W	–
Thermal resistance junction-board [3]	R_{thJB25}	–	16	–	K/W	–
Thermal resistance junction-bottom (heat sink) [6]	R_{thJB25}	–	16	–	K/W	–
Characterization parameter junction-top [4]	Ψ_{thJC25}	–	9	–	K/W	–
Characterization parameter junction-board [5]	Ψ_{thJB25}	–	15	–	K/W	–

1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

4) The characterization parameter junction-top, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining Rth, using a procedure described in JESD51-2a (sections 6 and 7).

5) The characterization parameter junction-board, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining Rth, using a procedure described in JESD51-2a (sections 6 and 7).

6) The junction-to-bottom thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

5.3 Operating range

Table 7 Operating range

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{VDD}	4.5	–	20	V	Min defined by UVLO
Logic input voltage	V_{IN}	-5	–	20	V	–
Junction temperature	T_J	-40	–	150	°C	1)

1) Continuous operation above 125 °C may reduce life time.

5.4 Electrical characteristics

Unless otherwise noted, min./max. values of characteristics are the lower and upper limits respectively. They are valid within the full operating range. The supply voltage is V_{VDD}= 12 V. Typical values are given at T_J=25°C.

Table 8 Power supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VDD quiescent current	I_{VDDqu1}	–	0.4	–	mA	OUT = high, V_{VDD}= 12 V
VDD quiescent current	I_{VDDqu2}	–	0.37	–	mA	OUT = low, V_{VDD}= 12 V

Table 9 Undervoltage lockout for logic level MOSFET

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage lockout (UVLO) turn on threshold	$UVLO_{on}$	3.9	4.2	4.5	V	–
Undervoltage lockout (UVLO) turn off threshold	$UVLO_{off}$	3.6	3.9	4.2	V	–
UVLO threshold hysteresis	$UVLO_{hys}$	–	0.3	–	V	–

Table 10 Undervoltage lockout for standard and superjunction MOSFET version

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage lockout (UVLO) turn on threshold	$UVLO_{on}$	7.4	8.0	8.6	V	–
Undervoltage lockout (UVLO) turn off threshold	$UVLO_{off}$	6.5	7.0	7.5	V	–
UVLO threshold hysteresis	$UVLO_{hys}$	–	1.0	–	V	–

Table 11 Logic inputs IN+, IN-

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	V_{INH}	1.9	2.1	2.3	V	–
Input voltage threshold for transition HL	V_{INL}	0.8	1.0	1.2	V	–
Input pull up resistor[1)]	$R_{IN\,H}$	–	400	–	kΩ	–
Input pull down resistor[2)]	$R_{IN\,L}$	–	100	–	kΩ	–

1) Inputs with initial high logic level
2) Inputs with initial low logic level

Table 12 Static output characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level (sourcing) output resistance	R_{on_SRC}	0.42	0.85	1.46	Ω	I_{SRC} = 50 mA
High level (sourcing) output current	I_{SRC_peak}	–	4.0	[1)]	A	–
Low level (sinking) output resistance	R_{on_SNK}	0.18	0.35	0.64	Ω	I_{SNK} = 50 mA
Low level (sinking) output current	I_{SNK_Peak}	–	-8.0	[2)]	A	–

1) Active limited by design at approx. 5.2 A_{pk}, parameter is not subject to production test - verified by design / characterization, max. power dissipation must be observed
2) Active limited by design at approx. -10.4 A_{pk}, parameter is not subject to production test - verified by design / characterization, max. power dissipation must be observed

Table 13 Dynamic characteristics (see Figure 6, Figure 7, Figure 8)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input to output propagation delay	T_{PDON}	15	19	25	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Input to output propagation delay	T_{PDOFF}	15	19	25	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Rise time	T_{RISE}	–	6.5	11[1)]	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Fall time	T_{FAll}	–	4.5	9[1)]	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Minimum input pulse width that changes output state	T_{PW}	–	6	10	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V

1) Parameter verified by design, not 100% tested in production.

6 Timing diagrams

Figure 6 shows the definition of rise, fall and delay times for the inputs. This is also valid for the inverted control.

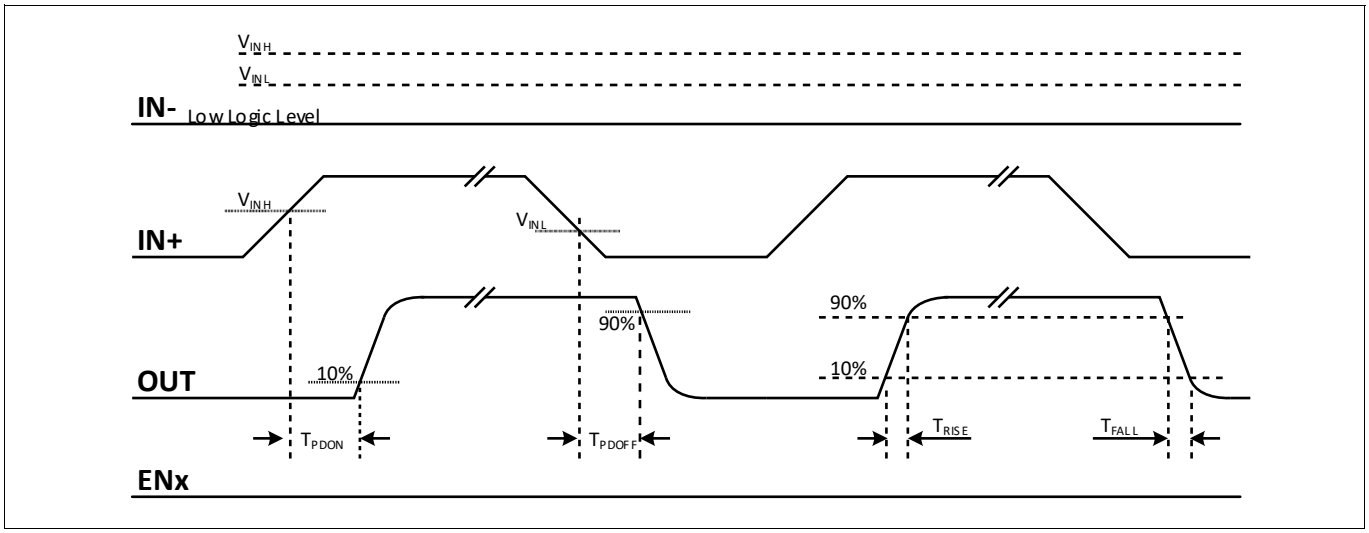

Figure 6 Propagation delay, rise and fall time, non-inverted

Figure 7 illustrates the undervoltage lockout function.

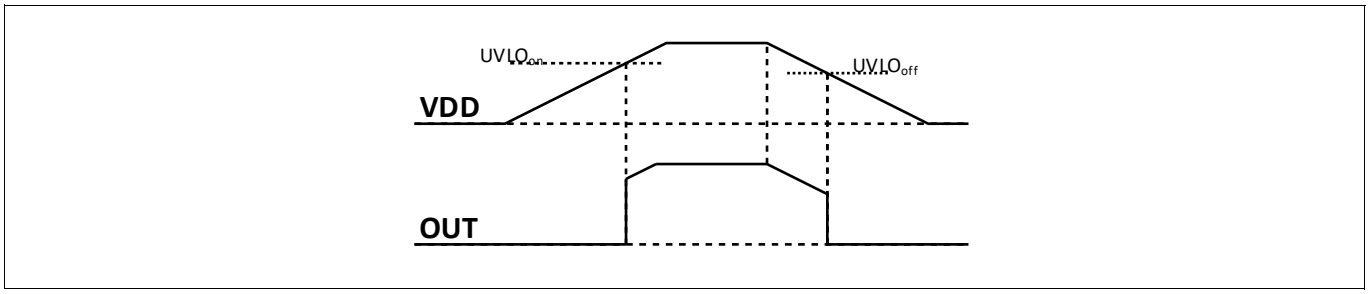

Figure 7 UVLO behaviour, input INx drives OUT normally high

Figure 8 illustrates the minimum input pulse width that changes output state.

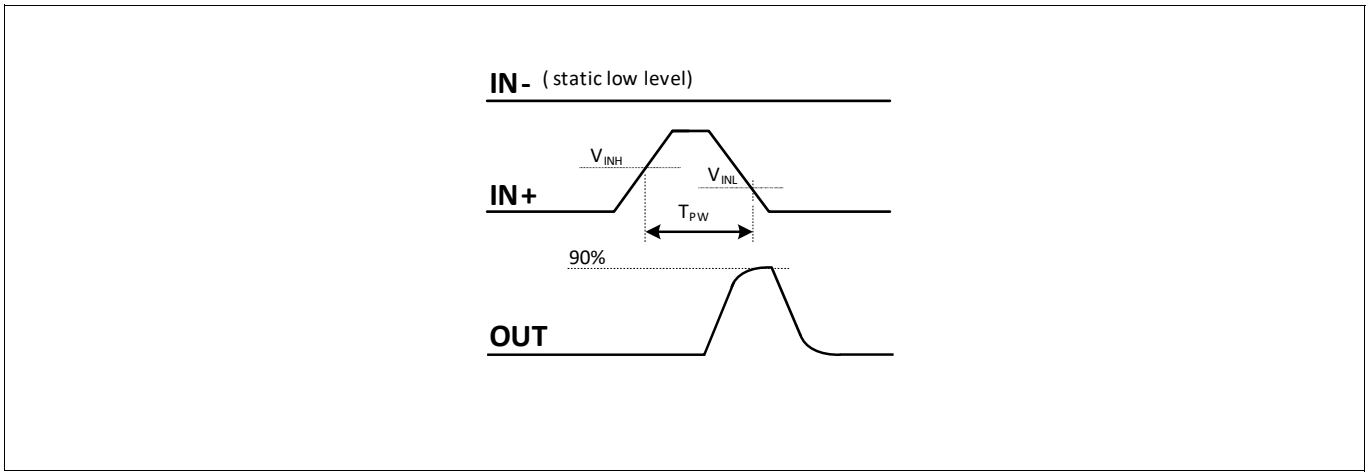

Figure 8 Minimum input pulse width that changes output state

7 Typical characteristics

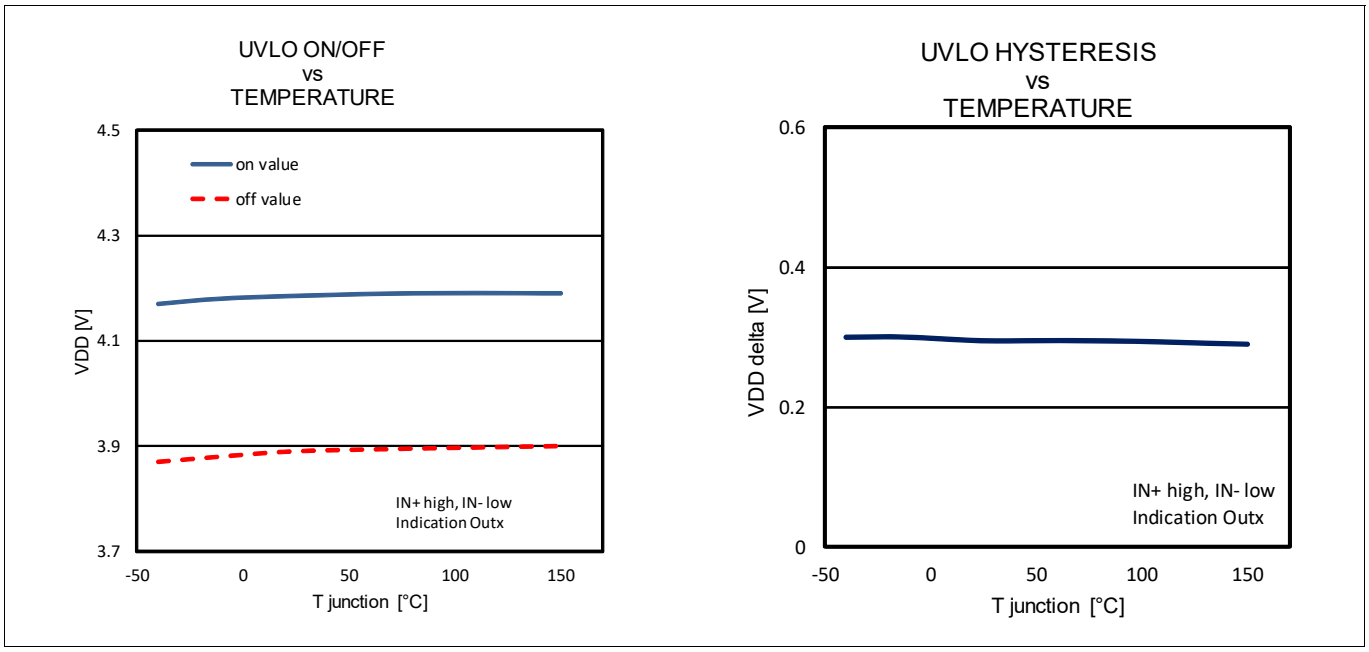

Figure 9 Undervoltage lockout 1EDN751x (4.2 V)

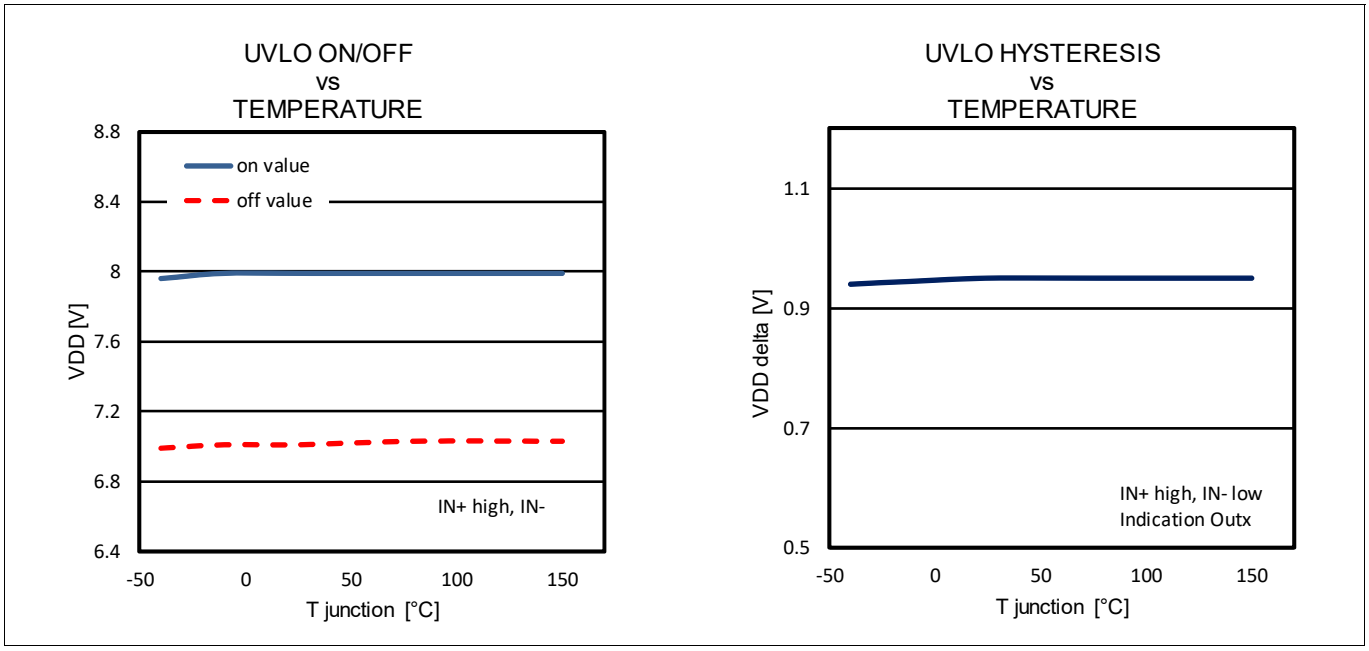

Figure 10 Undervoltage lockout 1EDN851x (8 V)

Typical characteristics

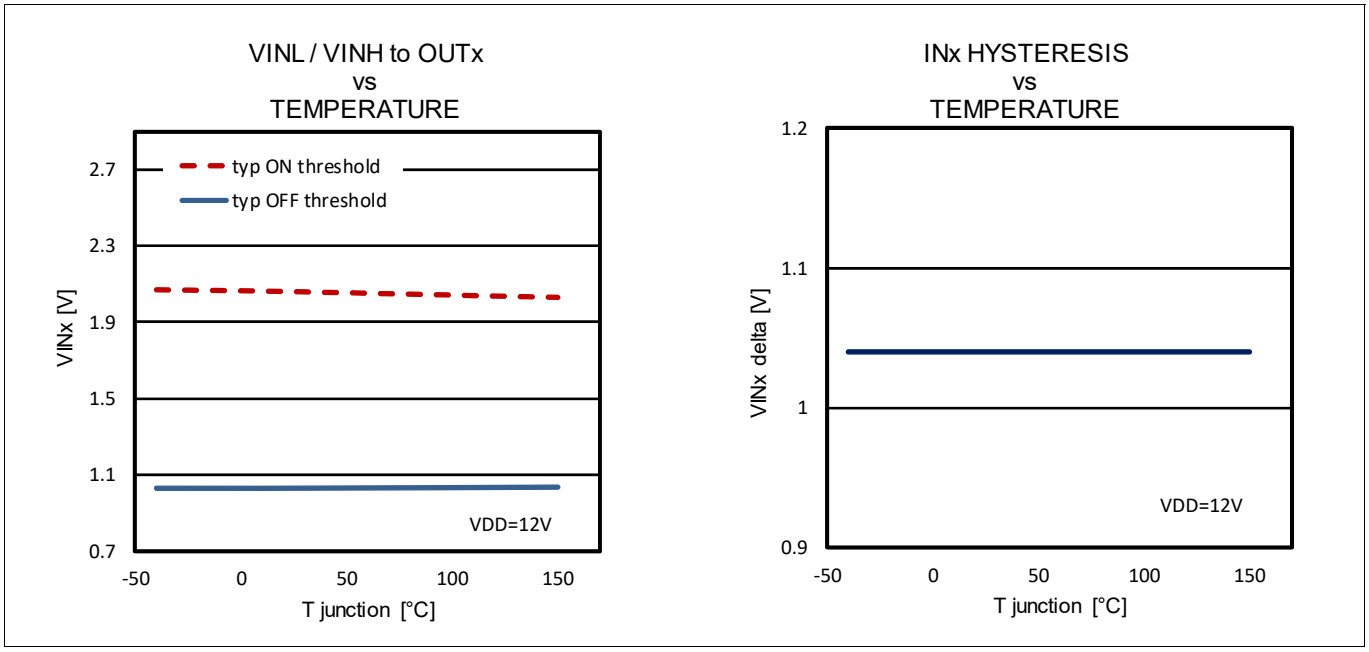

Figure 11 Input (INx) characteristic

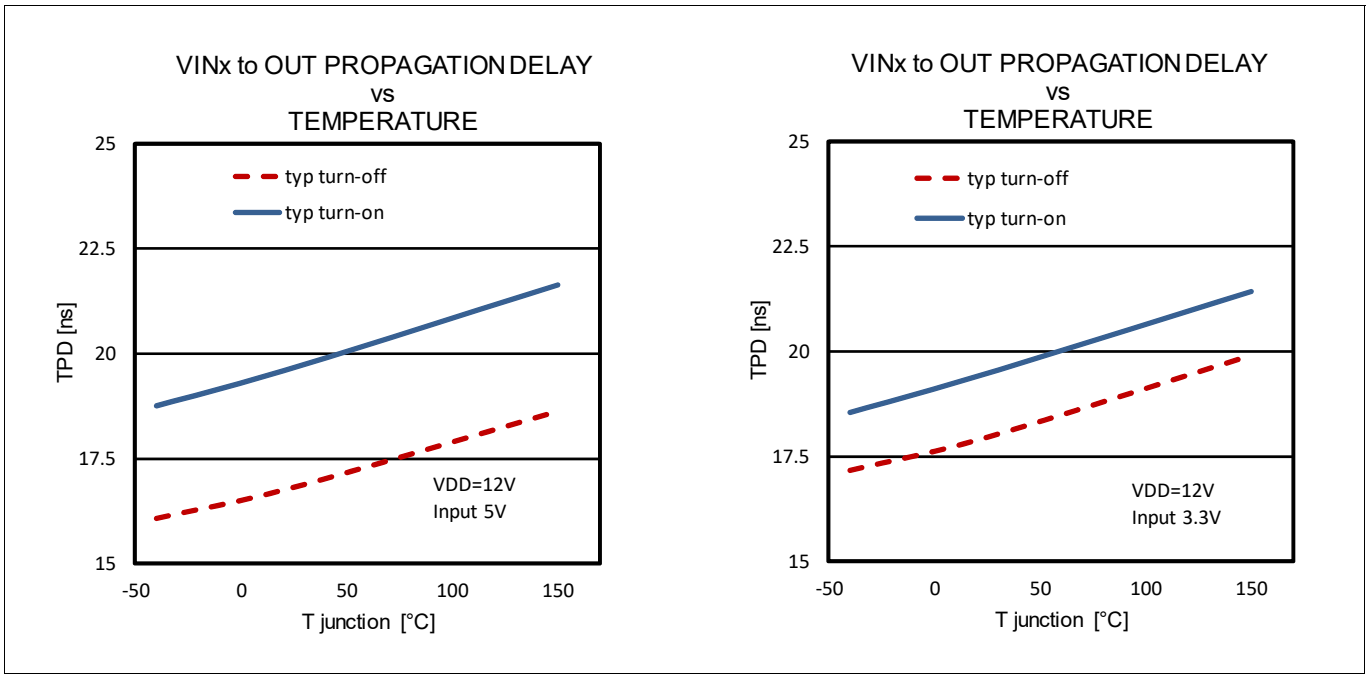

Figure 12 Propagation delay (INx) on different input logic levels (See Figure 6)

Typical characteristics

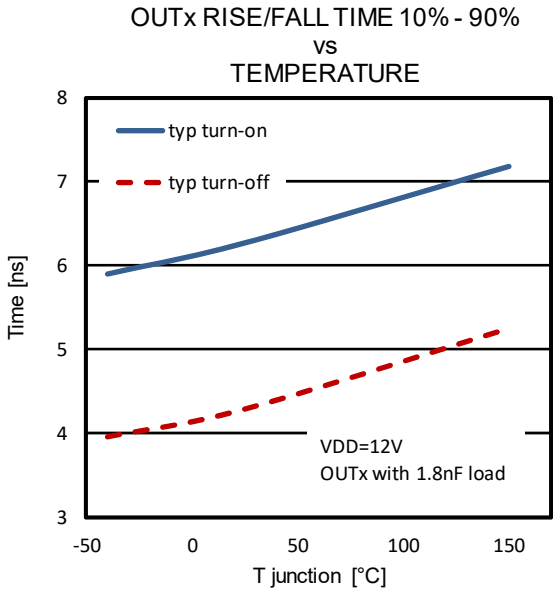

Figure 13 Rise/fall times with load on output

Typical characteristics

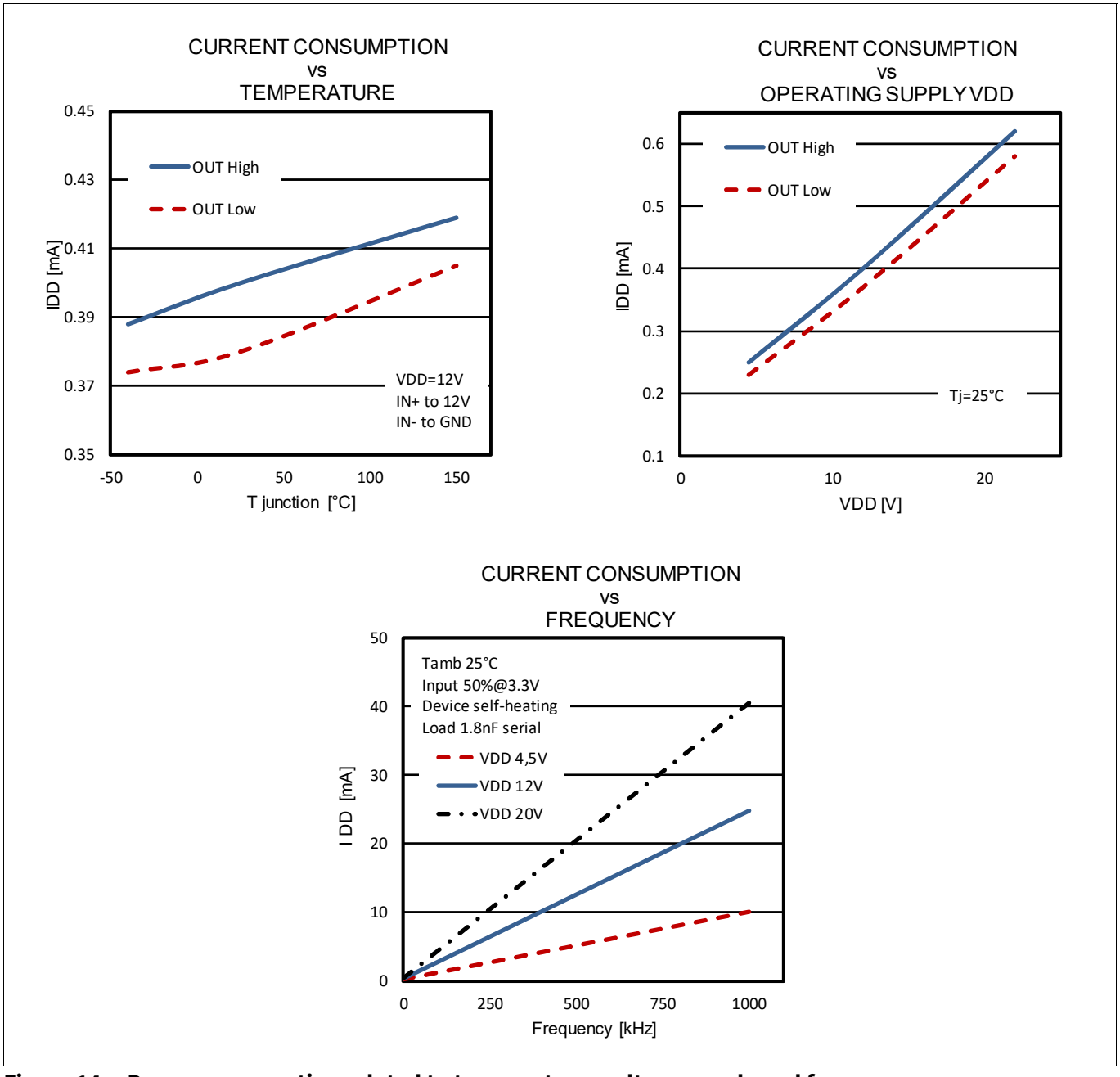

Figure 14 Power consumption related to temperature, voltage supply and frequency

Typical characteristics

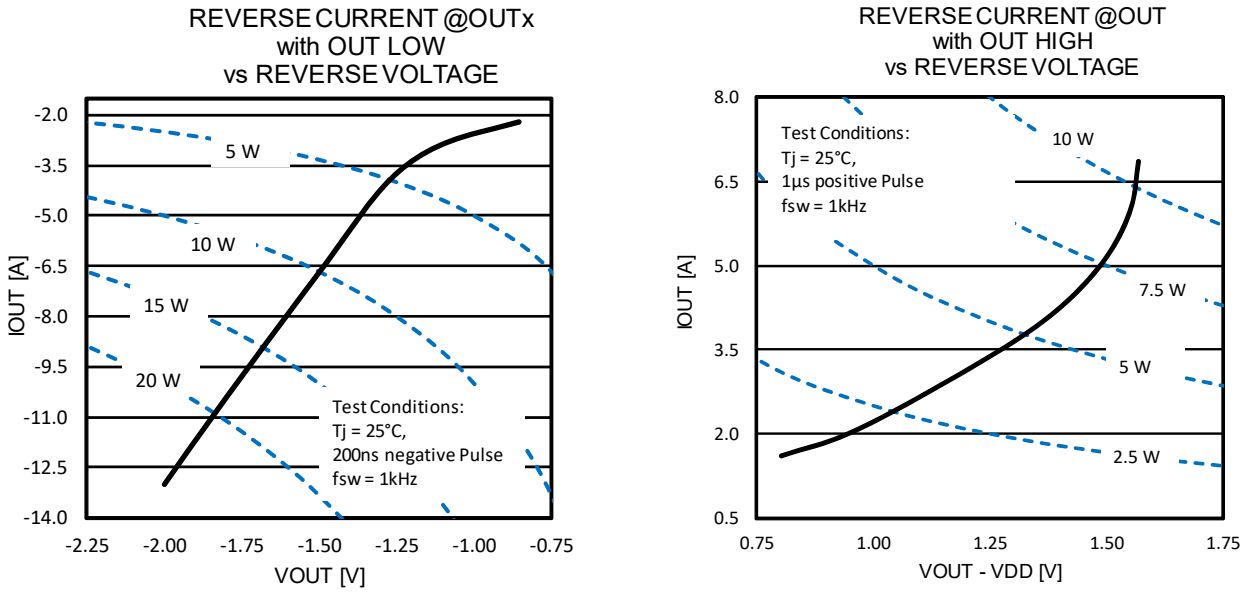

Figure 15 Output OUTx with reverse current and resulting power dissipation

8 Package outlines

Note: For further information on package types, recommendation for board assembly, please go to: ***Infineon packages****.*

8.1 Device numbers and markings

Table 14 Device numbers and markings

Part number	Orderable part number (OPN)	Device marking
1EDN7511B	1EDN7511BXUSA1	71
1EDN8511B	1EDN8511BXUSA1	81
1EDN7512B	1EDN7512BXTSA1	72
1EDN7512G	1EDN7512GXTMA1	1N7512 AG_XXX HYYWW

8.2 PG-SOT23-6-2

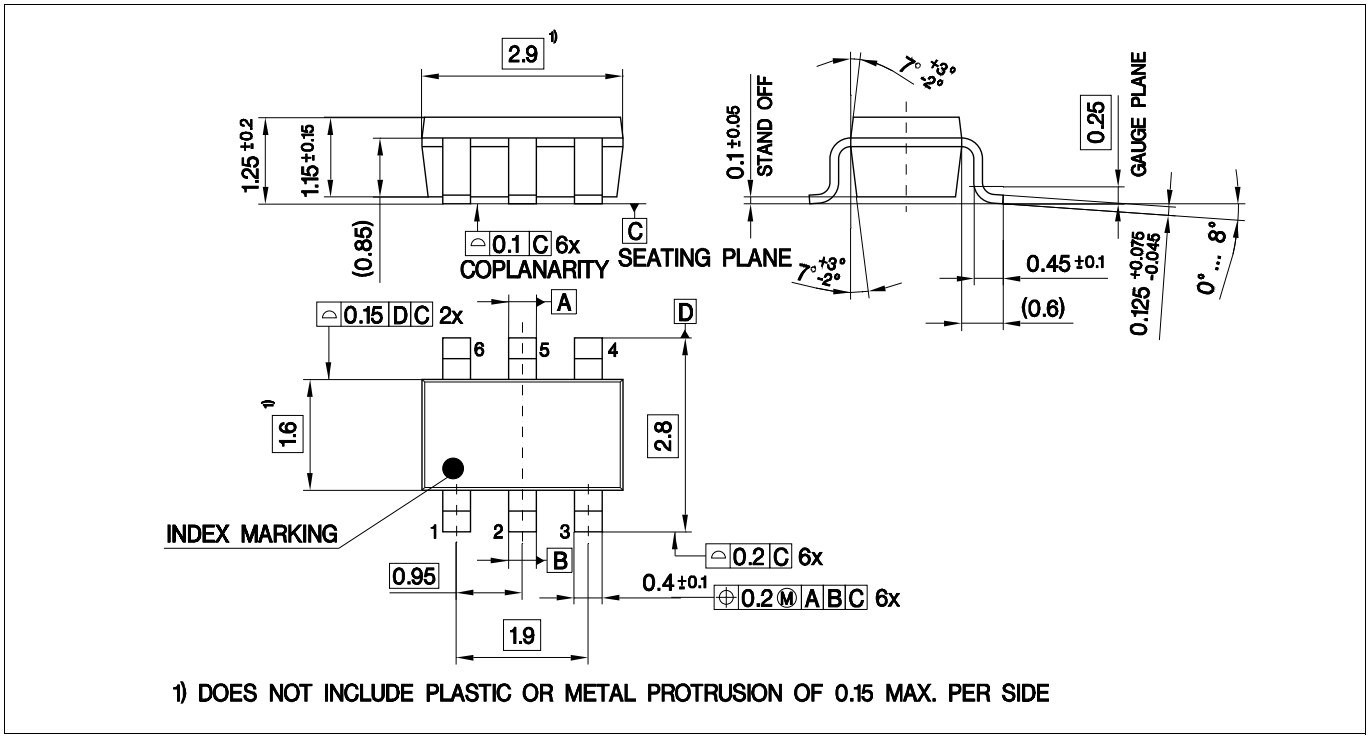

Figure 16 PG-SOT23-6-2 outline dimensions

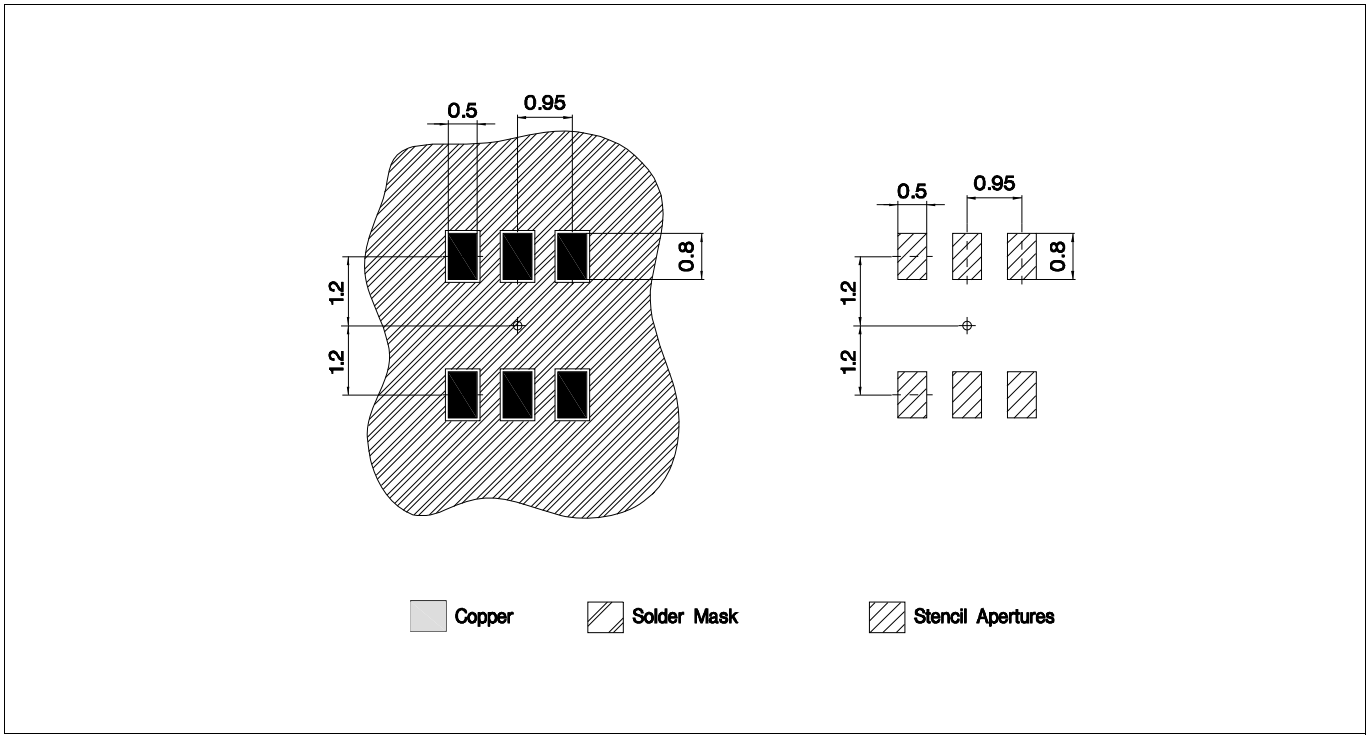

Figure 17 PG-SOT23-6-2 footprint dimensions

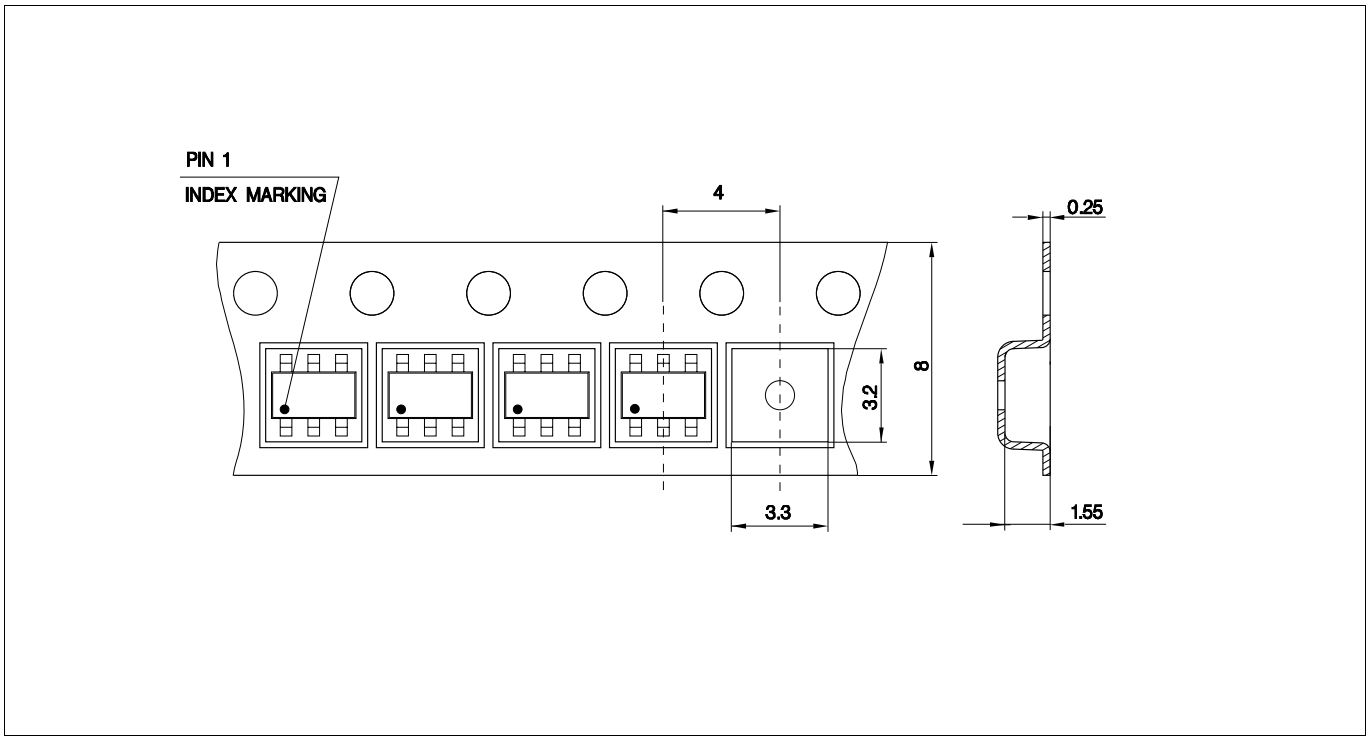

Figure 18 PG-SOT23-6-2 packaging dimensions

8.3 PG-SOT23-5-1

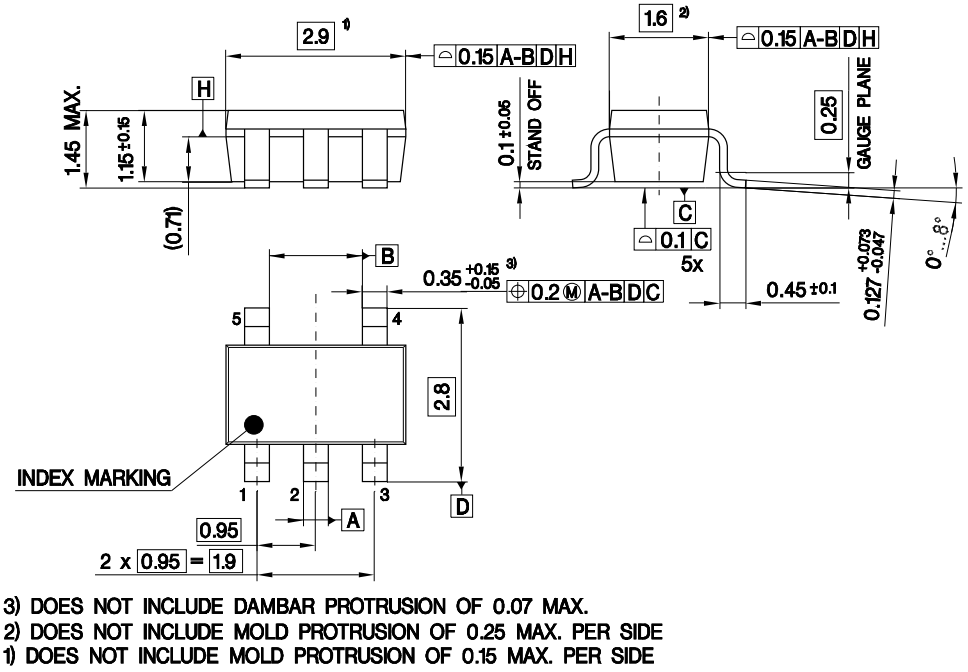

Figure 19 PG-SOT23-5-1 outline dimensions

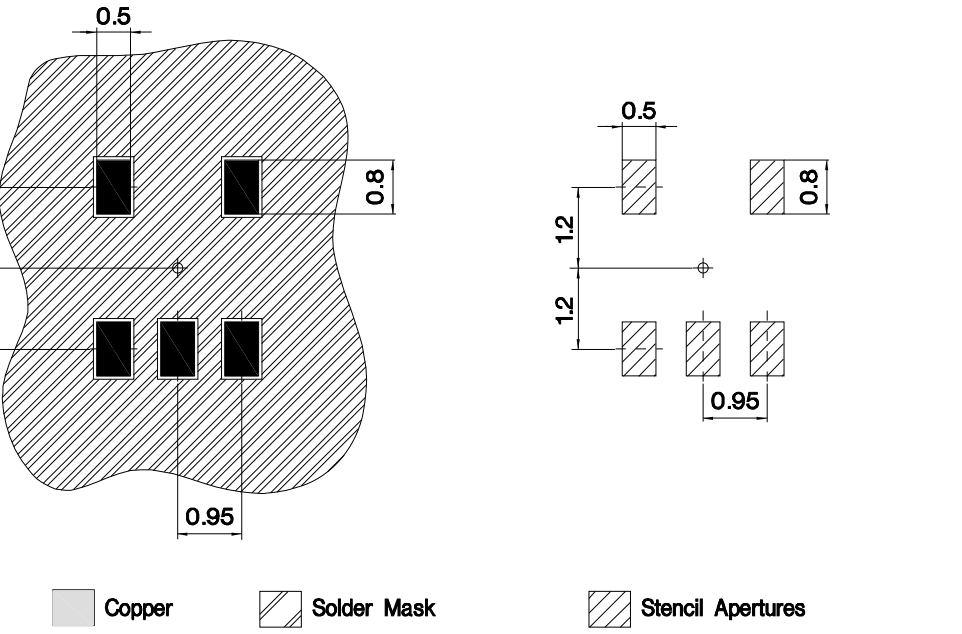

Figure 20 PG-SOT23-5-1 footprint dimensions

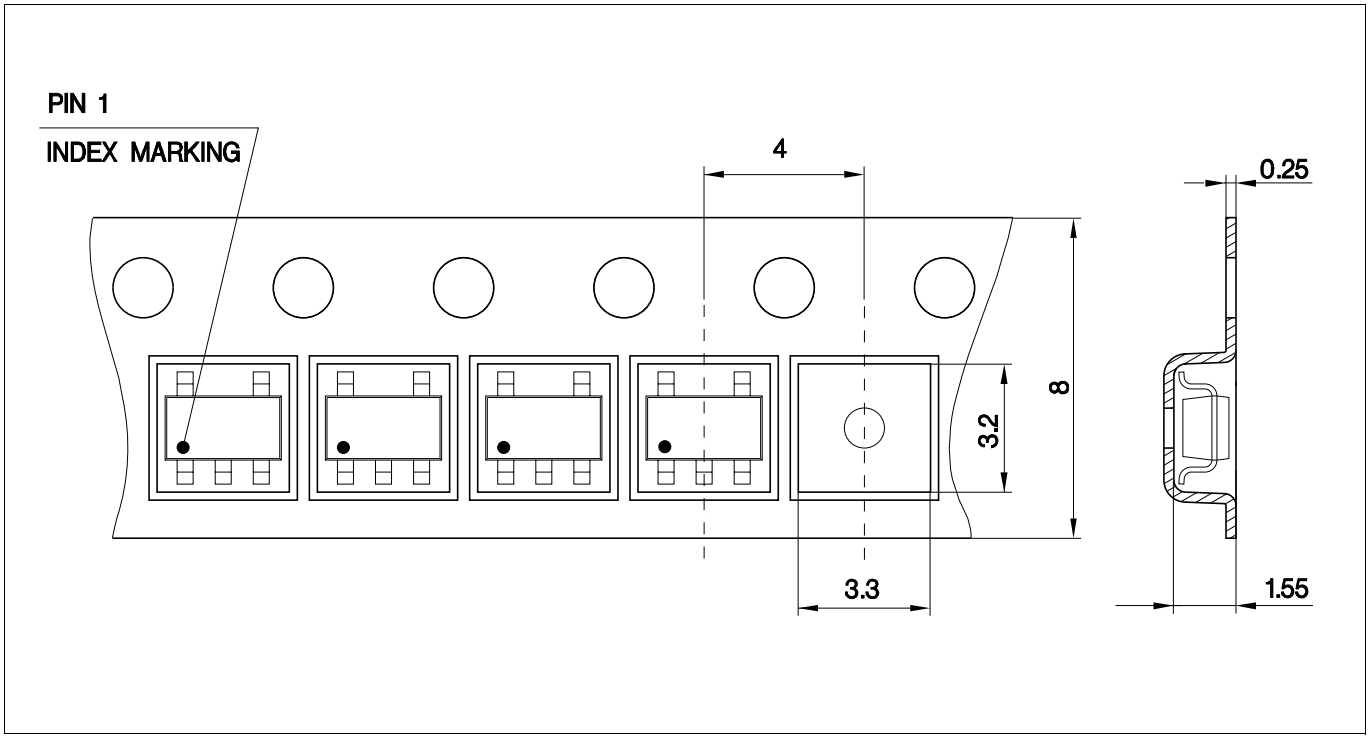

Figure 21 PG-SOT23-5-1 packaging dimensions

8.4 PG-WSON-6-1

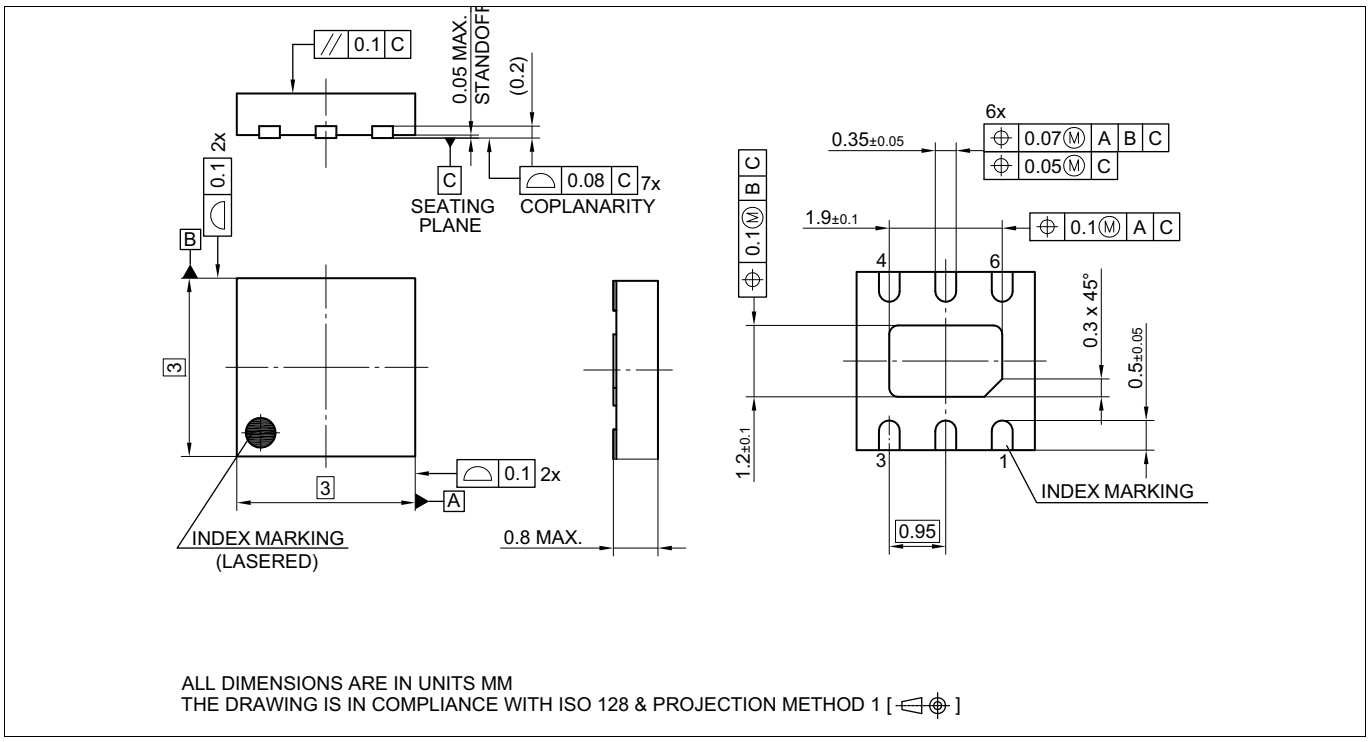

Figure 22 PG-WSON-6-1 outline dimensions

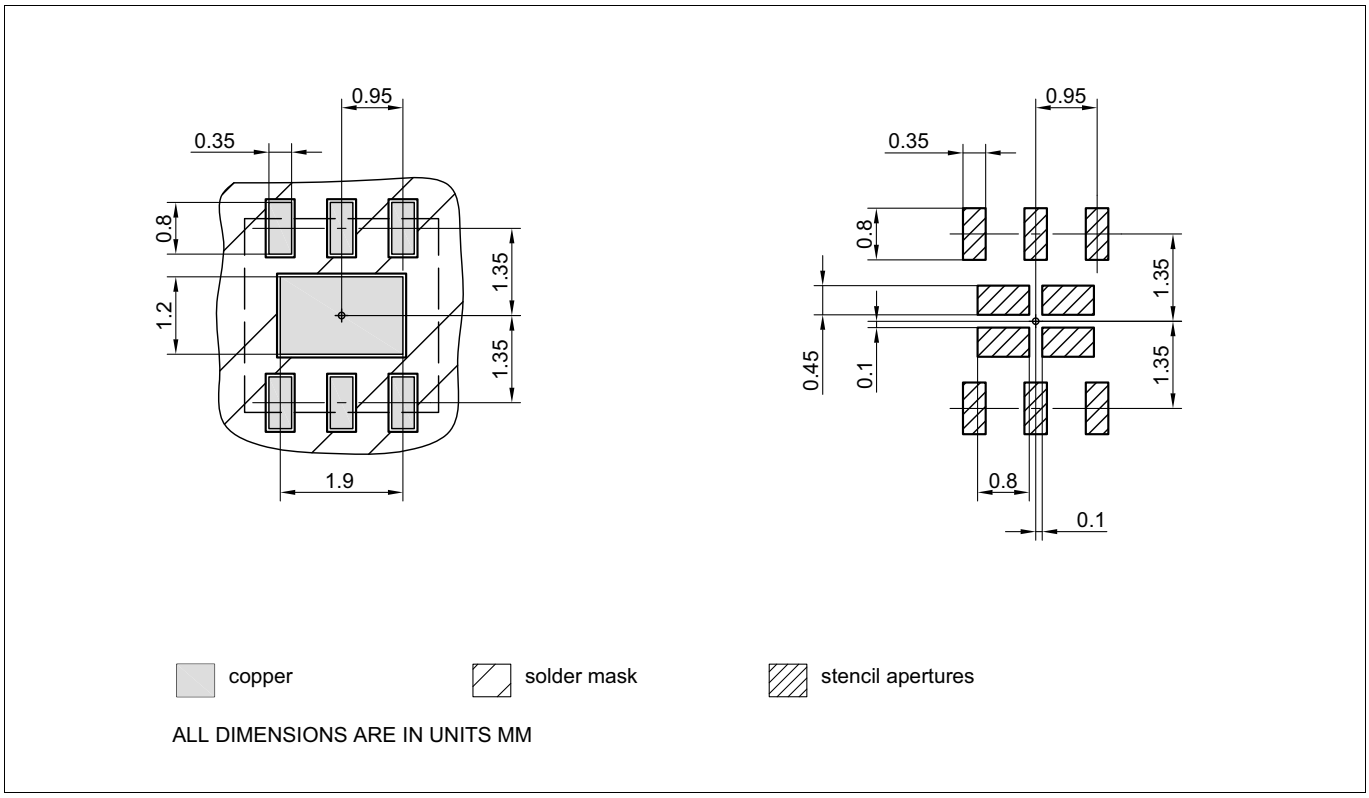

Figure 23 PG-WSON-6-1 footprint dimensions

Package outlines

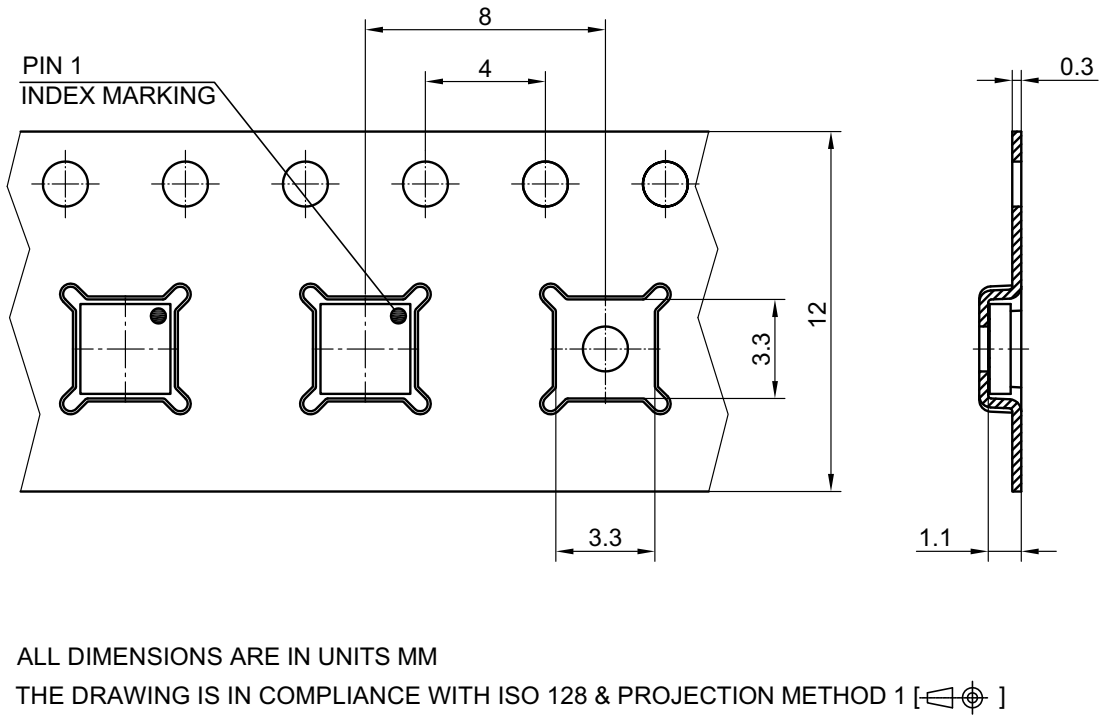

Figure 24 PG-WSON-6-1 packaging dimensions

Notes

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": **https://www.infineon.com/cms/en/product/packages/***
2. *Pin description and orientation is located in **Chapter 2***

9 Revision History

Version	Date	Changes
Rev.2.3	2022-01-21	• Specifications of 1EDN7511B, 1EDN8511B, 1EDN7512B, 1EDN7512G not changed • Editorial update in layout, figure and text on first page • Editorial update in **Product versions**, **Chapter 1** • Added pin numbers in **Table 1**, **Table 2** and **Table 3** • Added **Truth table**, **Table 4** • Updated **Absolute maximum ratings** for V_{OUT} (Repetitive pulse < 200ns) in **Table 5** • Added **Device numbers and markings**, **Table 14**
Rev.2.2	2018-04-20	• Updated package diagram PG-WSON-6-1
Rev.2.1	2017-10-02	• Restructured dimensional tolerances in drawing: **Figure 19**
Rev.2.0	2016-10-25	• Symbols correction: **Table 12** R_{on_SRC}, R_{on_SNK}, I_{SRC_peak}, I_{SNK_Peak} • Insert pulse timing diagram: **Figure 8** • Added max. and min. values of R_{on_SRC}, R_{on_SNK} in **Table 12**

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